Cat. No. 26-5404

$19.95

TECHNICAL REFERENCE

TANDY ELECTRONICS
Koninginneweg 222
1075 EM Amsterdam
020-645988 (computerafd.)
020-761426 (onderdelen)

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Technical Reference Manual

Table Of Contents

Table Of Contents

Appendices

List of Figures

List of Figures

1/ Introduction

The Radio Shack Model 2000 Personal Computer is modular in design to allow maximum flexibility in system configuration. The basic computer consists of a Main Unit, a detached keyboard with coiled cable for positioning the keyboard in the most convenient location, and a monitor. The Main Unit may be supplied with two internal floppy disk drives or one floppy disk drive and one internal hard disk drive. The standard monitor used with the Model 2000 is a monochrome display (green phosphor) which has a standard screen format of 80 characters width and 25 lines vertical. Since this unit is modular, it may be placed on top of the Main Unit or at any location convenient to the operator.

Internal floppy diskette storage is provided by either one or two 5-1/4" floppy disk drives. If the unit is supplied with two of these units, total internal memory storage capacity is 1.46 Mbytes. When supplied with the internal hard disk and one floppy disk storage unit, total internal memory storage becomes 10.73 Mbytes.

An optional Color Monitor may be used with the Model 2000 to provide up to eight of sixteen different colors on the screen at one time. This optional feature requires the use of a color monitor PCB assembly which plugs into one of the mother board slots at the rear of the Main Unit.

An internal 128K RAM board is standard on the Model 2000. An option to the Model 2000 is an additional 128K RAM board which provides expansion to 256K. Both boards are mounted internal to the Main Unit. An additional optional feature is a 256K RAM board which connects to the internal motherboard of the Main Unit. It is populated with 128K RAM which may be expanded to 256K RAM with the addition of RAM ICs. Two of these boards can be installed into the motherboard in the unit's card cage assembly. With all these options installed, the Model 2000 then has internal RAM memory capacity of 768K bytes.

Other options include a TV/Joystick input, a mouse/clock option which allows input from a hand-positioned interface, a monitor pedestal, black and white graphics option, and a floor unit which mounts the Main Unit vertically.

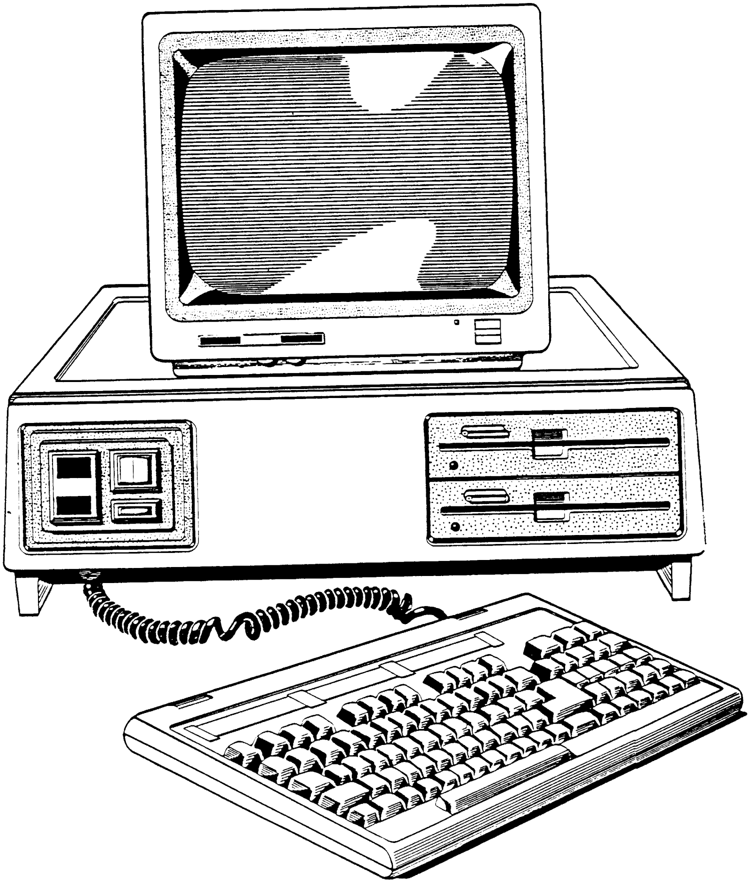
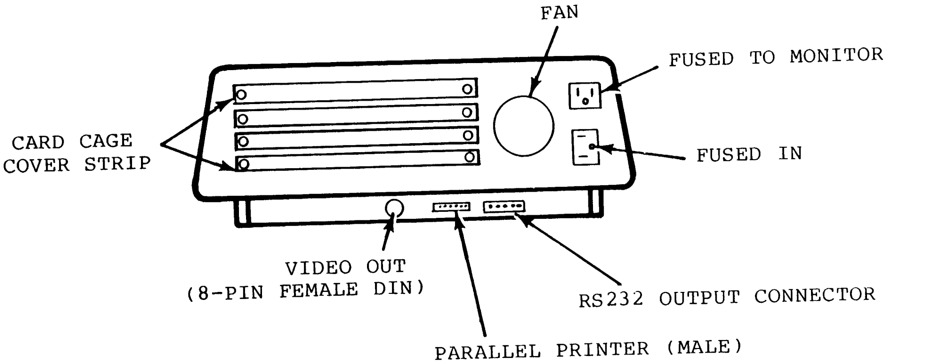


Figure 1.1 Model 2000 Computer Assembly

REAR VIEW



TOP VIEW

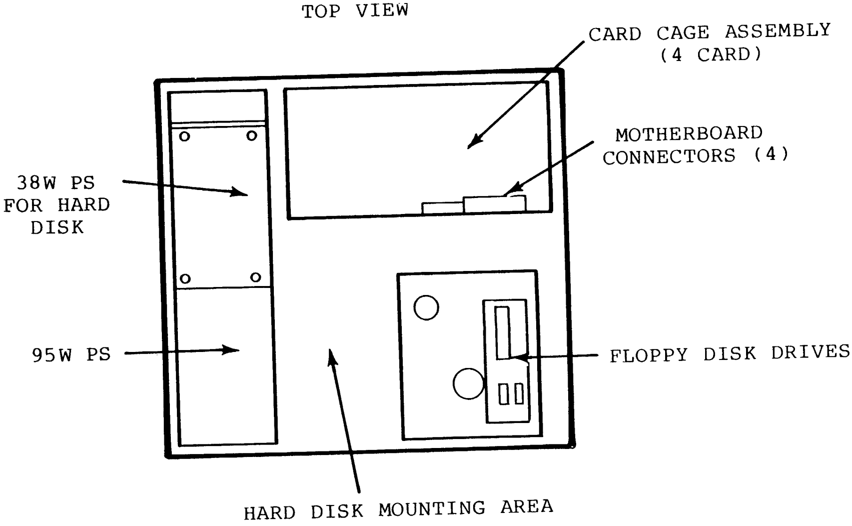


Figure 1.2 Model 2000 Major Component Subassemblies

The Main Unit is the heart of the Radio Shack Model 2000 microcomputer. It houses the microprocessor, Read-Only Memory (ROM - 16K for system start-up), system power supply, RAM boards and expansion slots for optional features, floppy disk drives (either one or two), and the internal hard disk drive and power supply.

The Main Logic Assembly is a large board mounted to the bottom of the Main Unit and interconnected to the keyboard, power supply, motherboard, and disk drives by a series of cables. A system block diagram is shown in Figure 1-1 showing the major components of the Model 2000 and the interconnecting cables. Both standard and optional features are included in this figure to provide a complete overall interconnection diagram of the unit.

The standard Power Supply for the Model 2000 microcomputer is a 95W switching regulator type, designed to provide adequate capacity for most all add-on features of the computer. When the system is supplied with the hard disk option, however, an additional 38W power supply is required to power the hard disk assembly separately.

The Model 2000 has a detachable keyboard which is connected to the Main Unit with a lightweight coiled cable which allows the keyboard to be used up to 3 feet away from the Main Unit for operator convenience. The keyboard features 90 keys in a standard typewriter keyboard layout with additional keys for numbers and functions.

The Floppy Diskette Drive uses special 5-1/4" double-sided, double-density diskettes to read, write or store data. These are 96 TPI soft sector diskettes. Two Disk Drive assemblies are installed in the standard unit, or it may contain one floppy disk drive and one internal hard disk drive assembly. Each of the floppy diskettes stores approximately 730 Kbytes of data. The hard disk drive is capable of storing 10 Mbytes of data. All system programs, with the exception of the system startup sequence, are stored on diskette.

The monitor used on the Radio Shack Model 2000 may be either a monochrome (#26-5111) or color (#26-5112) display. The monochrome monitor is a high resolution green phosphor display which provides excellent visual quality. It features a 12" screen with an anti-glare surface for improved viewing. The display is 25 lines of 80 characters each with the capability of displaying 256 different letters or characters. The characters are formed using a 7 x 9 matrix dot pattern.

Also available as an enhancement of the black and white monitor is a B/W graphics option board (26-5140). This feature allows the presentation of graphic material on the display monitor with individually addressed pixels. A color monitor (26-5112) is available which utilizes a 14" color screen, a color graphics option (26-26-5141), and the B/W graphics option to provide 8 color presentations at one time on the monitor.

Standard internal RAM memory consists of a plug-in 128K board. This board plugs into the Main Logic board and may be expanded to provide 256K of RAM with an additional 128K board (26-5160). In addition to this memory up to two 26-5161 boards (considered external since they are accessible from the outside of the Main Unit) may be plugged into the motherboard located at the rear of the Main Unit. These boards are populated with 128K of RAM and may be further expanded to 256K each with additional 64K x 1 RAM chips (option 26-5162). When all of these boards are incorporated into the system, they provide a total RAM capacity of 784K bytes of memory.

The TV/Joystick Board allows attachment of user-supplied Joy Sticks or paddles. Two joysticks may be attached to the Model 2000 for use with games available in the software library of the Model 2000.

The Mouse/Clock option board allows input with an external input device called a "mouse" as well as providing the time of day with a battery backup clock/calendar chip. The mouse is a unit which is rolled along a desk top and encodes a digital input to the computer.

A built-in RS-232 asynchronous interface allows communication with external devices through the use of a modem. These devices may be local or remote, using a telephone line to co'm@unicate. The option supports 50 to 9600 BPS transmission speeds and utilizes a 25-pin D connector located on the rear panel of the Main Unit.

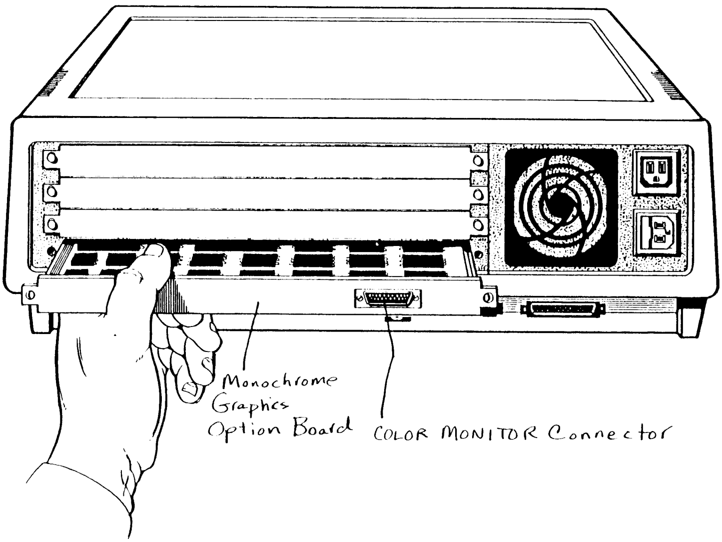


Figure 1.3 External Plug-in Option Cards

2/ Specifications

2.1 Physical Characteristics

Main Unit

Width	19.0 inches	(48.26 cm)
Height	6.0 inches	(15.24 cm)
Depth	16.0 inches	(40.64 cm)
Weight		
26-5103	23.0 pounds	(10.4 kgm)
26-5104	26.5 pounds	(12.0 kgm)

Monochrome Monitor

Width	16.25 inches	(41.28 cm)
Height	11.4 inches	(29.0 cm)
Depth	12.2 inches	(31.0 cm)
Weight	15.4 pounds	(7.0 kgm)

Keyboard

Width	16.25 inches	(41.28 cm)
Height	1.2 inches	(3.05 cm)
Depth	7.875 inches	(20.0 cm)
Weight	2.8 pounds	(1.3 kgm)

2.2 System Operating Characteristics

Storage Temperature - -40 to +160°F (-40 to 71°C)
Ambient Temperature - 55 to 95°F (12 to 35°C)
Voltage Range (USA) - 95 to 135 Vac
(Europe) - 190 to 270 Vac

Current Drain - USA - AC Main Unit/Convenience Outlet
Model 26-5103 - 3.0 Amperes
Model 26-5104 - 3.5 Amperes

European - AC current Main Unit only
Model 26-5103 - 0.94 Ampere
Model 26-5104 - 1.2 Amperes

Line Frequency - 47 to 63 Hz

2.3 Peripheral Interfaces

RS232C Connector - DB25 socket connector accessible at the rear of the main unit. Pinout connections are shown in Section 5 of this manual.

2.3 Peripheral Interfaces (con't)

Parallel Printer Connector - 34-pin connector for connection of parallel printer or modem for conversion to serial transmission. Pinout connections are shown in Section 5 of this manual.

Monochrome Monitor Connector - 8-pin socket DIN connector accessible at the rear of the Main Unit.

Motherboard - accessible from the rear of the Main Unit allows up to four optional boards to be plugged into main unit. Existing cover strip and Nylatch latches are removed and optional board is inserted and latched into place with Nylatch hardware.

2.4 Optional Features

Internal 128K RAM Board - plugs into existing 128K RAM board to give 256K bytes of internal RAM storage. Requires disassembly of the main unit for installation. See Section 2 on disassembly procedures.

External 256K Board - plugs into slot on Motherboard at rear of main unit. Supplied with 128K, but may have another 128K added for total of 256K bytes of external RAM.

TV/Joystick Board - plugs into slot on Motherboard and allows use of Joysticks for games available in software library of Model 2000.

Mouse/Clock Option Board - plugs into slot on Mother-board. Provides real time clock displayed on monitor screen as well as input from external "mouse" option, a hand-positioned transducer which translates "X" and "Y" position into digital encoded signal.

3/ Disassembly/Assembly

Since the Model 2000 is modular in its construction, disassembly/assembly procedures are simplified. The main modules which make up the Model 2000 are the Main Unit, the keyboard, and the display monitor. These three units may be supplemented by various I/0 devices such as printers, modems, memory devices or additional monitors. Disassembly of each module will be described in the following paragraphs. Exercise case when handling the modules to prevent damage to internal components or exterior surfaces.

3.1 Main Unit

The Main Unit contains the Power ON-OFF switch and indicator, the disk drives and the system power supply. All cables interconnect this unit with external devices. Most cables are connected to the rear terminal panel of the Main Unit but there are some connections to the front panel of the Main Unit, such as the keyboard connector. Attached to the bottom of the main unit is a metal chassis which houses the main logic PCB assembly. Turn the Main Unit assembly on either the left or right side to gain access to the mounting screws. There are four screws which attach this assembly to the Main Unit housing. When properly positioned, the logic board provides interconnection from this base PCB to the Mother Board which is used for interconnecting optional feature boards. In addition to this 96-pin connector, there are other connectors which tie to the PCB. When the screws are removed from the base cover, swing the rear of the cover away from the main unit. This will allow the connectors which are at the front of the unit to be removed without damaging them.

Disconnect all connections to the main logic PCB (these include the power input, reset, and sound). With these connectors disconnected, the base assembly may be removed completely from the Main Unit assembly. The PCB is attached to the metal base assembly with nine screws. There is an insulating separator to prevent possible shorting of any of the components on the PCB to the metal base assembly.

The Main Unit housing contains the Power Supply, the Disk Drive Assemblies (either two floppy disk drives or 1 floppy and 1 hard disk drive) and the Motherboard for system options. To gain access to the interior of this unit, remove two mounting screws at the lower rear of the Main

Unit. After removing these two screws, slide the top cover forward to release the catches at the front, then lift the top cover off the assembly. The back panel portion of the case housing remains a part of the Main Unit base as well as the power switch/reset and indicator.

3.1.1 Power Supply

The 95W main power supply for the Model 2000 is located at the left side of the Main Unit and is accessible when the cover is removed from the Main Unit as noted previously. The power supply is attached to the base of the Main Unit with 6 screws, 4 of which are screwed into the bottom of the base and 2 of which are attached to the backside of the front bezel If the Main Unit has a Hard Disk assembly installed, it must be detached to provide access to the connectors which connect the power supply to the Main Logic PCB.

1. Remove the connectors attached to the Motherboard, disk drives, and Main Logic PCB.

2. Remove 4 screws which attach the power supply assembly to the base plastic.

3. Remove the two screws which connect the power supply to the front bezel assembly.

4. Lift the power supply from the Main Unit.

5. Remove 3 screws from the RH side of the power supply to allow the upper enclosure to be lifted off the supply.

6. Remove 4 connectors which attach to the power supply PCB.

7. Remove 8 screws which attach the PCB to the lower enclosure weldment.

8. Cable replacement is accomplished by removing the connectors from the enclosure weldment. All connectors are clip-mounting type connectors which allow replacement without special tools. Remove wires attached to the connector and then depress retaining clips from inside the enclosure. Slide connector out of enclosure weldment.

Assemble the power supply in the reverse order of disassembly. Ensure that the power supply is properly operating before reinstalling it in the Main Unit. See Section 7.2 for checkout procedures for the main power supply.

The 38W Hard Disk power supply assembly is attached to the underside of the power supply cover and nests above the main power supply PCB. It is accessible when the cover is removed from the main supply.

1. Remove the cover from the main unit as noted in Paragraph 3.1.

2. Remove the main power supply cover by removing the 4 mounting screws.

3. Remove the mating connectors to the 38W power supply -- there are two connectors. One is for AC input and the other for DC output. There are three DC output connectors on the PCB. The DC output connector may be attached to any one of the three on reassembly.

4. Remove the 38W power supply board from the cover by removing the 4 mounting screws.

Reassembly of the power supply is in the reverse order of disassembly. Ensure that the orientation of the supply is the same as it was prior to disassembly to prevent interference with the main power supply PCB components.

3.1.2 Disk Drives

The floppy disk drives are mounted at the right side of the Main Unit, attached to the base of the main unit with a mounting bracket on either side of the drives. The drive assemblies (including mounting brackets) may be removed from the Main Unit base by removing 4 screws in the base. After these screws and cables connected to the drives are removed, the drive assembly may be removed completely from the Main Unit.

The hard disk assembly is mounted to the left of the floppy disk drive assemblies. If the unit contains a hard disk drive assembly, it is removed from the Main unit by removing the four mounting screws and attached cables.

3.2 Keyboard Assembly

The keyboard assembly is connected by a coiled cable attached to the left side of the front plate of the Main Unit. Disconnect this connector to completely detach the keyboard assembly. Disassemble the keyboard as noted below.

3.2.1 Disassembly

1. After removing the connector from the Main Unit, turn the keyboard assembly upside down on a soft surface to prevent scratching the surface or keys.

2. Remove three screws from the front of the keyboard. Keep separate so that they mayu be replaced in the front 3 mounting holes.

3. Remove remaining 6 screws from the sides and back of the keyboard assembly.

4. Hold the top and bottom of keyboard assembly together and turn the assembly rightside up.

5. Lift the top cover off the assembly, exposing the keyboard printed circuit board.

6. Disconnect the cable connector at the right rear of the keyboard assembly and remove the keyboard PCB.

7. Lift the keyboard supports from the rear of the keyboard. These are positioned over the support springs in the keyboard base (two on each side).

8. The cable is secured to keyboard base with a strain relief. If necessary, squeeze the strain relief to remove the cable from the base.

9. The cable wire connections must be removed from the connector to replace the cable assembly. Use a small tool to depress spring clip in the connector and pull the wire/clip end from the connector.

10. The four keyboard support springs slide into the base from the outside of the plastic holders. See the exploded view in Section 8 if required.

3.2.2 Assembly

The keyboard is assembled in the reverse order of disassembly. Ensure that the keyboard supports are properly positioned on the support springs prior to installing the top cover. Also ensure that the shorter mounting screws are used in the front positions of the keyboard assembly to prevent damage to the keyboard plastic.

3.3 Display Unit

The Display Unit for the Tandy Model 2000 computer may be either monochrome or color, depending on individual requirements. Servicing either of the two units is covered in the service manual for the particular type monitor used. See the supplemental sections at the end of this Model 2000 service manual for servicing information.

4/ Adjustments

4.1 Power Supply Adjustment

Adjustment of voltage sources required by the Model 2000 is contained in Paragraph 7.2.1.3 Performance Test. These voltages include +5 Vdc, +12 Vdc, and -12 Vdc.

4.2 PLL Adjustment

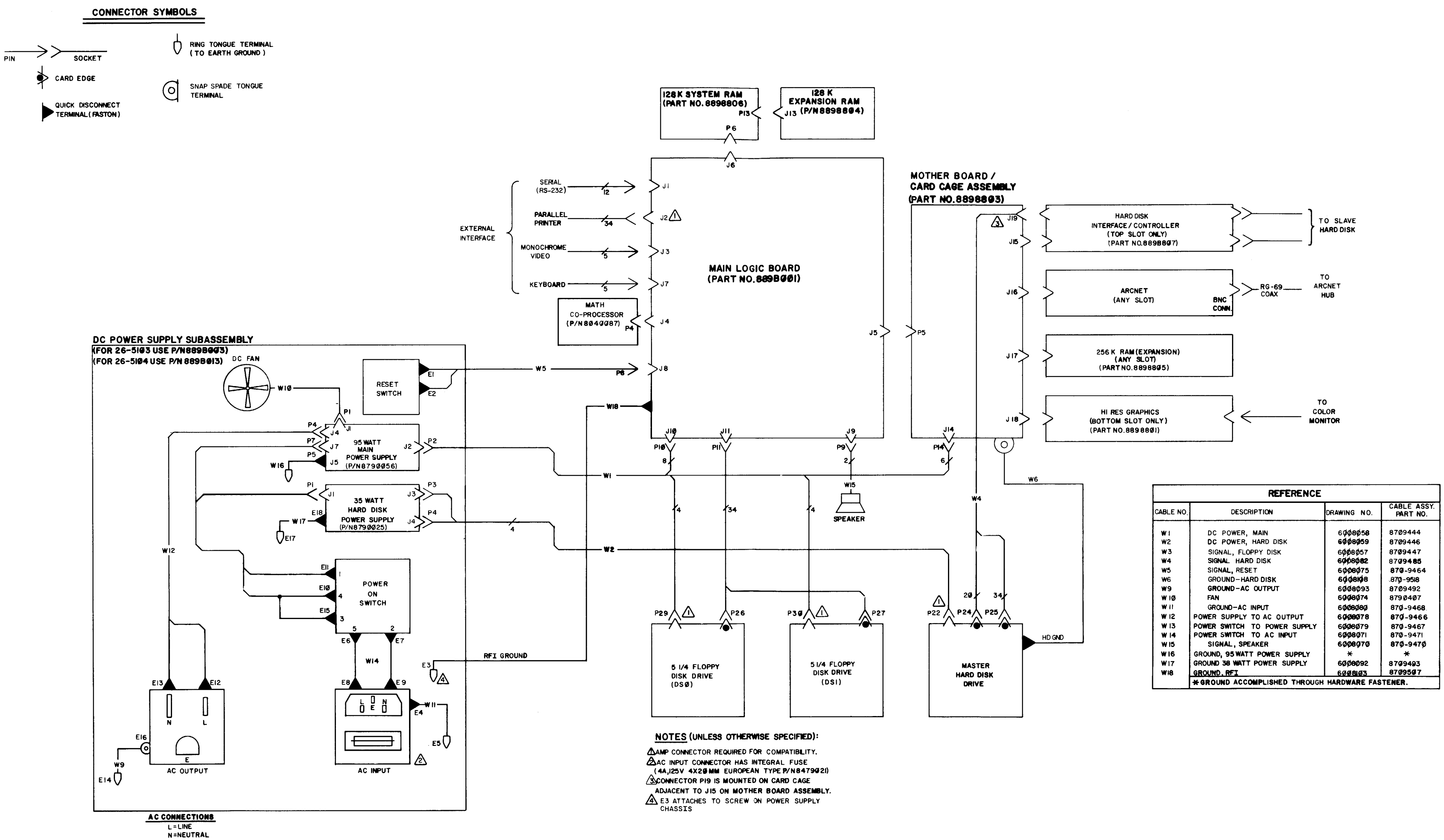
Adjustment of the PLL circuitry is accomplished by the adjustments noted in Paragraph 7.1.7.4.

4.3 Video Adjustment

Adjustments to the video circuits should be made according to the alignment instructions noted in the supplements contained in Section 10 of this manual. Instructions are included for both the Monochrome and Color Monitors.

5/ Cabling Diagrams/Pinout Connections

This section of the manual contains connector diagrams and pin out descriptions of the connectors used in the Model 2000 microcomputer. Figure 7-1 shows an interconnecting wiring diagram and identifies the connectors by symbol number. The following pages then show physical representation of the connector and corresponding pin designations.



NOTES (UNLESS OTHERWISE SPECIFIED):

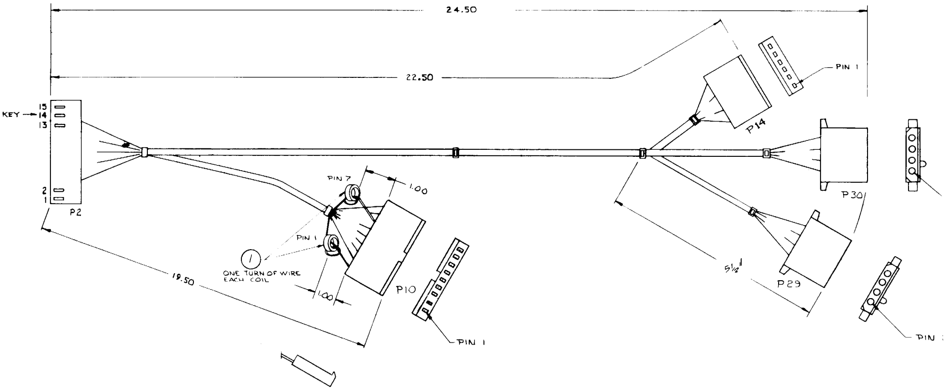
1. AMP CONNECTOR REQUIRED FOR COMPATIBILITY.
2. AC INPUT CONNECTOR HAS INTEGRAL FUSE (4A,125V 4X20MM EUROPEAN TYPE P/N8479021)
3. CONNECTOR P19 IS MOUNTED ON CARD CAGE ADJACENT TO J15 ON MOTHER BOARD ASSEMBLY.
4. E3 ATTACHES TO SCREW ON POWER SUPPLY CHASSIS

REFERENCE

CABLE NO.	DESCRIPTION	DRAWING NO.	CABLE ASSY. PART NO.
W1	DC POWER, MAIN	6008058	8709444
W2	DC POWER, HARD DISK	6008059	8709446
W3	SIGNAL, FLOPPY DISK	6008057	8709447
W4	SIGNAL HARD DISK	6008082	8709485
W5	SIGNAL, RESET	6008075	870-9464
W6	GROUND-HARD DISK	6008108	870-9518
W9	GROUND-AC OUTPUT	6008093	8709492
W10	FAN	6008074	8790407
W11	GROUND-AC INPUT	6008080	870-9468
W12	POWER SUPPLY TO AC OUTPUT	6008078	870-9466
W13	POWER SWITCH TO POWER SUPPLY	6008079	870-9467
W14	POWER SWITCH TO AC INPUT	6008071	870-9471
W15	SIGNAL, SPEAKER	6008070	870-9470
W16	GROUND, 95 WATT POWER SUPPLY	*	*
W17	GROUND 38 WATT POWER SUPPLY	6008092	8709493
W18	GROUND, RFI	6008103	8709507
	*GROUND ACCOMPLISHED THROUGH HARDWARE FASTENER.		

Connector/Cable Interconnection Diagram 8000206A
Model 2000 Computer

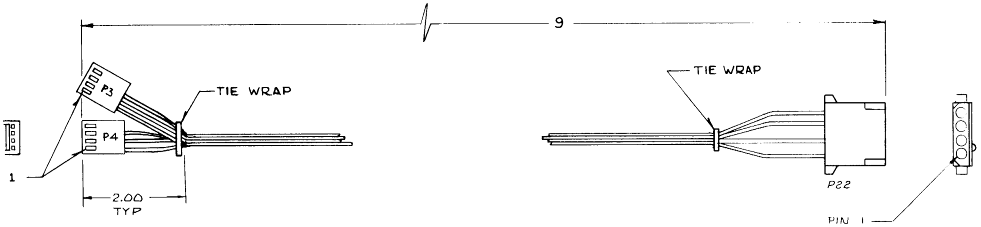
Connector/Cable Interconnection Diagram 8000206A
Model 2000 Computer



PARTS LIST				
DES	QTY	DESCRIPITION	MFG / PART NO.	REMARKS
P2	1	CONN, SOCKET 15 POSITION	MOLEX / 09-50-3151	
	15	COUTACT	MOLEX / 08-50-0105	FEMALE PIN
P10	1	CONN SOCKET 9 POSITION	MOLEX / 09-50-3091	
	9	CONTACT	MOLEX / 08-50-0105	
P14	1	CONN SOCKET 6 POSITION	MOLEX / 09-50-3061	
	6	CONTACT	MOLEX / 08-50-0105	
P29 P30	2	CONN SOCKET 4 POSITION	AMP / 1-480424-0	
	8	COUTACT	AMP / 61117-1	
	1	KEY	MOLEX / 15-04-0219	
1	2	COIL, TORID	FAIR-RITE / 5943000201	+12V & -12V ON P10

WIRE LIST								
FUNCTION	WIRE		CONNECTO / PIN #					
	AWG	COLOR		P2	P10	P14	P29	P30
+12V	20	ORG		1			1	
	20			1				1
	20			2	1			
+12V	20	ORG		2		1		
GND	18	BLK		3			2	
				3			3	
				4				2
				4				3
				5	5			
				5	6			
				6	8			
				7		3		
GND		BLK		7		5		
+5V		RED		8	3			
				9	4			
				10			4	
				10				4
				11		2		
+5V	18	RED		12		4		
−12V	20	WHT		13	7			
−12V	20			13		6		
KEY	−	−		14				
ACLO	20	GRY		15	2			

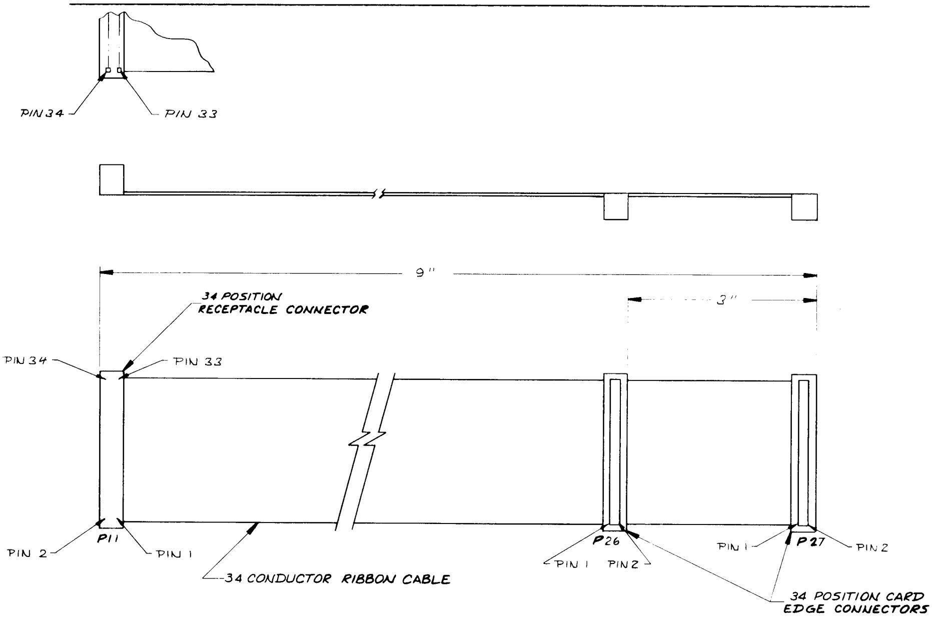
Cable Assembly W1 (6008058)



WIRE LIST									
FUNC-TION	WIRE		CONNECTOR / PIN NO.						
	AWG	COLOR		P22		P3		P4	
+12V	20	ORG.		1		3		–	
+12V	20	ORG.		1		–		3	
GND	20	BLK		2		2		–	
GND	20	BLK	···	3		–		2	
+5V	20	RED		4		1		–	
+5V	20	RED		4		–		1	

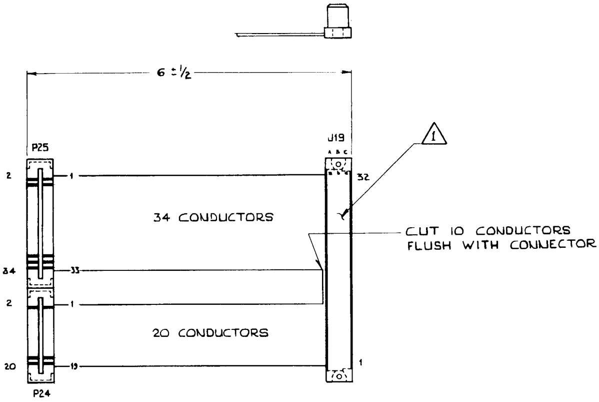
PARTS LIST				
DES	QTY	DESCRIPTION	MFG PART NO.	REMARKS
P22	1	CONN. SOCKET, 4 POSITION	AMP / 1-480424-0	
	4	CONTACT	AMP / 61117-1	
P4/P3	2	CONN. SOCKET, 4 POSITION	MOLEX / 22-01-3047	
	8	CONTACT	MOLEX / 08-50-0113	

Cable Assembly W2 (6008059)



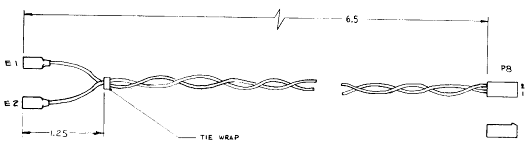
PARTS LIST				
DES	QTY	DESCRIPTION	MFG / PART NO.	REMARKS
P11	1	CONN., 34-PIN RECEPTACLE	MOLEX / 15-29-3343	STRAIN RELIEF 15-25-1343
P26,27	2	CONN., 34-PIN EDGE CARD	3M / 3463-0001	
		.	AMP/ 499930-3	
		CABLE 34-COND.,.050 PITCH		

Cable Assembly W3 (6008057)



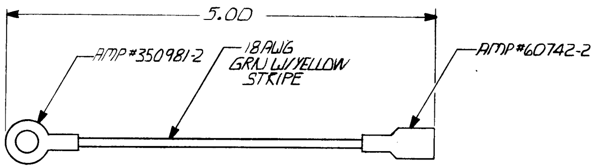
PARTS' LIST					
DESIGNATION	QTY.	DESCRIPTION	MFG.	PART NUMBER	REMARKS
J19	1	96 PIN EURO CONNECTOR	BURNDY	BPS3B96AcRaFoZ1	ROWS A & C LOADED
			BERG	75860-001	
			CANNON	G06M96P3BLBL-004	
P24	1	20 POSITION EDGE CARD CONNECTOR	AMP	499930-6	
			3M	3461-0001	
P25	1	34 POSITION EDGE CARD CONNECTOR	AMP	499930-3	
			3M	3463-0001	
W2	1	64 COND. FLAT CABLE .050 PITCH CABLE			

Cable Assembly W4 (6008082

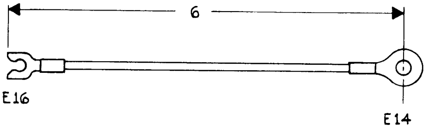


PARTS' LIST					
DESIGNATION	QTY.	DESCRIPTION	MFG.	PART №	REMARKS
X1	1	E1-P7,2 : BLK. 20 AWG GND. E1-P7,1 : GRAY 20 AWG RESET			± 1/2 LENGTH TOLER.
E1, E2	2	QUICK DISCONNECT	AMP	2-350803-2	FULLY INSULATED
P8	1	HOUSING, 2 PIN	MOLEX	09-50-3021	W/LOCKING RAMP
	2	CONTACT	MOLEX	08 50 0105	

Cable Assembly W5 (6008075)

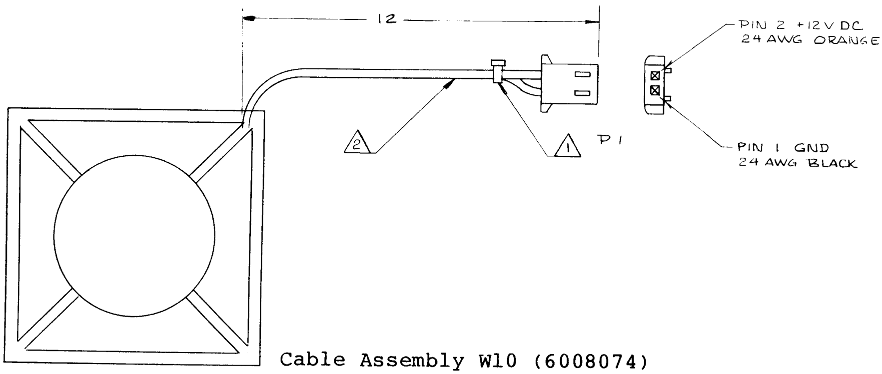


Cable Assembly W6 (6008108

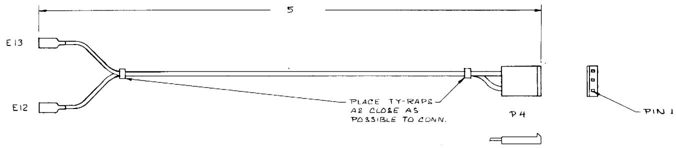


PARTS' LIST				
DES.	QTY.	DESCRIPTION	MFG.	P/N
E14	1	RING TERMINAL	AMP	350981-2
E16	1	SNAPSPADE TERM.	AMP	640769-1
	1	WIRE, 18 AWG. GRN. W/YELLOW STRIPE		

Cable Assembly W9 (6008093)



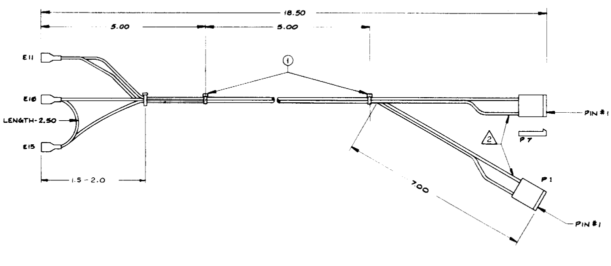
Cable Assembly W10 (6008074)



WIRE LIST									
FUNCTION	WIRE			CONNECTOR / PIN #					
	AWG	COLOR			P4				
LINE	18	BRN		E12	1				
NEUTRAL	18	BLU		E13	3				

PARTS LIST				
DES	QTY	DESCRIPTION	MFG / PART NO.	REMARKS
P4	1	3 CKT HOUSING W/LOCK RAMP	MOLEX / 09-50-3031	
	2	CONTACTS	MOLEX / 08-50-0105	
E12 E13	2	QUICK DISCONNECT (.25x.03)	AMP 2-520183-2	FULLY INSULATED

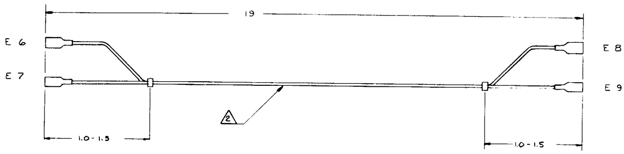
Cable Assembly W12 (6008078



WIRE LIST							
FUNCTION	WIRE		CONNECTOR / PIN #				
	AWG	COLOR	P7	P1	E10	E11	E15
LINE	18	BROWN	1		1		
LINE	18	BROWN			1		1
LINE	18	BROWN		1			1
NEUTRAL	18	BLUE	3			1	
NEUTRAL	18	BLUE		3		1	

PARTS LIST					
DESIGNATION	QTY	DESCRIPTION	MFG	PART NO.	REMARKS
P7, P1	2	3 POS CONN, W/LOCKING RAMP	MOLEX	09-50-3031	
	4	CONTACT	MOLEX	08-50-0105	
E10, E11, E15	3	1/4 X 1/32 QUICK DISCONNECT	AMP	3-350819-2	FULLY INSULATED
(1)	2	TIE WRAP			

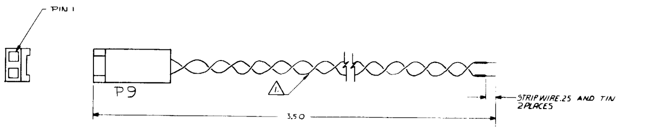
Cable Assembly W13 (6008079)



WIRE LIST					
FUNCTION	WIRE		CONNECTOR / PIN NO.		
	AWG	COLOR			
LINE	18	BRN	E6	E 8	
NEUT	18	BLU	E7	E9	

PARTS LIST				
DES	QTY	DESCRIPTION	MFG/PART NO.	REMARKS
E6-E9	4	QUICK DISCONNECT .25x.03	AMP 2-350803 2	FULLY INSULATED
	2	TIE WRAP		

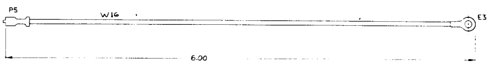
Cable Assembly W14 (6008071)



WIRE LIST				
FUNCTION	WIRE		CONNECTOR / PIN NO.	
	AWG	COLOR	P-9	
SPKROUT	24	GRY	1	TO SPEAKER + TERMINAL
GND	24	BLK	2	TO SPEAKER - TERMINAL

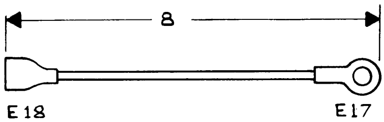
PARTS LIST				
DES	QTY	DESCRIPTION	MFG / PART NO.	REMARKS
P9	1	CONN SOCKET 2 POS	MOLEX / 22 01-3027	
	2	CONTACT	MOLEX / 08-50-0113	

Cable Assembly W15 (6008070



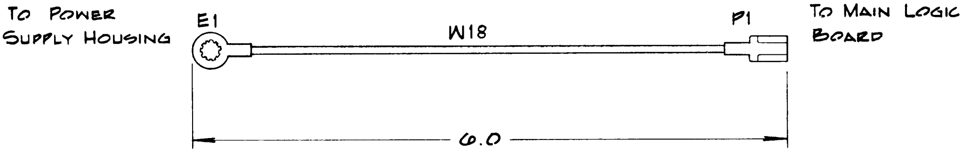
PARTS' LIST					
DESIGNATION	QTY.	DESCRIPTION	MFG.	PART №	REMARKS
P5	1	1/4 X 1/32 QUICK DISCONECT	AMP	42400-2	INSULATED BARREL
E3	1	RING TERMINAL	AMP	350981-20	INSULATED BARREL
W16	1	18 GA. GREEN W/YELLOW STRIP WIRE			± 1/2 LENGTH TOLER.

Cable Assembly W16 (6008080



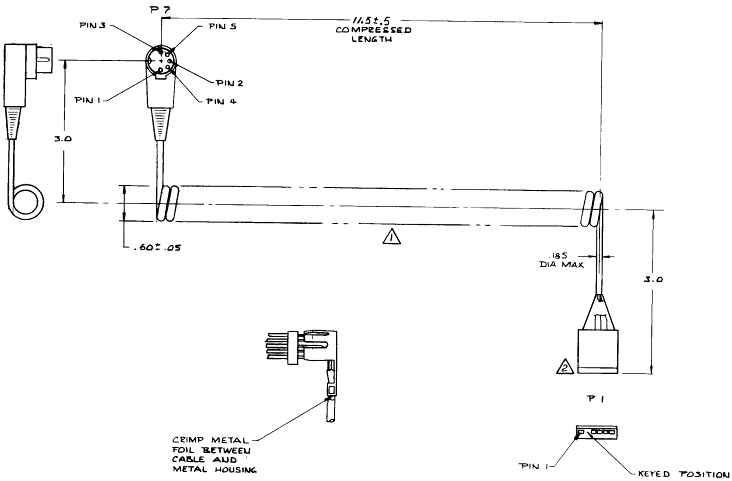
PARTS' LIST					
DES.	QTY.	DESCRIPTION	MFG.	P/N	REMARKS
E18	1	1/4 x 1/32 QUICK DISCONECT	AMP	42-400-2	INS. BARREL
E17	1	RING TERMINAL	AMP	350981-2	INS. BARREL
	1	18 GA. GRN. W/ YELLOW STRIPE WIRE.			

Cable Assembly W17 (6008092)



PARTS LIST				
DES	QTY	DESCRIPTION	MFG / P.N.	REMARKS
E1	1	RING TERMINAL	AMP / 61793-1	OR EQUIVALENT
P1	1	.250 FASTON RECEPTACLE	AMP / 42400-2	OR EQUIVALENT
W1	1	AWG 12/65 STRANDS OF 30 GA		GREEN W/ YELLOW STRIPE

Cable Assembly W18 (6008103)



WIRE LIST								
FUNCTION	WIRE		CONNECTOR / PIN NO.					
	AWG	COLOR	P7	P1				
KBDDAT	26	BLK	1	1				
KBDCLK	26	GRN	4	3				
KBDBSY*	26	YEL	2	4				
+5VDC	26	RED	5	5				
GND	22	[illegible]	3	6				

PARTS' LIST				
DES	QTY	DESCRIPTION	MFG/PART NO	REMARKS
P 7	1	CONN 5 PIN DIN RT ANGLE	HOSHIDEN/[illegible]	
P 1	1	6 CKT HOUSING	MOLEX / 22-01-3069	[illegible] KEY IN POS 2
	5	CONTACT	MOLEX / 08-50-0113	

Keyboard Cable Assembly 6008072

MAIN LOGIC PCB REV. @

J1 - SERIAL INTERFACE (RS-232C)
(25-PIN FEMALE RT. ANGLE DB25)

01	GROUND	02	SERTD*
03	SERRD	04	SERRTS
05	SERCTS	06	SERDSR
07	GROUND	08	SERCD
09	NO CONNECTION	10	NO CONNECTION
11	NO CONNECTION	12	NO CONNECTION
13	NO CONNECTION	14	NO CONNECTION
15	SERTXC	16	NO CONNECTION
17	SERRXC	18	NO CONNECTION
19	NO CONNECTION	20	SERDTR
21	NO CONNECTION	22	SERRI
23	NO CONNECTION	24	NO CONNECTION
25	NO CONNECTION		

J2 - PARALLEL INTERFACE
(34-PIN MALE SHROUDED RT. ANGLE)

01	LPRDATSTB	02	GROUND
03	LPRD0	04	GROUND
05	LPRD1	06	GROUND
07	LPRD2	08	GROUND
09	LPRD3	10	GROUND
11	LPRD4	12	GROUND
13	LPRD5	14	GROUND
15	LPRD6	16	GROUND
17	LPRD7	18	GROUND
19	LPRACK*	20	GROUND
21	LPRBSY	22	GROUND
23	LPRPAEM	24	GROUND
25	LPRSEL*	26	STROBEIN
27	GROUND	28	LPRFLT*
29	LPRIN0	30	LPRIN1
31	GROUND	32	LPRIN2 @
33	GROUND	34	INBUFFULL

MAIN LOGIC PCB REV. PP2

J3 - MONOCHROME VIDEO
(8-PIN DIN RT. ANGLE)

1	NO CONNECTION
2	GROUND
3	INTMON
4	BUSHSYNC
5	BUSVSYNC
6	NO CONNECTION
7	VIDEOMON
8	NO CONNECTION

J4 - MATH CO-PROCESSOR CONNECTOR
(DUAL 31-PIN, 0.100" GRID)

01	+ 5 VOLTS	02	GROUND
03	S0*	04	S1*
05	S2*	06	RESET
07	CLKOUT	08	BHE*
09	AD19	10	AD18
11	AD17	12	AD16
13	AD15	14	AD07
15	AD14	16	AD06
17	AD13	18	AD05
19	AD12	20	AD04
21	AD10	22	AD11
23	AD09	24	AD03
25	AD08	26	AD02
27	AD00	28	AD01
29	RD*	30	RD*
31	WR*	32	WR*
33	ALE	34	ALE
35	ARDY	36	ARDY
37	HOLD	38	HOLD
39	MCS0*	40	MCS0*
41	DT/R*	42	DT/R*
43	NO CONNECTION	44	MCS2*
45	NO CONNECTION	46	MCS3*
47	MCS1*	48	MCS1*
49	GROUND	50	TEST*
51	HLDA	52	HLDA
53	DEN*	54	DEN*
55	SRDY IN	56	DRQ0
57	SRDY OUT	58	DRQ1
59	LATCHED SRDY	60	MCPINT14
61	+5 VOLTS	62	GROUND

NOTE: SIGNALS INTERCEPTED AND REGENERATED BY THE MATH CO-PROCESSOR ARE INDICATED BY BOLD FACE PRINT. A JUMPER TO THE CORRESPONDING SIGNAL IS REQUIRED WHEN THE MATH CO-PROCESSOR IS NOT USED. THESE JUMPERS ARE INCORPORATED ON THE PCB ARTWORK ON THE SOLDER SIDE OF THE BOARD AND MUST BE CUT WHEN INSTALLING THE MATH CO-PROCESSOR.

MAIN LOGIC PCB REV. PP2

J5 - MOTHER BOARD CONNECTOR
(96-PIN MALE EUROCONNECTOR)

01a	NO CONNECTION	01b	NO CONNECTION	01c	NO CONNECTION
02a	GND	02b	AGVID	02c	NO CONNECTION
03a	GND	03b	GND	03c	GND
04a	BUSBLANK	04b	G/A	04c	BUSDOTCLK
05a	BUSCLK	05b	BUSHSYNC	05c	BUSVSYNC
06a	NMI*	06b	GND	06c	AINT
07a	BUSVLT	07b	NO CONNECTION	07c	NO CONNECTION
08a	BUSPCLK	08b	BUSINT03	08c	BUSPCS5*
09a	BUSRFSH*	09b	BUSINT16	09c	BUSPCS4*
10a	BUSIOR*	10b	HDCINT06	10c	BUSPCS3*
11a	BUSHLDA*	11b	RATINT12	11c	BUSLOCK*
12a	BUSBHE*	12b	BUSIOW*	12c	BUSDMARQ1*
13a	BUSMCS1*	13b	BUSMCS0*	13c	BUSDMARQ2*
14a	BUSMR*	14b	BUSMW*	14c	BUSARDY*
15a	BUSRFINH*	15b	BUSL/E*	15c	BUSINT05
16a	BUSMRST*	16b	BUSDEN*	16c	BUSINT07
17a	BUSDT/R*	17b	BUSDMACK3*	17c	BUSINT17
18a	BUSDMACK2*	18b	MEMINT15	18c	BUSDMACK1*
19a	BUSALE	19b	BUSHOLD*	19c	BUSDMARQ3*
20a	GND	20b	GND	20c	GND
21a	BUSD04	21b	BUSD05	21c	BUSD03
22a	BUSD06	22b	BUSD07	22c	BUSD15
23a	BUSD00	23b	BUSD01	23c	BUSD02
24a	BUSD14	24b	BUSD10	24c	BUSD11
25a	BUSD13	25b	BUSD09	25c	BUSD12
26a	BUSD08	26b	BUSA04	26c	BUSA00
27a	BUSA11	27b	BUSA12	27c	BUSA07
28a	BUSA18	28b	BUSA17	28c	BUSA15
29a	BUSA19	29b	BUSA13	29c	BUSA14
30a	BUSA08	30b	BUSA09	30c	BUSA01
31a	BUSA10	31b	BUSA03	31c	BUSA02
32a	BUSA16	32b	BUSA06	32c	BUSA05

MAIN LOGIC PCB REV. PP2

J6 - SYSTEM RAM INTERFACE
(40-PIN MALE HEADER, STRAIGHT)

01	IB01	02	IB00
03	IB02	04	IB04
05	IB03	06	IB05
07	IB07	08	IB06
09	DIPL	10	DOPL
11	WR0*	12	DMEMA06
13	RAS0*	14	DMEMA03
15	DMEMA00	16	DMEMA04
17	DMEMA02	18	DMEMA05
19	DME@A01	20	DMEMA07
21	GND	22	CASU*
23	GND	24	GND
25	+5 VOLTS	26	+5 VOLTS
27	+5 VOLTS	28	RAS1*
29	WR1*	30	CASL*
31	DOPU	32	DIPU
33	IB12	34	IB15
35	IB11	36	IB14
37	IB10	38	IB08
39	IB09	40	IB13

J7 - KEYBOARD INTERFACE
(5-PIN DIN, RT. ANGLE)

01	KBDDAT	02	KBDBSY*
03	GROUND	04	KBDCLK
05	KBDPOWER		

J8 - RESET
(2-PIN MOLEX W/FRICTION LOCK)

01	RES*	02	GROUND@

J9 - SPEAKER
(2-PIN MALE HEADER, POLARIZED)

01	SPKDRV	02	GROUND

J10 - DC POWER
(9-PIN MALE HEADER, POLARIZED)

01	+12 VOLTS
02	ACLO*
03	+5 VOLTS
04	+5 VOLTS
05	GND
06	GND
07	-12 VOLTS
08	.GND
09	NO CONNECTION

J11 - FLOPPY DISK CONTROLLER INTERFACE
(34-PIN MALE HEADER, STRAIGHT)

01	GROUND	02	NO CONNECTION
03	GROUND	04	FLDINUSE*
05	GROUND	06	NO CONNECTION
07	GROUND	08	FLDIDX*
09	GROUND	10	FLDDS0*
11	GROUND	12	FLDDS1*
13	GROUND	14	NO CONNECTION
15	GROUND	16	FLDMTRON*
17	GROUND	18	FLDDIR*
19	GROUND	20	FLDSTP*
21	GROUND	22	FLDWRDAT*
23	GROUND	24	FLDWE*
25	GROUND	26	FLDTRK0*
27	GROUND	28	FLDWRPRT*
29	GROUND	30	FLDRDDAT*
31	GROUND	32	FLDSDSEL*
33	GROUND	34	FLDRDY*

EXPANSION RAM PIN DEFINITIONS
(J13 - EXPANSION RAM BD.)

01	IB01	02	IB00
03	IB02	04	IB04
05	IB03	06	IB05
07	IB07	08	IB06
09	DIPL	10	DOPL
11	NO CONNECTION	12	DMEMA06
13	NO CONNECTION	14	DMEMA03
15	DMEMA00	16	DMEMA04
17	DMEMA02	18	DMEMA05
19	DMEMA01	20	DMEMA07
21	GND	22	CASU*
23	GND	24	GND
25	+5 VOLTS	26	+5 VOLTS
27	+5 VOLTS	28	RAS1*
29	WR1*	30	CASL*
31	DOPU	32	DIPU
33	IB12	34	IB15
35	IB11	36	IB14
37	IB10	38	IB08
39	IB09	40	IB13

OPTION CARD CONNECTOR PIN ASSIGNMENTS
(96-PIN EUROCONNECTOR)

01a	+5 VOLTS	01b	+5 VOLTS	01c	+5 VOLTS
02a	GND	02b	AGVID	02c	+5 VOLTS
03a	GND	03b	GND	03c	GND
04a	BUSBLANK	04b	G/A	04c	BUSDOTCLK
05a	BUSCLK	05b	BUSHSYNC	05c	BUSVSYNC
06a	NMI*	06b	GND	06c	AINT
07a	BUSVLT	07b	+12 VOLTS	07c	-12 VOLTS
08a	BUSPCLK	08b	BUSINT03	08c	BUSPCS5*
09a	BUSRFSH*	09b	BUSINT16	09c	BUSPCS4*
10a	BUSIOR*	10b	HDCINT06	10c	BUSPCS3*
11a	BUSHLDA*	11b	RATINT12	11c	BUSLOCK*
12a	BUSBHE*	12b	BUSIOW*	12c	BUSDMARQ1*
13a	BUSMCS1*	13b	BUSMCS0*	13c	BUSDMARQ2*
14a	BUSMR*	14b	BUSMW*	14c	BUSARDY*
15a	BUSRFINH*	15b	BUSL/E*	15c	BUSINT05
16a	BUSMRST*	16b	BUSDEN*	16c	BUSINT07
17a	BUSDT/R*	17b	BUSDMACK3*	17c	BUSINT17
18a	BUSDMACK2*	18b	MEMINT15	18c	BUSDMACK1*
19a	BUSALE	19b	BUSHOLD*	19c	BUSDMARQ3*
20a	GND	20b	GND	20c	GND
21a	BUSD04	21b	BUSD05	21c	BUSD03
22a	BUSD06	22b	BUSD07	22c	BUSD15
23a	BUSD00	23b	BUSD01	23c	BUSD02
24a	BUSD14	24b	BUSD10	24c	BUSD11
25a	BUSD13	25b	BUSD09	25c	BUSD12
26a	BUSD08	26b	BUSA04	26c	BUSA00
27a	BUSA11	27b	BUSA12	27c	BUSA07
28a	BUSA18	28b	BUSA17	28c	BUSA15
29a	BUSA19	29b	BUSA13	29c	BUSA14
30a	BUSA08	30b	BUSA09	30c	BUSA01
31a	BUSA10	31b	BUSA03	31c	BUSA02
32a	BUSA16	32b	BUSA06	32c	BUSA05

MOUSE INTERFACE
(9-PIN "D" TYPE, FEMALE RT. ANGLE)

01	GROUND	02	+5 VOLTS
03	S3*	04	XA
05	XB	06	S2*
07	S1*	08	YA
09	YB		

COLOR MONITOR PIN ASSIGNMENT
(GRAPHICS BD.)

1	GROUND
2	GROUND
3	RED
4	GREEN
5	BLUE
6	INTENSITY
7	NO CONNECTION
8	HSYNC
9	VSYNC

6/ Troubleshooting Procedures

6.1 Power Supply

General diagnostics can be performed on the power supply without removing it from the chassis.

To check the power supply for correct outputs to the logic board and floppy disk, simply remove the top cover of the main unit and disconnect the power connector (P30) from the top floppy disk drive. Check for +12 Vdc (pin 1) and +5 Vdc (pin 4). If these voltages are present, replace the plug and remove the power connector (P10) from the main logic board. Check for +12 Vdc (pin 1), -12 Vdc (pin 7), and +5 Vdc (pins 3 and 4).

CAUTION

DO NOT DISCONNECT BOTH PLUGS at the same time. To function properly, the power supply must have a minimum load.

If any of the voltages do not conform to the specifications contained in Paragraph 7.2.1.1, the power supply and/or harness may be defective. Remove the power supply and troubleshoot using Paragraph 7.2.1.2.

For troubleshooting the power supply assembly, see Section 7.5.4.

6.2 Other Components

If all voltages are present as described in Paragraph 6.1 and the unit is still inoperative, replace first the RAM board and then the CPU to correct the problem. Refer to Paragraph 7.5.2 for a theory of operation on the RAM boards and 7.1.2 for the CPU theory.

7/ Theory of Operation

This section of the manual contains an explanation of the components used in the Model 2000 Microcomputer. It includes a discussion of the Main Logic Board, Power Supply Board(s), and optional boards. The discussions on the Main Logic Board are related to the overall block diagram shown in Figure 7.1. Each subsection contains a simplified block diagram, referenced to a specific page of schematic . The complete schematic of the Main Logic Board is located at the end of Section 7.1. The Power Supply used in the Model 2000 is described in Paragraph 7.2, as well as the supply required for the addition of a Hard Disk Drive Assembly. The Disk Drive Assembly description is contained in Paragraph 7.3. Information concerning the Card Cage Assembly and Motherboard is contained in Paragraph 7.4.

Discussion of optional features, such as 128K Add-On Memory, B/W Graphics Board, Color Graphics Option, Color Monitor, TV/Joystick Board, and Mouse/Clock Board is contained in the manual covering the specific option.

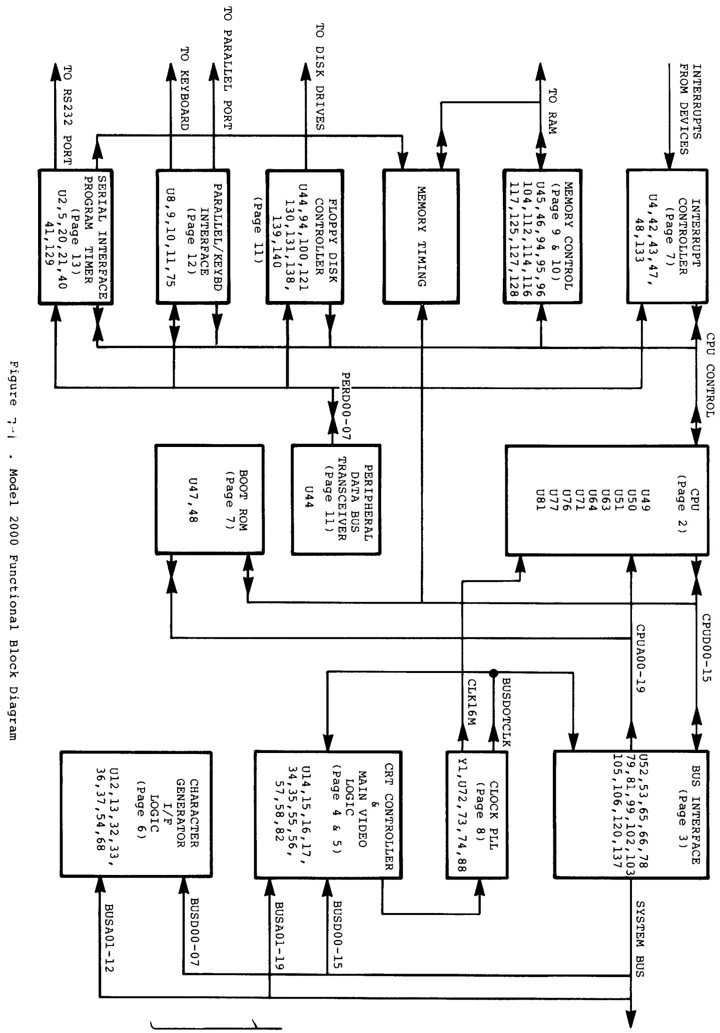


Figure 7.1 Model 2000 Functional Block Diagram

7.1 Main Logic Board

7.1.1 General

The Main Logic Board is mounted to the underside of the Main Unit and is accessible from the underside. It is mounted to a pan assembly which provides protection and support for the board which is approximately 10" x 16". It contains connectors which allow it to be interconnected to the power supply, disk drives, reset circuitry, and motherboard assembly for optional boards.

See Section 3 for disassembly procedures for the Main Logic Board.

7.1.2 CPU (Sheet 2)

The CPU (Central Processing Unit) revolves around an Intel 80186 microprocessory chip with a clock input of 16 MHz (this yields a 125 nsec machine cycle or "T" state). It is assumed that the reader is familiar with 80186 timing and interfacing. For more information, refer to Intel literature. The CPU section includes logic to buffer and latch all data and address signals. All chip selects (except the boot ROM and character generator) are generated by this section also. A "fail safe" memory timeout circuit prevents the 80186 from waiting forever for a non-existent memory or port address to respond. A programmable DMA (Direct Memory Access) multiplexer maps four bus DMA channels into the two channels resident on the 80186. Logic that directs the bus controller to point the system buses in the right direction is contained here also.

7.1.2.1 CPU Buffering

The Intel 80186 uses a multiplexed address-data bus. The bus is demultiplexed using 74SL373 8-bit transparent latches and 74LS245 octal bi-directional bus drivers. The 74LS373 is enabled for output by CPUHLDA (CPU HoLD Acknowledge, active high) so that it may drive the address bus while the 80186 has the control of the system. The latches are controlled by CPUALE (CPU Address Latch Enable, active high). The falling edge of CPUALE locks the data into the latches for the entire memory cycle. A16 - A19 are not multiplexed with data but require latching as do S0* - S2* (Processor Status bits 0 - 2).

The data buffers are controlled by 80186 generated signals DEN* (Data ENable, active low) and DT/R* (Data Transmit/Receive, high for write cycles, low for read cycles). Within the first T state, DT/R* is set to point the data buffers in the right direction, and DEN* goes low when data appears on the bus.

7.1.2.2 CPU Address Decoding

Address decoding falls into two categories: memory and peripheral. Each is identified by unique read and write status codes on S0* - S2*. The 80186 is software programmable to generate select signals to both spaces. The Model 2000 will always be programmed as shown in Figure 1.

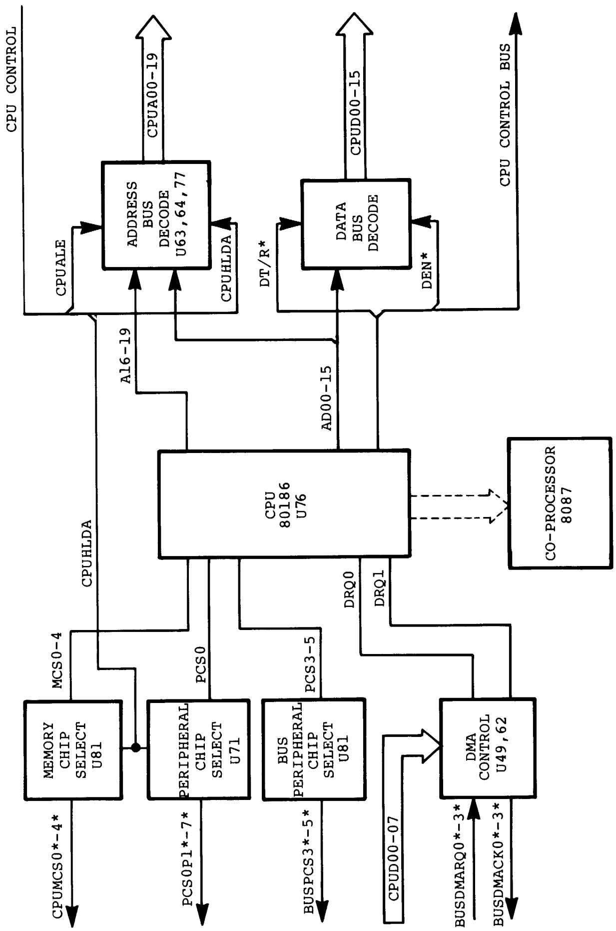


Figure 7-1. CPU Block Diagram

Signal	Memory/Peripheral	Address Range
LCS*	M	Not Used
MCS0*	M	00000H - 1FFFFH
MCS1*	M	20000H - 3FFFFH
MCS2*	M	40000H - 5FFFFH
(not used)		
MCS3*	M	60000H - 7FFFFH
(not used)		
UCS*	M	F8000H -FFFFFH
PCS0*	P	0000H - 007FH
PCS1*	P	0080H - 00FFH
PCS2*	P	0100H - 017FH
PCS3*	P	0180H - 01FFH
PCS4*	P	0200H - 027FH
PCS5*	P	0280H - 02FFH
PCS6*	P	0300H - 037FH
(not used)		

NOTE:

MCSn* address areas are programmed to insert 0 wait states and use 80186 ready inputs. The UCS* address area is programmed to insert 3 wait states and ignore 80186 ready inputs. All PCSn* areas are programmed to insert 2 wait states and ignore 80186 ready inputs.

Figure 7-2. 80186 Programmed Chip Selects

Most internal peripherals are mapped into PCS0* space. This space is split into eight 16-byte active low chip selects by a 74LS138. Both PCS0* and CPUALE condition the 74LS138 to guarantee the subsequent chip selects are valid only when all address bits are stable. The first block of 16 addresses is further broken into four 2-byte blocks (mirrored twice) by 1/2 of a 74LS139. Address assignments are given in Figure 7-4.

Address	Name	Device
0000H - 0001H	PCS0P0A*	Speaker/clocks control
0002H - 0003H	PCS0P0B*	DMA Multiplexer control
0004H - 0005H	FLDTC*	Floppy Disk Term. Count
0006H - 0007H	------	Unused (no connect)
0010H - 001F	PCS0P1	8251A
0020H - 002FH	PCS0P2	Unused (no connect)
0030H - 003FH	PCS0P3	8272A
0040H - 004FH	PCS0P4	8253-5
0050H - 005FH	PCS0P5	8255A-5
0060H - 006FH	PCS0P6	8259A (Controller 0)
0070H - 007FH	PCS0P7	8259A (Controller 1)

Figure 7-3. Peripheral Chip Select 0 Address Assignments

Four DMA acknowledge channels are generated at a base address of 0080H in CPU peripheral address space (See Figure 3). Each one is thrity-two bytes in length. BUSDMACK0* (BUS DMA ACKnowledge 0, active low) is dedicated to the internal floppy disk controller and BUSDMACK3* is dedicated to the internal hard disk. BUSDMACK1* - BUSDMACK3* are routed to the expansion bus connector.

Address	Name	Device
0080H - 009FH	BUSDMACK0*	Internal Floppy Disk Controller
00A0H - 00BFH	BUSDMACK1*	No assignment
00C0H - 00DFH	BUSDMACK2*	No assignment
00E0H - 00FFH	BUSDMACK3*	Hard Disk Controller

Figure 7-4. DMA Acknowledge Address Assignments

An additional level of decoding is required to support the Model 2000 bus structure. The CPUL/E* (CPU Local/External, high for local, low for external) is generated by a 74LS30 8-input NAND gate. The decoded chip selects for CPUMCS0*, CPUMCS1*, PCS0*, BOOT*, and BUSDMACK0* as well as INTAK* and TMOINT01* constitute local addresses. All other addresses are external.

7.1.2.3 Synchronous and Asynchronous Ready

Addressed memory and peripherals handshake with the CPU indicates that a transaction is complete by pulling CPUARDY* (CPU Asynchronous ReaDY, active low wire OR bus) low. Devices not required to handshake in this manner are those which are selected by a memory or peripheral chip select that ignores external ready inputs (See Figure 7.1), with the exceptions being the boot ROM and any interrupt acknowledge cycle (see next paragraph). CPURDY* is then inverted and connected to the ARDY (Asynchronous ReaDY, active high) input on the CPU. Once synchronized inside the CPU, ARDY is ORed with the SRDY (Synchronous ReaDY, active high) so that if either input is a logic "1", the CPU will assume that the addressed device is ready to complete the transaction.

The SRDY input to the CPU is handled differently. When the CPU is reset, UCS* (Upper memory Chip Select, active low from which the boot ROM chip select is generated) will have three wait states inserted automatically and will include external ready inputs. Because no logic provision was included for a UCS* addressed device to respond to the CPUARDY* bus, the CPU will wait indefinitely. A corresponding situation exists for INTAK* (INTerrupt AcKnowledge, active low). To overcome this, UCS* and INTAK* are logically ORed together to generate an active high signal whenever either input is active low. This signal is routed directly to the CPU SRDY input as well as to a 74LS74 which synchronizes it to the CPU clock for use with a co-processor.

7.1.2.4 Memory Timeout

A safeguard circuit is included to prevent the CPU from waiting an excessive amount of time for memory to respond with a ready. Revolving around a 74LS123 timer set for approximately 100 usec, the circuit begins timing a transaction at the leading edge of CPUALE. This forces the timer's Q output to a logical "1". The Q output is gated with CPUDEN* to form TMOINT01 (TiMeOut INTerrupt controller 0, level 1, active high) which goes active only if the timer times out while a transaction is still in progress (signaled by CPUDEN* remaining active low). TMOINT01 is inverted by an open collector gate and output in the correct sense to the CPUARDY* bus and remains low until CPUDEN* goes inactive, indicating that the CPU acknowledges the handshake. Concurrent with this operation, CPUL/E* is forced to the local state (logic "1") so that the bus drivers are forced inactive. This action prevents a contention on the CPUARDY* bus. If the transaction completes before a timeout, the time will continue until it is restarted by another CPUALE or until it times out. (The system will not see this timeout because CPUDEN* is inactive.)

7.1.2.5 Four Channel DMA Multiplexer

The Model 2000 has provisions for multiplexing four BUSDMARQn* (BUS Direct Memory Access ReQuest n, active low) into the two 80186 resident DMA channels, DRQn (DMA ReQuest n, active high). An 8-bit write only register, located at 0002H in CPU peripheral address space, controls the multiplexing process (bit assignments are given in Figure 4). This register is cleared after a system reset. Each input channel has both an enable bit (to enable the corresponding channel for requests), and a select bit (to select the 80186 channel to which the incoming request is routed). The DMEINT16 (DMA Error INTerrupt controller 1, level 6, active high) signal is used to indicate to software that an invalid programming condition has occured (more than two enabled channels routed to the same 80186 channel). DMEINT16 will remain active until the error condition is removed. DRQn are forces low while INTAK* is active low due to a logic error in early versions of the 80186.

7	6	5	4	3	2	1	0
Chan 3 select	Chan 2 select	Chan 1 select	Chan 0 select	Chan 3 enable	Chan 2 enable	Chan 1 enable	Chan 0 enable

For select bits: 0 for DRQ0
1 for DRQ1

For enable bits: 0 for disable
1 for enable

Figure 7-5. DMA Channel Control Register (Port 0002H)

7.1.3 Bus Interface (Sheet 3)

The Model 2000 uses a unique high performance split-bus architecture. The CPU (Central Processing Unit), base peripherals (floppy disk interface, RS232 interface, and printer/keyboard interface), and the first 256K RAM reside on the local bus while the monochrome and color video systems, as well as any additional memory, are on the external bus. These buses remain independent until a device initiates a transaction that crosses the boundaries.

7.1.3.1 Bus Signal Description

BUSAnn	I/O	20 bit bidirectional address bus (BUSA00 is the least significant bit, BUSA19 is the most significant bit). 220/330 ohm split termination.
BUSDnn	I/O	16 bit bidirectional data bus (BUSD00 is the least significant bit, BUSD19 is the most significant bit). 220/330 ohm split termination.
BUSMCS0*	I/O	BUS Memory Chip Select 0, active low. Selects RAM (on main logic board) in the address reange 00000H - 1FFFFH. 2.2 kohm pullup.
BUSMCS0*	I/O	BUS Memory Chip Select 0, active low. Selects RAM (on main logic board) in the address range 00000H - 1FFFFH. 2.2 kohm pullup.
BUSINT03	I	BUS INTerrupt controller 0, level 3, rising edge sensitive. 2.2 kohm pullup.
BUSINT05	I	BUS INTerrupt controller 0, level 5, rising edge sensitive. 2.2 kohm pullup.
HDCINT06	I	Hard Disk Controller INTerrupt controller 0, level 6, rising edge sensitive. 2.2 kohm pullup.
BUSINT07	I	BUS INTerrupt controller 0, level 7, rising edge sensitive. 2.2 kohm pullup.
RATINT12	I	Mouse Controller INTerrupt controller 1, level 2, rising edge sensitive. 2.2 kohm pullup.

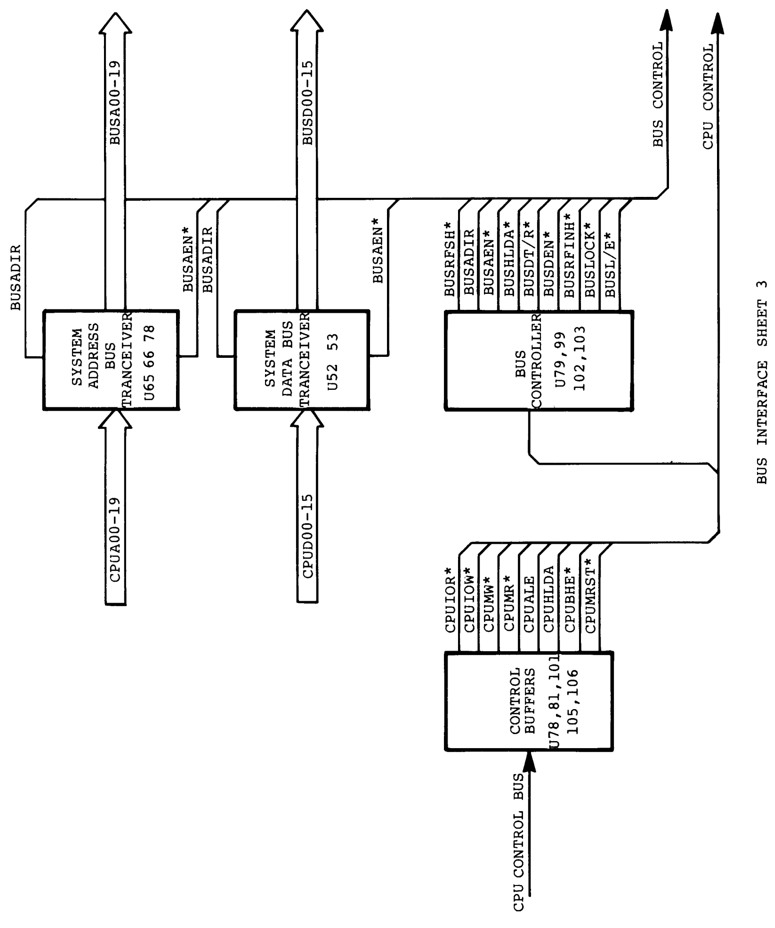


Figure 7-6. Bus Interface Block Diagram

MEMINT15	I	MEMory INTerrupt controller 1, level 5, rising edge sensitive. 2.2 kohm pullup. Open collector bus.
BUSINT16	I	BUS INTerrupt controller 1, level 6, rising edge sensitive. 2.2 kohm pullup.
BUSINT17	I	BUS INTerrupt controller 1, level 7, rising edge sensitive. 2.2 kohm pullup.
BUSNMI*	I	BUS Non-Maskable Interrupt, active low. 2.2 kohm pullup. Open collector bus.
BUSDMARQn*	I	BUS Direct Memory Access ReQuest n (1 - 3), active low. 2.2 kohm pullup.
BUSDMACKn*	I	BUS Direct Memory Access ACKnowledge n (1 - 3), active low. 2.2 kohm pullup.
BUSMR*	I/O	BUS Memory Read, active low. 220/330 ohm split termination.
BUSMW*	I/O	BUS Memory Write, active low. 220/330 ohm split termination.
BUSIOR*	I/O	BUS I/O Read, active low. This line may not be driven by an external master. 220/330 ohm split termination.
BUSIOW*	I/O	I/O Memory Write, active low. This line may not be driven by an external master. 220/330 ohm split termination.
BUSMRST*	O	BUS Master ReSeT, active low. Indicates that the CPU is in a reset state. This signal is never tri-stated. 2.2 kohm pullup.
BUSALE	O	BUS Address Latch Enable, active high. When active, bus addresses are unstable. Addresses may be latched at the falling edge of BUSALE. This signal is never tri-stated. 2.2 kohm pullup.
BUSDT/R*	I/O	BUS Data Transmit/Receive, high for transmit, low for receive. This signal indicates the direction that data will flow across the bus. 220/330 ohm split termination.

BUSDEN*	I/O	BUS Data ENable, active low. When active, this signal enables the bus data buffers. 220/330 ohm split termination.
BUSHOLD*	I	BUSH HOLD, active low. This line is pulled low by a bus master when the system bus is required for a transaction. Open collector bus. 2.2 kohm pullup.
BUSHLDA*	O	BUS HoLD Acknowledge, active low. This line is driven low when the bus controller honors the bus request on BUSHOLD*. 2.2 kohm pullup.
BUSLOCK*	I	BUS LOCK, active low. Signals the bus controller that a locked transaction is in progress on the bus and may not be disturbed by another device. 2.2 kohm pullup.
BUSBHE*	I/O	BUS Bus High Enable, active low. This signal enables the high byte (BUSD08 - BUSD15) for access. 220/330 ohm split termination.
BUSL/E*	I	BUS Local/External, high for local, low for external. This signal informs the bus controller if memory on the main logic board (local), or expansion memory is requested for an external master. 2.2 kohm pullup.
BUSARDY*	I/O	BUS Asynchronous ReaDY, active low. When a device is ready to complete a transaction, it will pull this line low. This line is always pointing in the opposite direction from the address lines, so that an external master may communicate with internal memory. Open collector bus. 220/330 ohm split termination.
BUSRFSH*	O	BUS ReFreSH, active low. This signal is the logical OR of CPUMR or CPUMW to indicate to a memory refresh controller that a hidden refresh may occur. THis signal is never tri-stated. 2.2 kohm pullup.

BUSRFINH*	O	BUS ReFresh INHibit, active low. This signal indicates that the current bus master has a fixed memory access time and will not insert wait states so refresh cycles should be inhibited. Never tri-stated. 220/330 ohm split termination.
BUSPCLK	O	BUS Processor CLocK. Buffered CLKOUT from the CPU. May be used for synchronization with the CPU. This signal is never tri-stated. 2.2 kohm pullup.
		THE FOLLOWING SIGNALS ARE CONNECTED TO THE BOTTOM EXPANSION CONNECTOR ONLY
BUSDOTCLK	O	BUS DOT CLocK. The system dot clock either 22.387290 MHz or 27.984113 MHz, depending on the monochrome video mode selected. No termination.
BUSVSYNC	O	BUS Vertical SYNChronization, active low. When active, this signal indicates a vertical synchronization interval. No termination.
BUSHSYNC	O	BUS Horizontal SYNChronization, active low. When active, this signal indicates a horizontal synchronization interval. No termination.
BUSBLANK	O	BUS BLANK, active high. When active, this signal indicates that the video beam is blanked. No termination.
AINT	I/O	Alphanumeric video INTensity. This bit reflects the intensity of the video beam on the monochrome monitor outlet (high for full intensity, low for partial intensity). No termination.
AGVID	I/O	Alphanumeric/Graphic video data. This bit reflects the state of the video on the monochrome monitor outlet (high for on, low for off). No termination.

G/A*	I	Graphic/Alphanumeric. This bit describes the source of the data that appears on the AGVID/AINT buses. If high, video from the high resolution option card will appear on the bus; if low, video from the monochrome sub-system will appear. Pulled up by 2.2 kohm resistor on the main logic board.
BUSVLT	O	BUS Visible Line Time, active high. When active, this signal indicates that the video beam may be visible. No termination.

7.1.3.2 Bus Controller

The bus controller logic is contained in two PAL (Programmable Array Logic) devices. An eight-bit synchronizing latch, clocked by BUSDOTCLK, is used to force changes in state of all signals to occur synchronously. The first PAL (U103, a 16L8) decodes the present bus state and outputs a bus state code on outputs X0* - X4*. It also directly controls BUSADIR and BUSAEN* based on the control inputs. The current bus state also indicates whether the CPU must be halted to honor the bus request, so HOLD is also output by U103.

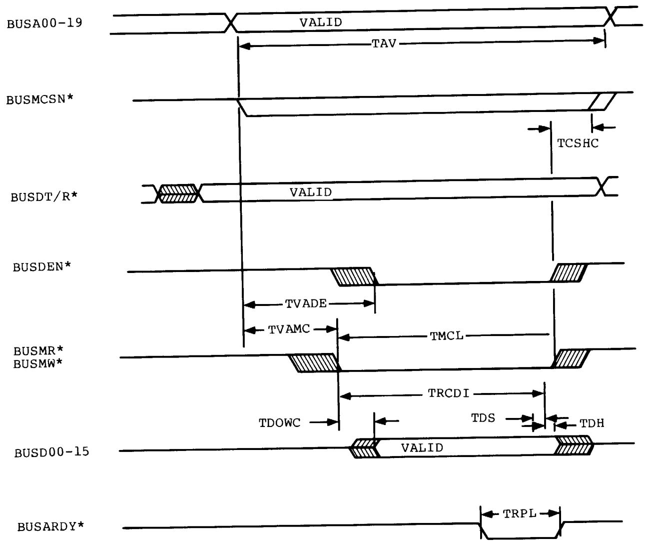
The second half of the bus controller (U102, also a 16L8) decodes the bus state code and asserts the proper control on the bus. It acknowledges all hold requests and asserts BUSRFINH* when necessary. It also maintains control over BUSDEN* and BUSDT/R*. If the bus is granted to an external master, these lines are tri-stated so that the master may direct the data as necessary.

All requests are arbitrated in conjunction with the requester's L/E* signal to determine the extent of action taken. The 80186 has the lowest priority followed by the external bus master. The monochrome video controller has the highest priority. If an external master requests the local bus (as indicated by the associated L/E* being driven high), the CPU is put in a HOLD state and all buses are given to the requester. As long as the CPU does not request the external bus, transactions may occur on that bus without halting the CPU. If an external transaction is in progress and the CPU requests the external bus, it will wait (by virtue of CPUARDY* being high) until the transaction is complete. It is highly recommended that transactions take less than 100 usec because the memory timeout circuit will abort the transaction. All external master devices are expected to drive all tri-stated I/O signals listed in the previous section or be satisfied with the default condition.

The latched status code signals (LS0* - LS2*) are decoded by a 74F138. Two signals enable the decoder: CPUALE and CPUHLDA. The latched status bits are not guaranteed to be stable until CPUALE falling edge and while the CPU is in a hold state, the status bits indicate a passive state (all 1s) and may be disregarded. The read and write signals (MR*, MRF*, MW*, IOR*, and IOW*) are further conditioned by RD* and WR* as necessary to generate read and write signals with the correct timing.

7.1.3.3 Bus Timing Parameters

Symbol	Parameter	Min	Max	Unit	Comments
t_{VAMC}	Valid address to memory command	20		ns	
t_{AV}	Address valid length	415		ns	Assuming no wait states
t_{VADE}	Valid address to data enable	130	190	ns	
t_{MCL}	Memory command pulse width (read or write)	190		ns	Assuming no wait states
t_{RCDI}	Memory read command to data in	175		ns	Assuming no wait states
t_{DS}	Data setup before data in	20		ns	
t_{DH}	Data hold after data in	10		ns	
t_{DOWC}	Data valid after write command	15	200	ns	
t_{RPL}	BUSARDY* pulse length	125		ns	To generate recognition
t_{CSHC}	Chip select hold after command	35		ns	
t_{BACA}	BUSHLDA* active to address and control driven by requestor	500		ns	
t_{CIBI}	Control inactive before BUSHOLD* inactive	20		ns	



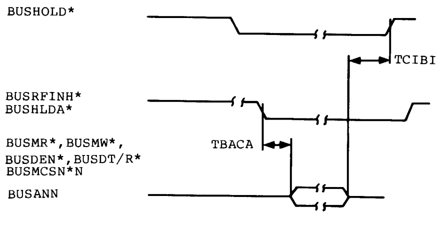


Figure 7-7. Timing Parameter Diagram

7.1.4/ VIDEO SYSTEM (Pages 4 & 5)

The Standard Microsystems Corporation CRT9XXX chip set constitutes the major components of the monochrome video sub-system. Specifically, the CRT9007 Video Processor and Controller (VPAC) is at the center of the system. It generates all video character-related timing such as horizontal sync, vertical sync, composite blank, etc. It also generates memory addresses so that the two CRT9212 Double Row Buffers (DRB) may latch character and attribute data. Attribute data is presented directly to the CRT9021 Video Attribute Generator in the format given below, while the character itself is latched and presented one CCLK* (Character Clock - 357 nsec) later to the RAM-based character generator. The attributes are delayed within the CRT9021 by two CCLK*s so that the character dots from the character generator may "catch up".

The VPAC addresses in system memory (as defined by the address control register) are directed toward even bytes. Ihis allows an entire word of character and attribute data to be loaded into the 9212s in a single, word-wide memory cycle. Confusion may arise when referencing the SMC specification, because that document assumes that the CRT9007 is addressing byte-wide memory. Therefore, each entry in the video row table takes four bytes in system memory, with the two bytes associated with that entry located at even addresses. The fourteen-bit address written to the row table entry should be divided by 2 to account for the VPAC addressing offset. The data at the odd addresses is unused. Also, the addresses of the VPAC registers should be multiplied by 2 to get the correct offset into the system peripheral address space.

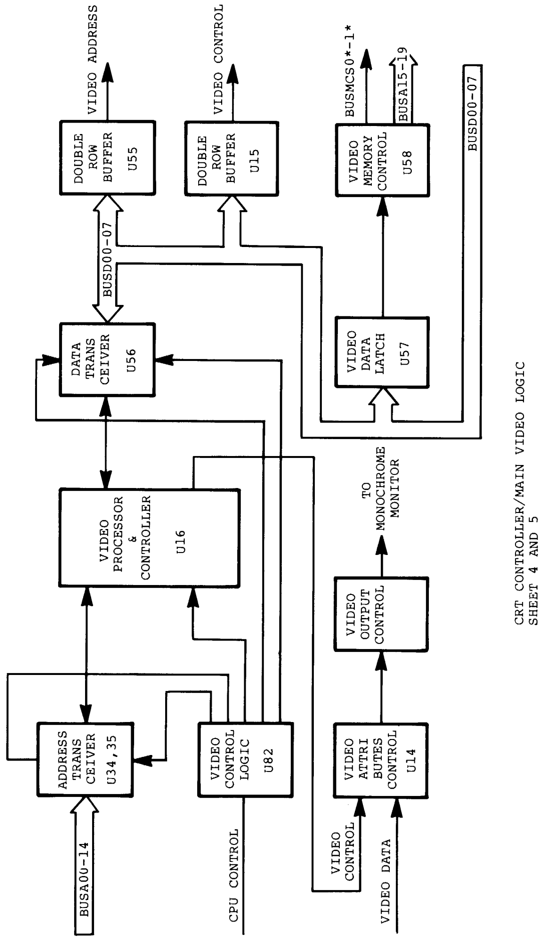


Figure 7-8. CRT Controller/Main Video Logic

7.1.4.1 VIDEO SYSTEM THEORY OF OPERATION

The CPU may access the CRT9007 registers by driving PCS2* active low. A PAL10L8 conditions PCS2* with CPUA00 and CPUDE@* to generate a chip select to the VPAC on even addresses only while data is valid. The PCS2* signal is also conditioned with CPUBHE*, CPUDEN*, and CPUIOW* to generate the ADDLWE* (ADDress Latch Write Enable) signal on odd addresses. Data from CPUD08-CPUD15 is written to the address latch on the rising edge of ADDLWE*, approximately 30 nsec after the rising edge of CPUIOW* (the propagation delay through the PAL10L8). The logic allows writing to both the 9007 and the address control register at the same time.

Data and addresses are buffered through 74F series octal buffers with control signals generated in the PAL10L8. The data buffer, a 74F245, is enabled when either VIDCS* (the VPAC chip select) is active low, or both VIDHOLD and VIDHLDA are active high, indicating a CRT9007 DMA cycle is in progress. When PCS2* is active, the data buffer's direction is controlled by CPUA06. When low, data is transferred from the CPU to the CRT9007; when high, data is transferred from the CRT9007 to the CPU on data lines CPUD00-CPUD07. During a VPAC DMA cycle, the data buffer is enabled with the transfer direction from the data bus to the CRT9007. VA00-VA06 are bidirectional address lines and are buffered through a 74F245 whose enable signal is derived from PCS2* active low or VIDHOLD and VIDHLDA active high. Direction for the 74F245 as well as the 74F244 enable (buffering VA07-VA13) is generated from the HIP (Hold In Progress, active high when VIDHOLD and VIDHLDA are active) signal. Addresses are transferred to the CRT9007 when HIP is low.

All DMA cycle timing is derived from VIDCCLK* (the VIDeo Character CLocK), which in turn is derived from VIDDCLK (the VIDeo Dot CLocK). Bit 6 in the address control register selects how many dot clocks constitute a character clock (hence the number of dots across a character, either 8 or 10).

In the 10 dot-per-character mode, the counter is initialized with a value of 06H. When the counter counts up to a value of 0AH, a "0" is clocked into 1/2 of a 74S74 flip flop on the next rising dot clock edge, forcing the VIDLDSH (VIDeo LoaD/SHift) signal low for use by the CRI9021. The inverted value of the counter's Qc output (delayed by four 74S gate delays to make it coincident with VIDLDSH) is used to generate VIDCCLK*. When a count of 0AH is decoded, a "0" is clocked into the flip flop, forcing VIDLDSH low. Qc rising edge (one state after VIDLDSH goes low) presets the 74S74, forcing VIDLDSH high. When a count of 0FH is reached, the RC* (Ripple Clock) output of the 74LS669 counter goes low, and forces the counter to reload the initial count value on the next clock. The 8 dot-per-character mode is identical except that the counter is loaded with 08H (VIDCCLK* period becomes two states shorter).

Delay logic (in the form of a 6-shift register) delays two of the attribute signals (BLC and BKC) as well as the composite sync signal. The attribute signals need two CCLK delays because the 9021 adds these delays to all attribute inputs except BLC and BKC. The delay of the composite sync signal was required because the 9007 offsets the "real" sync signals (vertical and horizontal sync) from the composite sync signal by two character times. Both the monochrome graphics adapter and the color video adapter require all timing to line up.

During a video DMA cycle, BUSA15 thru BUSA19, BUSMCS0*, and BUSMCS1* are driven to states defined by the address control register (see below) through a 74LS244 driver. BUSA00 and BUSBHE* are driven low through bidirectional drivers in an 82S153 integrated field logic device to enable 16-bit data transfers to the CRT9007 and the CRT9212s. BUSMR* is also driven through a bidirectional driver in the 82S153. Its timing is derived from VIDCCLK* and DLYCCLK* (VIDCCLK* delayed by about 100 nsec) so that CPUMR* goes active low 115 nsec after VIDCCLK* rising edge and stays low until the next VIDCCLK* rising edge.

Scan line data is output by the CRT9007 in a serial fashion with the LSB output first. A 74LS378 is used to convert the data from serial to parallel for use by the character generator. Each bit is output on CCLK* rising edge on SLD (Scan Line Data) as framed by SLG* (Scan Line Gate, active low). The CRT9021 has an on-chip shift register to perform the same function.

A flexible means for transporting video signals from the monochrome system to the color monitor and from the high resolution graphics option board to the monochrome monitor is provided. Two single-bit data buses, AGVID (Alphanumerics/Graphics VIDeo) and AINT (Alphanumerics INTensity) form the bidirectional data path. VIDOUTSEL (VIDeo OUT SELect) controls the monochrome monitor which will display character video or high resolution graphics video (see Address Control Register, below). Both types of video are passed through a 74LS159 multiplexer with VIDOUTSEL acting as the select input. The VIDEOUT and INTOUT outputs from the CRT9021 are also routed to a pair of 74LS125 gates which are enabled by the bus signal G/A* (Graphics/Alphanumerics, high for graphics, low for alphanumerics). When no graphics board is present, this signal is pulled up.

7.1.4.2 ADDRESS CONTROL REGISTER

Note: The following register definition describes production level boards (Rev 3).

Bit 7							Bit 0
VIDOUTS	CLKCNT	CLKSPD	A19	A18	A17	A16	A15

The address control register is a write-only register that appears at all odd bytes in the space shared with the CRT9007 (which is located at all even bytes) in the block mapped into the system peripheral space defined by the CPU signal PCS2*.

A15-A19 The value of these bits is output to the address bus during video DMA cycles to select the 32K byte page of display RAM.

CCKCNT This bit selects which count value is loaded into the video clock generator. When this bit is zero, the clock generator is loaded with a "6" (for 10 dot-per-character normal video), and when high, the counter is loaded with an "8" (for 8 dot-per-character color and graphic video).

CLKSPD This bit selects the dot clock frequency. When it is a "0", 22.4 MHz is selected (normally for 8 dots-per-character), and when it is a "1", 28 MHz is selected (normally for 10 dots-per-character). Note that when either the monochrome graphics adapter or the color graphics adapter is installed, this bit should be set to a "0".

VIDEOUTSel This bit selects the source of video information to be output to the monochrome video connector. When this bit is a "1", video from the onboard video system is output to the monochrome video connector. When this bit is a "0", video from a card in the expansion cage is selected.

7.1.4.3 CHARACTER ATTRIBUTES BYTE

Bit 7							Bit 0
REVID	INT	BLINK	MS1	MS0	BLANK	BKC	BLC

This byte is located on the odd byte of each character word in the character block defined above (bits 0-5 of the address control register).

REVID   This bit, when set, will display the character in reverse video.

INT   This bit, when set, will display the character in full intensity.

BLINK   This bit, when set, will cause the character to blink.

MS1-MS0 These bits are programmed to control character attributes as shown below:

MS1	MS0	Character Attribute Selected
0	0	Wide graphics mode*
1	0	Thin graphics mode*
0	1	Normal character mode
1	1	Normal character mode with underline

*For more information on graphics modes, see CRT9021 specification.

BLANK This bit, when set, will blank the character position.

BLC-BKC These bits are programmed to control cursor attributes as shown below:

BKC	BLC	Cursor Appearance
0	0	Blinking underline cursor
1	0	Blinking reverse video block
0	1	Underline cursor
1	1	Reverse video block

7.1.5 Character Generator (Sheet 6)

As mentioned earlier, the character generator is RAM based. Two uPD4016 2K x 8 static NMOS RAM devices form the 4K byte block. Addresses are supplied by two mutually exclusive sources. During video display, the least significant three bits (CGRA01-CGRA03) from the scan line decoder (the fourth bit CGRA00 is used by the 82S153 to select one of the two RAMs), and 8 latched bits from the CRT9212 connected to the lower data bus form the 11-bit character generator address. During a CPU access to the character generator (indicated by CGRCS* Character Generator RAM Chip Select going active low), these outputs are disabled and buffered CPUA01-CPUA12 are sent to the RAM address bits instead. Because any CPU access takes precedence over a fetch from the video system, it is highly recommended that any access to the character generator (read or write) should wait for a horizontal or vertical retrace when the video is blanked. Objectional "hash" will occur otherwise. The 82S153 selects which RAM will output or receive data as determined by BUSMR* and BUSMW* by pulsing the OE* (Output Enable, active low) or WE* (Write Enable, active low) of the correct RAM device. One RAM is dedicated to odd addresses and the other to even addresses.

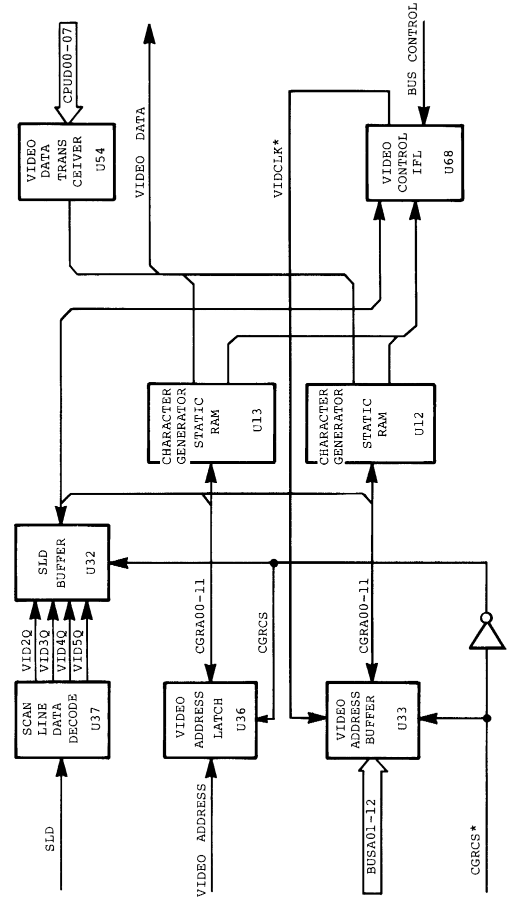


Figure 7-9. Character Generator

7.1.6 Boot ROM/Interrupt Controller (Sheet 7)

7.1.6.1 Boot ROM

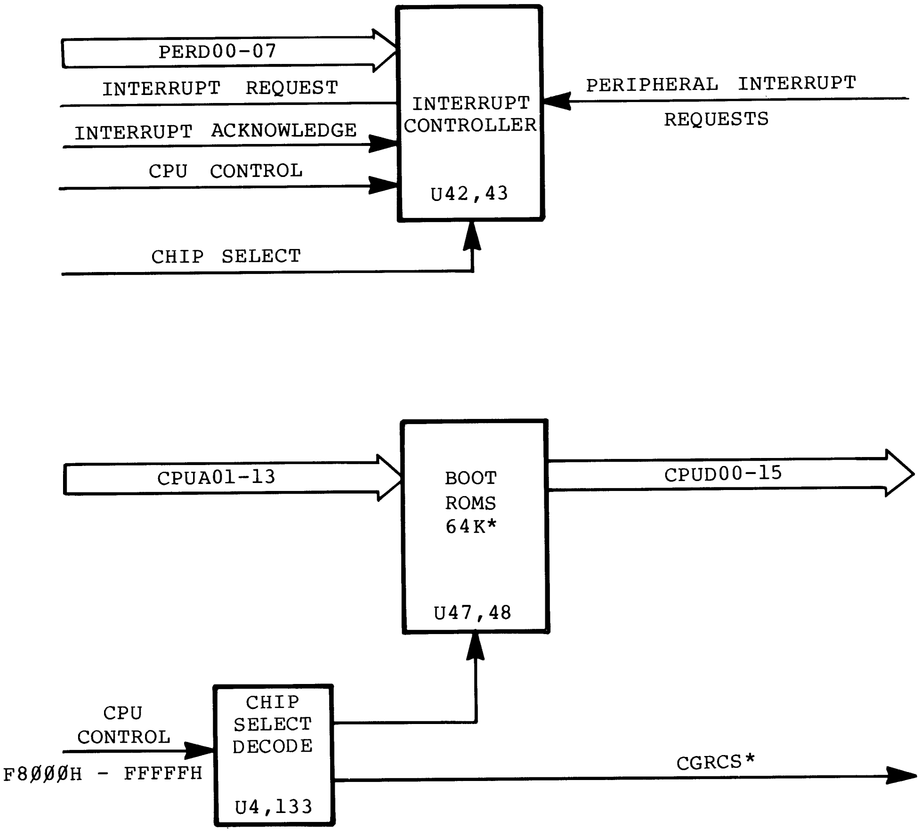
The boot ROM (Read Only Memory) section consists of two ROM devices. Device pinouts must be compatible with the TMS2532 (Texas Instruments). One of the ROMs provides CPUD00 -CPUD07 and the other provides CPUD08 - CPUD15. They respond to all accesses in CPU (Central Processing Unit) memory space from FC000H to FFFFFH. The decode is done in two stages:

1. UCS* (Upper memory Chip Select, active low from F8000H to FFFFFH in CPU memory space) is qualified with CPUALE (CPU Address Latch Enable, active high) to provide a chip select that is valid when all bus address bits are valid.

2. The decoded space is then divided (by CPUA14) into 16K byte spaces so that it may be shared with the character generator.

7.1.6.2 Interrupt Controller

The interrupt controller section consists of two Intel 8259A priority interrupt control devices. They are configured as slave devices to the 80186's internal master interrupt controller (set for cascade mode). Communication with the CPU occurs in one of two forms. The CPU may write commands or check status by accessing the space decoded by PCS0P6* (Peripheral Chip Select 0, Port 6, active low at peripheral addresses 60H to 6FH) for controller 0 or PCS0P7* (Peripheral Chip Select 0, Port 7, active low at peripheral addresses 70H to 7FH) for controller 1. Address assignments for 8259A registers are given in Figure 7-11. All interrupts for the Model 2000 microcomputer are generated on the rising edge of the interrupt input. If the input is high prior to the interrupt, it must go low and remain low for at least 100 nsec to insure recognition. If the interrupt level is unmasked, the interrupt controller will then signal the CPU by activating the INT (INTerrupt output, active high) line. In response, the CPU will pulse either INTA0* or INTA1* (INTerrupt Acknowledge 0 or 1, active low) twice. On the second pulse, the addressed controller is expected to place the vector corresponding to the active interrupt on the preipheral data bus. Interrupt input assignments are given in Figure 7-11. For more information on programming and interfacing with the 8259A, see Intel literature.



INTERRUPT CONTROLLER BOOT ROM
SHEET 7

Figure 7-10. Interrupt Controller/Boot ROM

ADDRESS	READ/WRITE	FUNCTION
0060H	Read	Read OCW2 and OCW3 (Controller 0)
0062H	Read	Read OCW1 (Controller 0)
0060H	Write	Write ICW1 (Controller 0)
0062H	Write	Write ICW2 - ICW4 (Controller 0)
0070H	Read	Read OCW2 and OCW3 (Controller 1)
0072H	Read	Read OCW1 (Controller 1)
0070H	Write	Write ICW1 (Controller 1)
0072H	Write	Write ICW2 - ICW4 (Controller 1)

Figure 7-11. Interrupt Controller Register Assignments

Name	Location		Source	Edge/Level
MEMINT00	8259A	0	Main Logic Board parity error	
TMOINT01	8259A	0	Memory/Peripheral acknowledge timeout	
SERINT02	8259A	0	Onboard Serial transmit/receive interrupt	
BUSINT03	8259A	0	Reserved for second serial channel (on motherboard)	
FLDINT04	8259A	0	Onboard floppy disk controller interrupt	
BUSINT05	8259A	0	Reserved for second floppy disk (on motherboard)	
HDCINT06	8259A	0	Hard disk controller interrupt (on motherboard)	
BUSINT07	8259A	0	Reserved for second hard disk (on motherboard)	
KBDINT10	8259A	1	Keyboard interrupt	
VIDINT11	8259A	1	CRT 9007 interrupt	
RATINT12	8259A	1	Mouse interrupt (on motherboard)	
LPRINT13	8259A	1	Line printer interrupt	
MCPINT14	8259A	1	Onboard math co-processory interrupt	
MEMINT15	8259A	1	Add-on memory parity error (on motherboard)	
DMEINT16	8259A	1	DMA programming error	
BUSINT17	8259A	1	Unused (on motherboard)	

Figure 7-12. Interrupt Controller Input Assignments

7.1.7 Clock/PLL (Sheet 8)

The phase lock loop (PLL) circuit is part of the frequency synthesizer for BUSDOTCLK. The BUSDOTCLK signal must be locked (synchronized) to CLK16M. The frequency of BUSDOTCLK is selectable via CLKSP0 to 28.00 MHz (high res display mode) or 22.40 MHz (normal display mode).

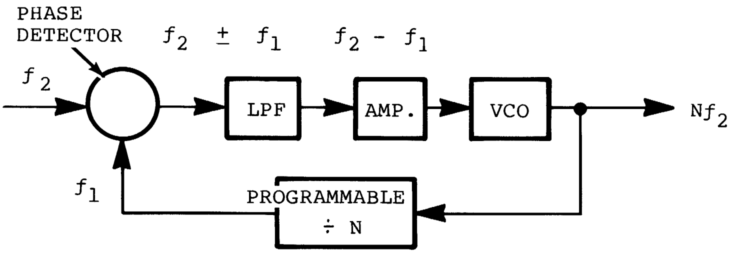


Figure 7-13. Block Diagram

7.1.7.1 General Frequency Synthesis Theory

The block diagram above shows the basic operating principle of the frequency synthesizer. The input frequency is generated by a stable source such as a crystal oscillator. The input frequency f2 is compared at the phase detector whose output consists of f2 ± f1. The low pass filter selects f1 - f2. This signal is amplified and fed to the voltage-controlled oscillator. This drives f1 toward f2 so they lock together, and only a phase difference exists between f1 and f2 which gives sufficient signal to f1 to keep it locked to f2. To vary the output frequency, the value of N is changed in the programmable divider.

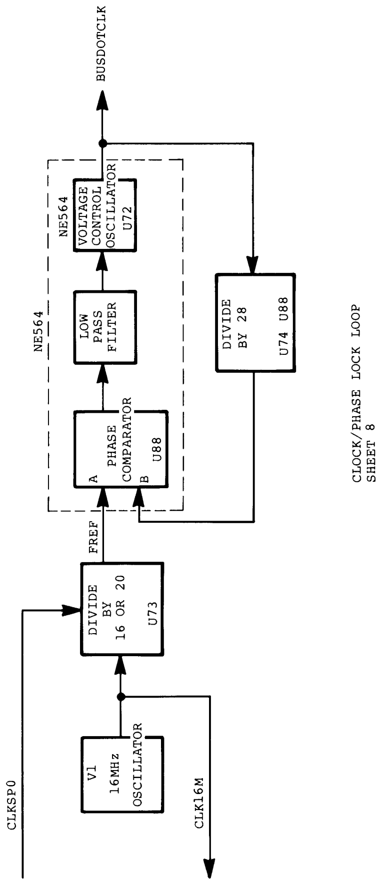


Figure 7-14. Block Diagram Clock/PPL (Sheet 8)

7.1.7.2 Model 2000 PLL Frequency Theory of Operation

The reference frequency f2 is generated by a 16 MHz crystal oscillator (CLK16M) which is divided by either 16 (divide by 8 x 2) or 20 (divide by 10 x 2), depending on the status of CLKSP0. The divide by 2 allows f2 to have a 50% duty cycle into the PLL. This provides reference frequencies of 1.0 MHz and 0.8 MHz respectively for f2. The VCO output frequency fo (BUSDOTCLK) is divided by 28 (divide by 14 x 2) and input to the phase detector (f1). The phase detector will output an error voltage (f2 - f1) to the VCO to lock f1 to f2. Due to the fixed divider in the feedback leg (divide by 28), the VCO output frequency equation becomes:

f0 = 16 MHz x 28/16 or 20

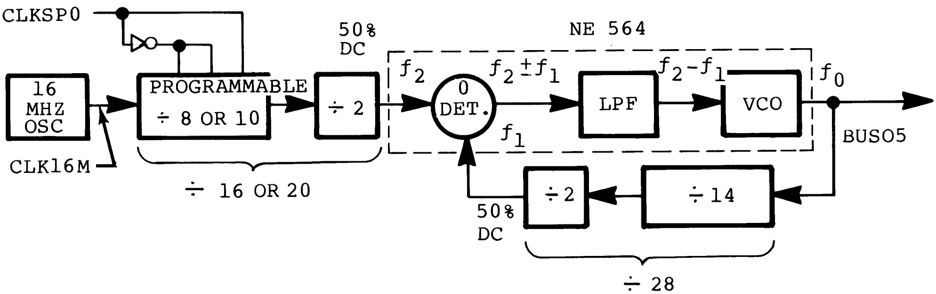


Figure 7-15. Model 2000 PLL Block Diagram

7.1.7.3 Theory of Operation - NE/SE564 Phase Locked Loop

The NE564 is a monolithic phase locked loop with a post detection processor. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to greater than 50 MHz. It is used in the Model 2000 as a modulator with a controllable frequency deviation.

The output voltage of the PLL can be written as shown in the following equation:

$$V_0 = \frac{(f_{in} - f_o)}{K_{vco}}$$

where K_{vco} = conversion gain of the VCO

f_{in} = frequency of the input signal

f_o = free running frequency of VCO

The process of recovering FSK signals involves the conversion of the PLL output into logic compatible signals. For high data rates, a considerable amount of carrier will be present at the output of the PLL due to the wideband nature of the loop filter. To avoid the use of complicated filters, a comparator with hysteresis or Schmitt trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by the above equation varies according to the frequency deviation of f_{in} from f_o. Since this differs from system to system, it is necessary that the hysteresis of the Schmitt trigger be capable of being changed so that it can be optimized for a particular system. This is accomplished in the 564 by varying the voltage at pin 15 which results in a change in the hysteresis of the Schmitt trigger.

For FSK signals, an important factor to be considered is the drift in the free-running frequency of the VCO itself. If this changes due to temperature (according to the equation above), it will lead to a change in the dc levels of the PLL output and consequently to errors in the digital output signal. This is especially true for narrow band signals where the deviation in f_{in} itself may be less than the change in f_o due to temperature. This effect can be eliminated if the dc or average value of the signal is retrieved and used as a reference to the comparator. In this manner, variations in the dc levels of the PLL output do not affect FSK output.

Due to its inherent high frequency performance, an emitter-coupled oscillator is used in the VCO. Variation of the phase detector output voltage changes the frequency of the oscillator. The frequency of the oscillator has a negative temperature coefficient due to the positive temperature coefficient of the monolithic resistor. To compensate for this, a current I_r with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

The phase comparator consists of a double-balanced modulator with a limiter amplifier to improve AM rejection. Schottky-clamped vertical PNPs are used to obtain TTL level inputs. The loop gain can be varied by changing the current at pin 2 which effectively changes the gain of the differential amplifiers.

The free-running frequency of the VCO is shown by the following equation:

$$f_{op} = \frac{1}{25R_c(Cl + C_s)}$$

R_c = 100 ohms

C_1 = external capacitor in farads

C_s = stray capacitance

The loop filter is explained by the following equation:

$$F(s) = \frac{1}{1 + xRC_3}$$

$R = R_{12} = R_{13} = 1.3$ kohm (INTERNAL)

By adding capacitors to pins 4 and 5, two poles are added to the loop transfer function at $w = \frac{1}{RC_3}$

7.1.7.4 Adjustment Procedure

Remove jumper E4-E5 and set R19 for a voltage of 0.0 V at pin 2 of the NE564. Connect a frequency counter to pin 6 of U89 and adjust C64 for an output frequency of 25.2 MHz. Set R19 for a voltage of 1.30 V at pin 2 of the NE564. Replace the E4-E5 jumper and the PLL should lock at either 28.0 MHz or 22.4 MHz, depending on the status of CLKSP0.

7.1.8 Timing and Control Circuits (Pages 9 & 10)

The onboard 256K memory timing and control circuit is designed to be a high performance, zero wait state system. It generates a 280 nsec memory cycle for 64K DRAMs (Dynamic Random Access Memories) as well as refreshing the array and checking parity. It is able to inhibit the refresh logic whenever necessary, and store the "missed" refreshes.

7.1.8.1 Memory Control Overview

The memory control circuit takes the timing signals generated by the timing circuit and generates buffered (and in some cases terminated) control signals. Data in and out as well as addresses are also buffered in this circuit. Parity is generated and checked here also.

7.1.8.2 Memory Timing Circuit

A memory cycle is started by the leading edge of either a CPUMR* (Central Processing Unit Memory Read) or a CPUMW* (CPU Memory Write), framed by either a CPUMCS0* (CPU Middle Chip Select area 0, active in CPU memory space from 00000H to 1FFFFH) or CPUMCS1* (CPU Middle Chip Select area 1, active in CPU memory space from 20000H to 3FFFFH), all active low. This condition is reflected by SMC (Start Memory Cycle) being active low.

The leading edge of SMC starts the memory timing chain. It also clocks a 74S112 flip-flop which generates the leading edge of T00 (all timing taps are active low and are denoted Tnnn where nnn is the time in nsec). When the T00 leading edge propagates through a ten-tap, 40 nsec per tap delay line to T80, the T00 flip-flop is cleared, generating an 80 nsec pulse width for all taps in the chain.

The leading edge of SMC also clocks another 74LS112 which generates RASTAP*. This allows a cycle to start as soon as possible (without waiting for the delay through the delay line and additional logic). RASTAP* is then routed to the control circuit to output RAS* to the correct RAM bank. RASTAP* is cleared by the leading edge of T160 (or master reset) generating a 160 nsec RAS* low time.

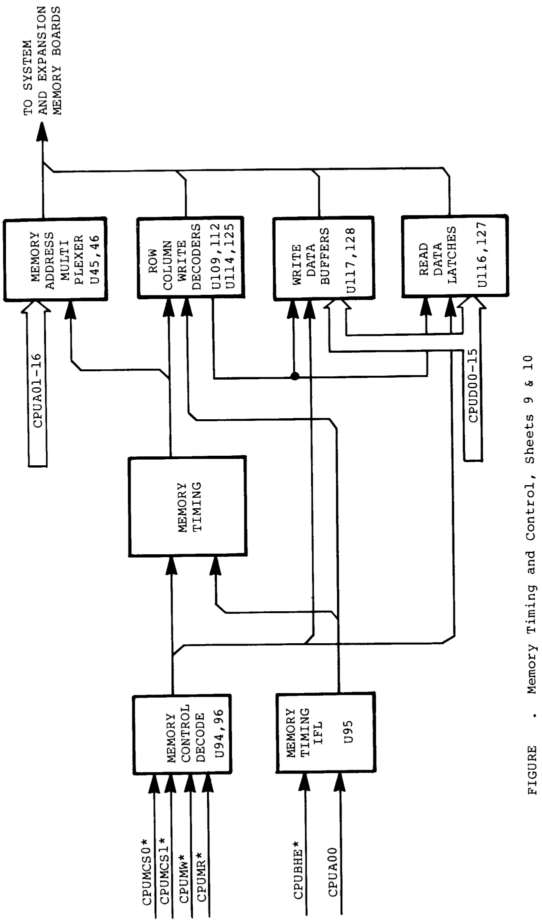


Figure 7-16. Memory Timing and Control

The T40 tap is used to generate both T40AMUX* (T40 Address Multiplex, T40 renamed) and AMUX (Address Multiplex). Both signals are used in memory control address generation. T40AMUX* is delayed by six 74LS04 inverters tied in series (approximately 25 nsec total delay) to generate AMUXDLY* (AMUX Delay, active low). The leading edge of this signal sets a 74S112 to generate CASTAP*. CASTAP* is then routed to the control circuit to output CAS* to the correct RAM bank. The flip-flop is cleared by the leading edge of T200 (or master reset), generating a CAS* pulse of about 135 nsec. The leading edge of T40AMUX* also sets a 74S112 flip-flop to generate WRTAP*. WRTAP* is also routed to memory control to output WR* to the correct RAM bank. It is cleared by T240 (or master reset) to generate a 200 nsec WR* pulse.

An 82S153 IFL (Integrated Field programmable Logic device) is used to generate the correct gating signals for memory control as well as two other miscellaneous signals (ENPARITY, ENable PARITY latch; and BUSRFSH*, the logical OR of CPURD* and CPUWR* to indicate to a bus memory controller slot exists for a hidden refresh). The active conditions for RASEN0*, RASEN1*, CASENL*, and CASENU* are given in Figure

CPUMCS0*	CPUMCS1*	CPUA00	CPUBHE*	RASEN0*	RASEN1*	CASENL*	CASENU*
1	1	X	X	1	1	1	1
X	X	1	1	1	1	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	0

Figure 7-17. RAM ControllerIFL Output Definitions

7.1.8.3 Parity Testing

Parity inputs from memory control, PARU and PARL (PARity Upper and PAR Lower) are ORed together to test for a "1". This signal is then gated with ENPARITY (generated in the IFL, active high which indicates a read from 00000H -3FFFFH). If no parity error exists, a "1" is clocked through a 74LS74 latch during DATALATCH time.

The latch is set to "1" by SMC* to ensure a known state at the start of each memory cycle. The inverted sense output of the latch is buffered through a 74LS38 open-collector buffer to generate MEMINT00 (MEMory INTerrupt controller 0, level 0, active low). The interrupt controller will latch the rising edge to signal the error condition to the CPU.

7.1.8.4 Refresh Control

Refresh cycles are always "tacked" on to the end of a CPU memory access. Memory accesses are stretched by not pulling down on CPUARDY* (CPU Asynchronous ReaDY, active low) until the refresh cycle is finished. If no refresh cycle is required on the current cycle, CPUARDY* is pulled low as soon as the access is decoded to provide a no-wait-state access. The refresh logic is completely disabled during BUSRFINH* (BUS ReFResh INHibit, active low) so that devices accessing memory with fixed access times are not disturbed by the refresh logic.

Refreshes are timed by output 1 of the 8253-5 counter/timer chip (see RS-232 interface document) at a 15 usec interval. Each rising edge of the timer output increments a 74LS193 four-bit binary up/down counter. The count is decoded as non-zero by a 74S260. If the count value is greater than 8, a NMI (Non-Maskable Interrupt) is generated so that the refresh may be serviced before memory is lost.

Before a refresh cycle is run, a memory cycle must be run to arbitrate the refresh request. The refresh cycle is run on the subsequent memory access. At 200 nsec into a non-inhibited memory access (the trailing edge of T120), the state of the refresh count decoder (zero, or non-zero) is clocked into a 74LS74 "D" latch. The latch's output creates both active low and active high senses of RFRQ (ReFresh ReQuest). BUSRFINH* deactivates the latch so that another arbitration cycle must be run after an inhibited cycle. The trailing edge of NCOMCl (active high for either CPUMCS0* or CPUMCSl*) while RFRQ is active clears the MEMRDY (MEMory ReaDY) latch so that CPUARDY* will not be pulled low at the start of the next cycle.

The next non-inhibited memory cycle is run normally until T120 when the latch that drives ENRASCAS* (ENable RAS CAS address buffers, active low) is set, deactivating the signal. The trailing edge of T120 (at 200 nsec) clocks RFRQ* through another 74LS74 latch to create a non-overlapping ENREFAD* (ENable REFresh ADdress buffers, active low). With the proper address buffers activated, a pseudo memory (refresh) cycle may be run. At T280 time, the RRFSH* (Run ReFreSH) goes active low and starts a T00 pulse through the timing chain. So that the refresh cycle is a RAS only cycle, CAS is inhibited by deactivating CASENU* and CASENL* in the 82S153 IFL and totally inhibiting WRTAP*.

The DECRCNT* (DECrement Refresh CouNT, active low) signal performs two functions: (1) it decrements the refresh counter, and (2) it increments the refresh address counters (in the memory control circuit, described below). It goes active at the leading edge of T40AMUX during a refresh cycle. Refreshes continue until a zero refresh count is decoded at the trailing edge of T120. This sets RFRQ inactive. At T240, both ENREFAD* and MEMRDY change states, with ENREFAD* going inactive and MEMRDY going active. MEMRDY active signals the CPU that the cycle is complete. The last operation of a refresh cycle is to set ENRASCAS* active by clocking the inactive state of RFRQ at the leading edge of T280.

7.1.8.5 Memory Control

The DRAM array has a common data in/data out bus. Data into the memory array is buffered by 74LS244 octal buffers enabled by MEMWR* (MEMory WRite, active low during a write to the CPU memory space from 00000H to 3FFFFH) to enable memory data onto the CPU data bus. Data to be output to the CPU data bus is buffered by 74F373 octal latches which hold data valid during extended refresh cycles. The latches are enabled for output by MEMRD* (MEMory ReaD, active low during a read from the CPU memory space from 00000H to 3FFFFH). The latches are clocked by DATALATCH (active low) which is the logical combination of a CAS* to either RAM bank.

Parity is both generated and checked by two 74S280s. On a write operation, data is summed eight bits at a time, an additional "1" is added on the I input, and odd parity is written to the appropriate parity RAM for the selected bank(s). On a read, data is again summed and added to the previously stored parity on the I input. The parity sum plus the active high odd sum bit will always be odd. If even parity is decoded, the error is indicated to the memory timing circuit for reporting to the CPU.

Addresses to the memory array may be from one of two mutually exclusive sources. CPU addresses A01-A16 (CPUA00 is used to select the low eight bits of a word address) are multiplexed through a pair of 74F258 multiplexers. During RAS* time, AMUX is low, and A01-A08 are output to the memory array. When RAS* hold time is satisfied, AMUX switches to a high state and selects A09-A16 to be output. Non-refresh cycles are defined by ENRASCAS* active low, which enables the 74F258s for output. During refresh cycles, ENREFAD* is active low, enabling a 74F244 to output the refresh address (stored by both halves of a 74LS393 counter and incremented by DECRCNT*). All addresses are series terminated by 33 ohm resistors to minimize ringing and overshoot.

A set of discrete F family logic gates is used to generate and buffer control signals for the RAM array. The array is divided into both odd and even byte banks and low and high address banks (at the 128K byte boundary as defined by CPUMCS0* and CPUMCS1*). Both the RAS* and WR* signals follow the address boundaries while CAS* follows the byte boundaries. All control signals are series terminated by 33 ohm resistors to minimize ringing and overshoot.

7.1.9 Floppy Disk Controller (Sheet 11)

The Model 2000 Floppy Disk Controller (FDC) circuitry is located on the Main Logic PCB Assembly (P.N. 889B001). It consists of an Intel 8272 FDC, an FDC9216 Floppy Disk Data Separator (FDDS, write precompensation control logic, drive select logic, and other support logic).

The FDC is capable of controlling two thinline Floppy Disk Drives (FDD) using double-side, double-density 5-1/4" flexible diskettes. This provides a formatted memory capacity of more than 635 kbytes per drive for double-density recording.

7.1.9.1 Data Bus Interface

All peripheral control devices on the Main Logic PCB, with the exception of the Video Control circuitry, communicate with the CPU over a bidirectional 8-bit data bus (PERD00-07). This interface is represented on the FDC schematic (sheet 11 of the Main Logic PCB schematic).

The signal CPUDT/R* controls the direction of data flow to and from the peripheral devices through the DIR input on the octal bus transceiver (74LS245). To prevent data bus contention between peripheral devices, the transceiver is enabled by the logical AND of peripheral chip select PCS0* and CPU DMA acknowledge (BUSDMACK0*) which is then ANDed with DMA interrupt acknowledge (INTAK*).

7.1.9.2 FDC Port Specifications

I/0 mapping of the peripheral devices places the 8272 at Base I/0 port PCS0, port 3, which is the chip select input to the 8272 (PCS0P3*). This signal must be low (positive logic 0) during any read or write operations to the FDC.

There are two registers in the 8272 which are accessible by the CPU -- a Status register and a Data register. The Main Status register is an 8-bit register which contains status information of the FDC that may be accessed at any time. Access to this register is accomplished by a READ instruction to address 0030H. A WRITE instruction to this register is illegal. The Data register is an 8-bit register that stores data, commands, parameters, and FDD status information. It is actually several registers in a stack where only one register is presented to the Peripheral Data Bus at a time. Data is read from or written to this

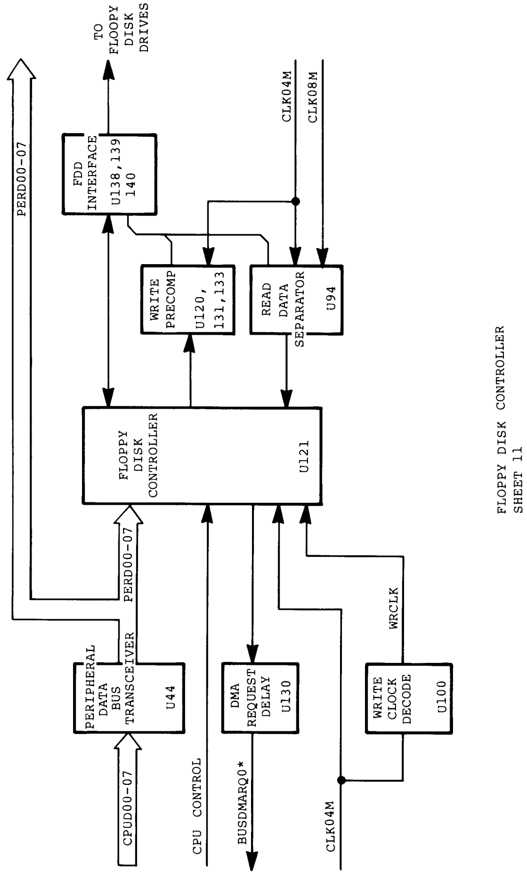


Figure 7-18. Floppy Disk Controller

register by a READ or WRITE instruction to address 0032H to obtain results after executing a command or to program the 8272.

One other operation that is requred is a terminal count strobe (TC). This strobe terminates a DMA transfer or the execution phase of an instruction cycle in programming the 8272. The terminate transfer strobe (FLDTC) is executed by a READ or WRITE instruction to address 0004H.

The following table summarizes this information.

FDC PORT SPECIFICATIONS

Register	Instruction	Address	Bits
Status	RD	0030H	D0-D7
WR	illegal		
Data	RD/WR	0032H	D0-D7
TC	RD/WR	0004H	xx

(xx = don't care)

7.1.9.3 DMA Request and Acknowledge

The 8272 is used in the DMA mode in conjunction with the DMA routing controller IFL (82S153) and the data latch (U49). DMA requests from the FDC (DRQ) are delayed by U130 (74LS74) to satisfy timing constraints before being sent to the DMA routing controller (BUSDMARQ0*). DMA acknowledge is decoded from CPUA05 and CPUA06 through Base I/0 port 1 (PCS1*) by U98 (75LS139, sheet 2 of Main Logic schematic) and output to the FDC (BUSDMACK0*).

7.1.9.4 FDD Read Data Sequence

When the FDC receives the first READ command from the CPU, it selects the drive and issues the head load signal (HDL). A high (logic 1) on HDL activates the motor-on (MTRON) signal to the disk drive. Before any data transfer can begin there must be a delay (approximately 250 msec) to allow the drive motor to reach its operating speed. This delay is accomplished by using the internal head load timer in the 8272 as a motor start-up timer. The HDL signal is also used to activate the activity light on the disk drive (FLDINUSE* if used by Tandon drives only).

Once the FDD has been activated and the 8272 has been placed in the Read Data Mode, the head is positioned at the required track on the diskette. The data is then read from the sector(s) and is presented to the Floppy Disk Data Separator (9216) as a composite serial clock/data stream. If the recording format used is single density, the signal will be an FM (Frequency Modulation) encoded signal. If the recording format used is double-density, the signal will be an MFM (Modified Frequency Modulation) encoded signal. Typical FM and MFM encoded signals are shown in Figures 7-19 and 7-20. The FDDS derives a clock signal from the composite signal and regenerates the clock (DW) and the data (SEPD*) signals.

As data is being transferred between the FDC and the CPU, the FDC must be serviced by the CPU every 54 µsec in the FM mode and every 26 µsec in the MFM mode for 5-1/4" disk drives. The FDC will terminate the Read command if the transfer times are longer than those specified.

When the Read Data command has been terminated, the HDL signal will go low, after the specified Head Unload time has elapsed as determined by the 8272 programming. The falling edge of the HDL starts the motor-on timer (74LS123) which maintains the MTRON signal to the disk drives. This allows the drive motor(s) to continue running for a period of approximately 3 seconds so that subsequent drive accesses may be initiated without having to wait for the motor start-up time. This delay decreases the access time between the FDC and the Disk Drives. This is especially valuable when a diskette is copied from one drive to another.

7.1.9.5 FDD Write Data Sequence

The Write Data sequence is similar to the Read Data sequence in that, when the WRITE command is first issued by the CPU, there is a delay for motor start-up time before the head is positioned at the required track. This delay is not required if the motor is already up to speed when the command is issued which may be determined by reading the motor-on status port located on the Two-Sided media input (TS) of the FDC.

When the head is in position, the FDC takes data from the CPU on a byte-by-byte basis from the Peripheral Data Bus (PERD00-07) and outputs it to the FDD. Data is written into each sector until the Write operation has been completed.

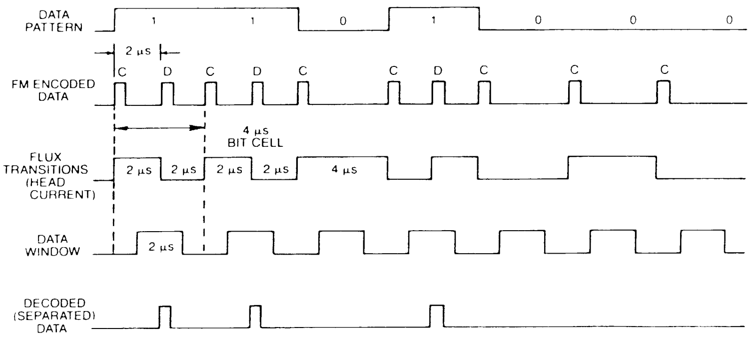


Figure 7-19. FM Encoding Scheme

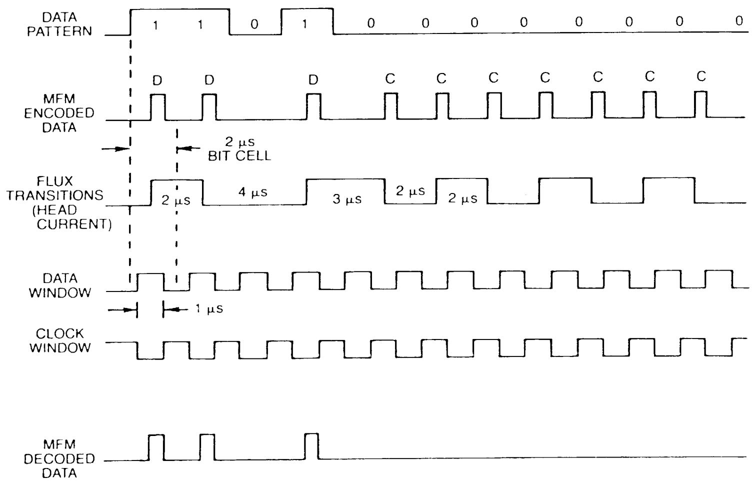


Figure 7-20. MFM Encoding Scheme

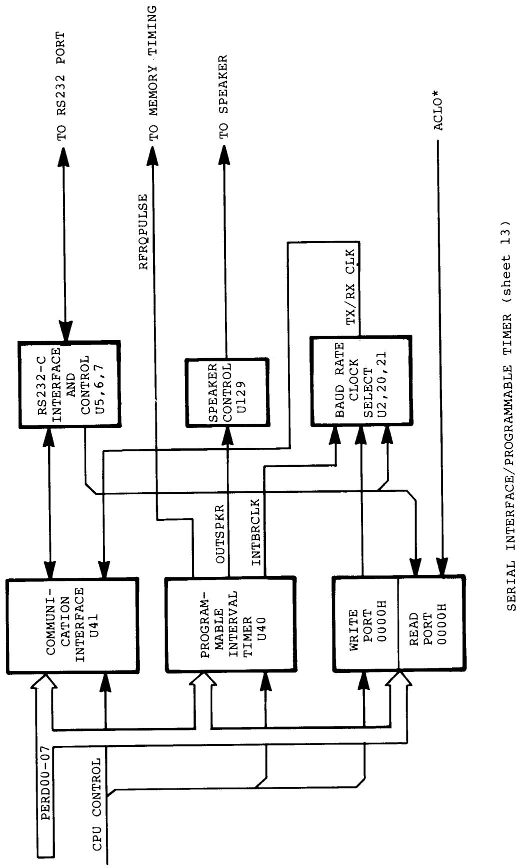


Figure 7-21. Serial Interface/Programmable Timer

Once completed, a Terminal Count (TC) is issued by the CPU and the Write command is terminated. Again, this sequence follows that of the Read DAta sequence by starting the motor-on time when HDL goes inactive (low).

Data transfer rates in the Write Data mode must also meet specific requirements to prevent the 8272 from terminating the command. Data transfers from the CPU to the 8272, when using 5-1/4" disk drives, may not exceed 62 μsec for RM mode or 30 μsec for MFM mode.

When writing data on inner tracks, it is necessary to shift the bit positions so that they appear to be at their nominal positions when reading data from those sectors. This is accomplished by using write precompensation which is a means of causing the flux transitions to be written early or late from their nominal positions. The direction of this shift is determined by the FDC according to the data pattern to be written. Precompensation for Model 2000 FDC is controlled by U131 (74LS195) and U133 (74LS02). The clock rate for write precompensation is selectable depending on the requirements of the disk drives used. The default rate is 250 nanoseconds (jumper E7 to E8) or 125 nanoseconds (jumper E6 to E7), if required.

All read and write operations must have the write clock (WRCLK) input to the 8272 enabled. WRCLK for the Model 2000 FDC is a 1 MHz clock with a 250 nanosecond pulse width generated from the 4 MHz clock (CLK04M) through a 4-bit binary counter (74LS161). This allows the Model 2000 to read single or double density diskettes, but to write only to double density diskettes.

7.1.9.6 FDC/FDD Interface

Requirements for the Floppy Disk Controller to Floppy Disk Drive interface are met by using 7416 open-collector drivers and 74LS14 Schmitt-trigger receivers with terminated inputs. The drive select decoder is a 74LS145 lamp/display driver which has the drive capability required for this interface. FDC connector pin assignments are shown in the Table 7-1.

FDC INTERFACE

CONNECTOR PIN ASSIGNMENTS

Pin Number	Signal Name
2	NC
4	FLDINUSE*
6	NC
8	FLDIDX*
10	FLDDS0*
12	FLDDS1*
14	NC
16	FLDMTRON*
18	FLDDIR*
20	FLDSTP*
22	FLDWRDAT*
24	FLDWE*
26	FLDTRK0*
28	FLDWRPRT*
30	FLDRDDAT*
32	FLDSDSEL*
34	FLDRDY*

NOTE: All odd numbered pins are connected to ground.
NC = No connection.

7.1.9.7 Drive Select Decode

Since the 8272 FDC is an "intelligent" controller, it utilizes a polling mode. This mode is automatically entered between commands and step pulses during the SEEK command, where it monitors the READY lines from all "four" disk drives. Since the Model 2000 is configured with only two drives, it is necessary to decode the drive select so that the motor on timer can time out after the last I/0 operation to the disk drives.

7.1.9.8 READ/WRITE and SEEK Control

During a READ or WRITE operation, the 8272 sets the RS/SEEK output low (logic 0) which enables two receivers on U135 (74LS241). In this mode, the FDC can read the write protect status (WRPRT) of the diskette installed in the drive(s) and the FDD fault status bit. The input of the receiver of the FDD has been tied low to prevent the FDC from seeing a fault condition that would result from a floating input, since the disk drives used do not use the fault line.

When a SEEK command has been issued by the FDC, the RW/SEEK output is set high (logic 1). This enables two drivers and two receivers on the 74LS241. The drivers control the FDD head direction (DIR) and step pulses (STP) which are output to the disk drive(s). The receivers monitor track 0 status (TRK00) and the two-sided media input (TS) to the 8272 which is used as a motor on status port.

7.1.9.9 FDC Reset Control

The reset input to the 8272 is under software control for programming flexibility. A reset is output to the FDC (FDCRST*) by the 74LS273 (sheet 13 of Main Logic schematic) when a WRITE instruction to address 0000H is executed to set to a low state (logic 0) bit 5 of the data byte written.

7.1.10 Parallel/Keyboard Interface (Sheet 12)

The Printer Interface operation depends on the 8255-A Programmable Peripheral Interface for its operation. The 8255-A is mapped at 050H to 05FH in the peripheral address space. It is located at even bytes only, and register mapping is shown in the table below.

Address	R/W	Operation
0050H	R	Port A - > Data Bus
0052H	R	Port B - > Data Bus
0054H	R	Port C - > Data Bus
0056H	R	Illegal Condition
0050H	W	Port A < - Data Bus
0052H	W	Port B < - Data Bus
0054H	W	Port C < - Data Bus
0056H	W	Control < - Data Bus

Table 7-1. Register Mapping

7.1.10.1 Printer Port

For unidirectional printer port operation, Port A and the upper half of Port C are programmed for Mode 1 operation (for more information on 8255A-5 programming, see Intel Microprocessor and Peripheral Handbook, 1983). Port B and the lower half of Port C are programmed as input and output respectively.

To output a byte of data to the printer, the following sequence should occur. After programming the 8255A-5 for the proper operating modes, a "1" should be written to Port C bit 0 to enable the printer bus buffer for output, and a "00" should be written to Port C bits 1 and 2 to enable printer status for output on the Port B data bus (see Table 7-2 for bit assignments). After determining that the printer is ready to accept data, a byte is written to Port A. Hardware in the 8255A-5 will generate a low-going pulse on Port C bit 7 (Output Buffer Full). This pulse is fed into a 74LS123 one-shot to generate a fixed length pulse of about 1.5 µsec which is the specified length for line printer strobe. The line printer acknowledge is dual-routed to the line printer status port as well as to Port C bit 6

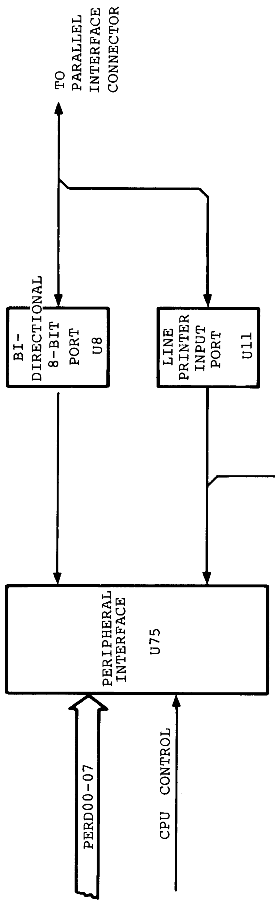


Figure 7-22. Parallel/Keyboard Interface

(ACKnowledge). A rising edge on the ACK* input of the 8255A-5 will cause an interrupt. Any read operation to the 8255A-5 will clear the interrupt.

Bit	Assignment
0	Auxiliary input 0 (currently unused)
1	Auxiliary input 1 (currently unused)
2	Auxiliary input 2 (currently unused)
3	LPRACK*
4	LPRFLT* (Line printer fault)
5	LPRSEL* (Line printer select)
6	LPRPAEM (Line printer paper empty)
7	LPRBSY (Line printer busy)

Table 7-2. Port B Bit Assignments

For bidirectional printer port operaton, the Port A/upper half of Port C combination must be programmed for Mode 2 operation. Port C bit 0 must be programmed for the direction of transfer ("0" for input from port, "1" for output to port). In this mode, Port C bits 4 - 7 take on new meanings. Bit 5 becomes IBFa (Input Buffer Full for Port A, active when the buffer contains unread data), bit 6 becomes ACKa (ACKnowledge output for Port A, same function as for unidirectional mode), and bit 7 becomes OBFa (Output Buffer Full output for Port A, also same as unidirectional mode).

7.1.10.2 Keyboard Interface

The keyboard interface is enabled for parallel input by setting Port C, bits 1 and 2 to "01". This enables the 74LS323 serial-to-parallel converter for output onto the Port B data bus. Data is shifted in serial fashion into the 74LS323 on KBDDAT on each KBDCLK rising edge. Data transfer is terminated with an End-of-Data pulse on KBDDAT (rising edge) while KBDCLK is low. This clocks a 74LS74 low, generating both KBDBSY* on its Q output and KBDINT10 on its Q* output. A read to address 0052H in CPU peripheral space (Port A read) will preset the 74LS74, thus removing KBDBSY* and KBDINT01.

Keyboard power is enabled through bit 0 at address 0000H in CPU peripheral space. This bit is cleared at reset, removing Vcc from the keyboard. When this bit is set to

"1", the logic level is translated to about +12 Vdc by a 751488 level shifter. This in turn drives the gate of an IRFD110 HEXFET, allowing current to pass from drain to source and on to the keyboard Vcc input. Driving -12 Vdc into the gate of the HEXFET (logic "0" translated by the 751488) turns the transistor and the keyboard off.

7.1.10.3 Revision Port

To read the revision port, Port C bits 1 and 2 must be programmed to a "10". This enables the 74LS244 buffer for output onto the Port B data bus. The revision port is encoded with an 8-bit number reflecting the current revision level of the main logic board. Each PCB update will increment this 8-bit value by one.

7.1.11 Serial Interface/Programmable Timer (Page 13)

7.1.11.1 Serial Interface

The serial interface relies on the 8251A Universal Synchronous/Asynchronous Receiver/Transmitter for its operation. The 8251A is used as a peripheral device and is programed by the CPU to operate using virtually any serial data transmission technique presently in use. The USART accepts data characters from the CPU in parallel format and then converts them into a continuous data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The 8251A is clocked at the rate of 2.00 MHz. The 8251A is mapped at 0010H - 001FH in the CPU peripheral address space at even locations only. Register addresses are given in Table 7-3.

Address	Read/Write	Operation
0010H	R	8251A Data -> Data Bus
0010H	W	Data Bus -> 8251A Data
0012H	R	8251A Status -> Data Bus
0012H	W	Data Bus -> 8251A Control

Table 7-3. 8251A Address Assignments

7.1.11.2 Counter/Timer Chip (Page 13)

The 8253-5 is a programmable counter/timer chip which is responsible for generating three timing signals:

1. Periodic speaker output

2. Baud rate clock for the 8251A

3. Refresh timing pulses for the dynamic RAM array

Ihe 8253-5 is mapped at 0040H - 004FH in the CPU peripheral address space at even addresses only. The register assignments are shown in Table 7-4.

Address	Read/Write	Operation
0040H	W	Load Counter 0
0042H	W	Load Counter 1
0044H	W	Load Counter 2
0046H	W	Write Mode Word
0040H	R	Read Counter 0
0042H	R	Read Counter 1
0044H	R	Read Counter 2
0046H	R	No operation

Table 7-4. 8253-5 Address Assignments

The clock for channel 0 is 1.00 MHz, channel 1 and channel 2 are 2.00 MHz. These clocks are derived from the 8.00 MHz clock from the CPU and are divided by 2 four times to generate 4.00 MHz, 2.00 MHz, 1.00 MHz, and 500 KHz by a 74LS161 binary counter.

7.1.11.3 RS-232 Operation (Page 13)

For asynchronous RS-232 operation, the baud rate clock for both transmit and receive is derived from the 8253-5 clock 1 output. To select the internally derived clock (external synchronous operation is outlined below), port 00H bit 1 is set to "1". This routes the 8253-5 clock 1 output to both the transmit and receive clock inputs on the 8251A. Bit assignments for port OOH are shown in Table 7-5.

Bit	Assignment	Function	Active Level
0	KBEN	Keyboard Enable	active high
1	EXTCLK	External baud rate clock	active high
2	SPKRGATE	Enable periodic speaker output	active high
3	SPKRDATA	Direct output to speaker	
4	RFSHEN	Enable refresh and baud rate clocks	active high
5	FDCRESET*	Reset 8272	active low
6	TMRIN0	Enable 80186 timer 0	active high
7	TMRIN1	Enable 80186 timer 1	active high

NOTE: Following a reset, all bits at port 00H are "0".

Table 7-5. Port 00H Bit Assignments

Inputs for the 8251A are taken from J1 after being level-shifted from +12 Vdc levels and inverted by 751489 interface chips. These inputs include: receive data, clear to send, and data set ready (all active low). Outputs from the 8251A which are inverted and level-shifted to +12 Vdc are: transmit data, request to send, and data terminal ready (all active low). Two active high outputs RxRDY and TxRDY) are ORed together to form SERINT02 (SERial INTerrupt controller 0, level 2). RxRDY goes active high when a full character is received. This bit is reset by a read to the data port. In a similar manner, TxEMP goes active high when the transmit buffer is empty while the transmitter is enabled or remains active high while the transmitter is disabled. It is reset by a write to the 8251A data port if the transmitter is enabled.

Synchronous operation is identical to asynchronous operation except that the transmit and receive clocks are supplied by the remote device. Like the data interface, these clocks are level-shifted by the 751489 inverting buffers. To route the external clocks to the 8251A, port 00H bit 1 must be set to "1".

Speaker Port

The speaker port has two modes of operation: periodic and direct. @or periodic mode, SPKRGATE and SPKRDATA must be set to "11" (bits 2 and 3 at port 00H, respectively). This enables output 0 of the 8253-5 to produce a 50% duty cycle square wave of programmed period. For direct mode, SPKRGATE should be set to "0". Then the speaker may be set and reset directly by SPKRDATA. Data from either source is buffered by a 75477 open collector high current buffer before being output to the AC-coupled speaker.

Refresh Clock

The output counter 2 is routed to the dynamic memory control logic and is used to indicate when it is time to do another refresh operation. This counter should be programmed for a pulse on terminal count and a 15 µsec period. Bit 4 at port 00H enables this output as well as clock 1 (the baud rate clock) when it is active high.

VCC AND GND LIST

DEVICE	REF. DESIGNATOR	+5 V	GND	+12 V	−12 V
7416	U138,140	14	7		
7438	U19	14	7		
74F00	U112	14	7		
74F02	U109	14	7		
74F04	U89,97	14	7		
74F08	U106,123	14	7		
74F32	U25,101,107,114,125,108	14	7		
74F64	U96	14	7		
74F138	U99	16	8		
74F161	U61,74	16	8		
74F244	U28,35	20	10		
74F245	U34,52,53,56,65,66,80	20	10		
74F258	U45,46	16	8		
74F373	U116,127	20	10		
74LS00	U4,91	14	7		
74LS02	U133	14	7		
74LS04	U23,120,122,137,141	14	7		
74LS08	U20,86	14	7		
74LS14	U139	14	7		
74LS30	U119	14	7		
74LS32	U2,21,85,136	14	7		
74LS38	U38,87	14	7		
74LS74	U3,84,88**,90,92,118,130	14	7		
74LS123	U24,132	16	8		
74LS125A	U22,27,83	14	7		
74LS138	U67,71	16	8		
74LS139	U98	16	8		
74LS161A	U73,100,104	16	8		
74LS193	U94	16	8		
74LS195	U131	16	8		
74LS241	U135	20	10		
74LS244	U10,11,17,33,58,78,81,105, 117,128,32	20	10		
74LS245	U8,44,50,51,54	20	10		
74LS273	U49,70,79	20	10		
74LS323	U9	20	10		
74LS373	U63,64,77	20	10		
74LS374	U36,57	20	10		
74LS393	U29	14	7		
74S00	U1	14	7		
74S74	U69	14	7		
74S112	U113,124	16	8		
74S139	U26	16	8		
74S157	U18	16	8		
74S260	U93	14	7		
74S280	U115,126	14	7		
75477	U129	8	4		
80186	U76	9,43	26,60		
8251A	U41	26	4		
8253-5	U40	24	12		
8255A-5	U75	26	7		
8259A-2	U42,43	28	14		
8272	U121	40	20		
82S153	U62,68	20	10		
CRT9007	U16	21	40		
CRT9021	U14	8	20		
CRT9212	U15,55	8	23		
FDC9216	U134	8	4		
MC1488	U5		7	14	1
MC1489	U6,7	14	7		
NE564	U72**		8		
PAL10L8	U82	20	10		
PAL16L8A	U95,102,103*	20	10		
PAL20L8	U103*	24	12		
PD4016	U12,13	24	12		
SPARE	U31	20	10		
SPARE	U142	20	10		
SPARE	U143	20	10		
74LS145	U30	16	8		
74LS174	U60	16	8		
74LS378	U37	16	8		
74S04	U39	14	7		

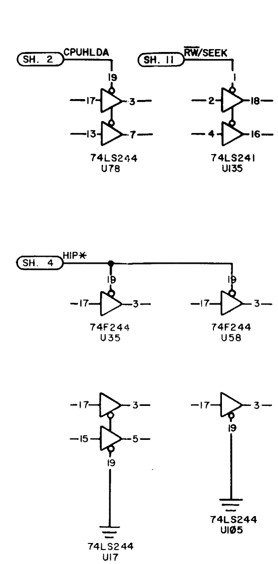
* U103 MAY USE A PAL16L8A OR PAL20L8 DEPENDING UPON PROGRAM REQUIREMENTS (SEE SHEET 3).

** U72 AND U88 ARE LOCATED IN AN ISOLATED Vcc AND GND AREA (SEE SHEET 7).

SPARE GATES LIST

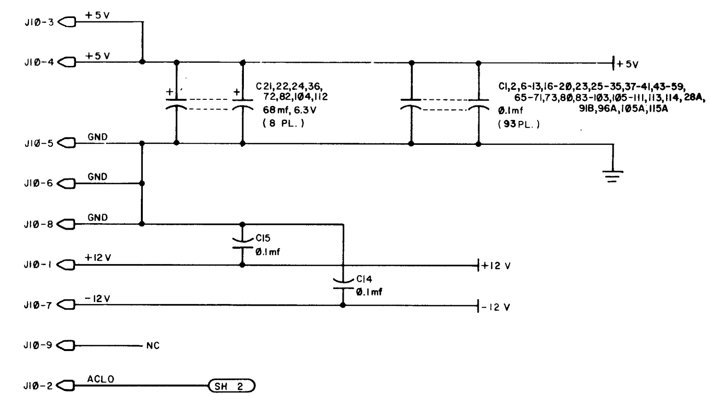
DEVICE	REF. DESG.	GATES NOT USED
7416	U138	1-6
7438	U19	1-6
74F00	U108	1-3,11-13
74F02	U109	4-6
74F08	U106	4-6,8-13
74F32	U25	11-13
74F32	U107	1-3,8-10
74LS00	U4	11-13
74LS00	U91	4-6
74LS02	U133	8-10
74LS04	U120	3-6,12,13
74LS04	U141	3-6,10,11
74LS08	U20	1-3
74LS14	U139	1,2
74LS32	U2	1-3
74LS32	U85	4-6,8-10
74LS32	U136	1-6
74LS38	U38	1-6,8-10
74LS38	U87	8-10
74LS74	U118	8-13
74LS123	U132	1-4,13-15
74LS125A	U22	11-13
74LS125A	U83	1-6
74S00	U1	1-3
74S157	U18	9-14
74S260	U93	1-3,5,12,13
MC1489	U7	11-13

SPARE BUFFERS



REFERENCE DESIGNATORS

LAST USED	NOT USED
U143	U111
Y1	
RP5	
CR1	
Q2	
J11	
R59	R17
C116	
L1	

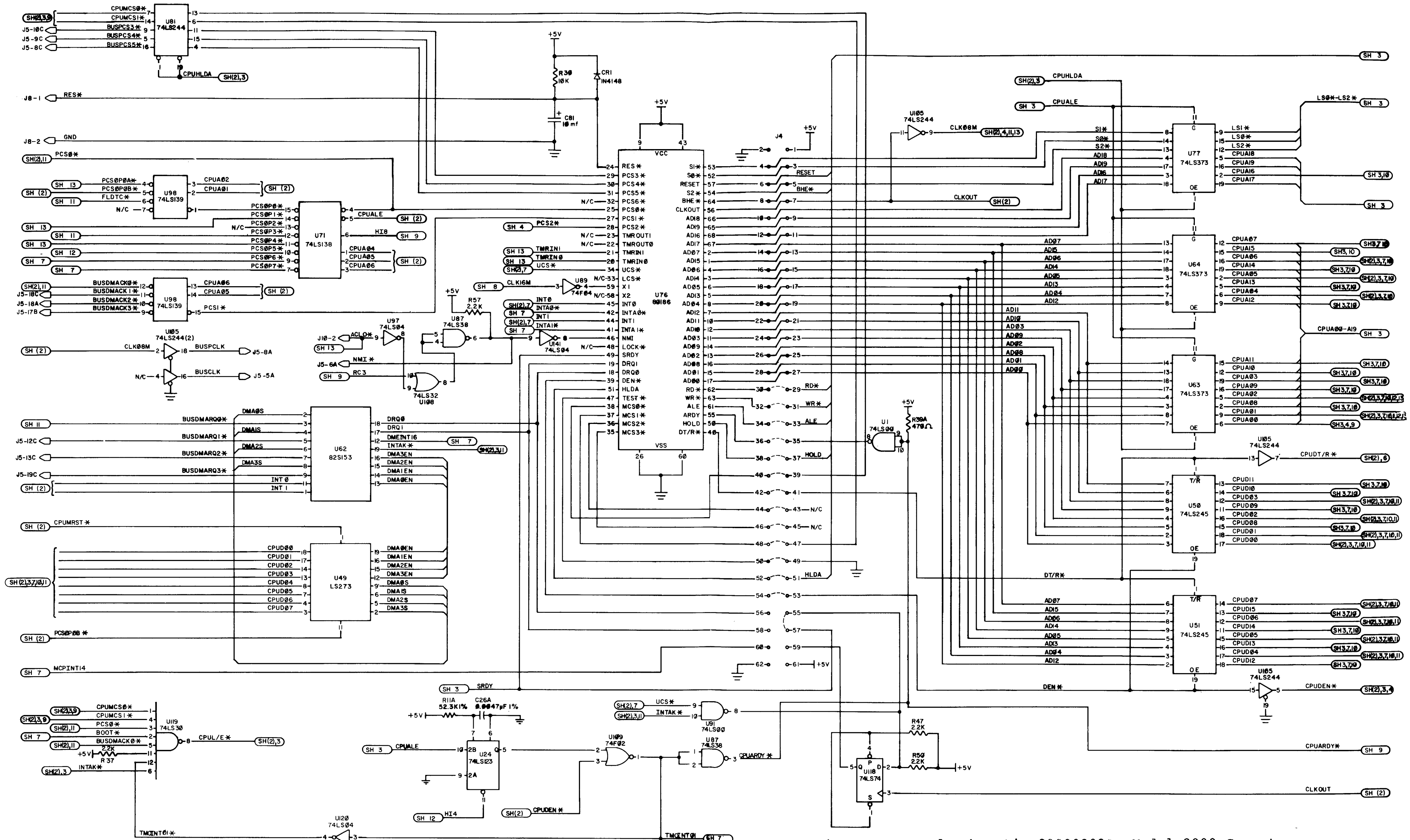


DC POWER SCHEMATIC

⚠ CONFIGURATION STATUS PORT: THE MAIN LOGIC BOARD HAS AN 8-BIT PORT THAT INDICATES THE CONFIGURATION STATUS OF THE PRINTED CIRCUIT BOARD WITH RESPECT TO SOFTWARE. THE INPUT STRAPPING TO THIS REGISTER (U10) MUST BE INCREMENTED BY ONE FOR EACH REVISION OF THE PC BOARD THAT DIRECTLY AFFECTS PROGRAMMING. THE HEX CODE FOR EACH PC BOARD CONFIGURATION CHANGE APPEARS IN THE CONFIGURATION STATUS SCHEDULE AT RIGHT (SEE SHEET 12).

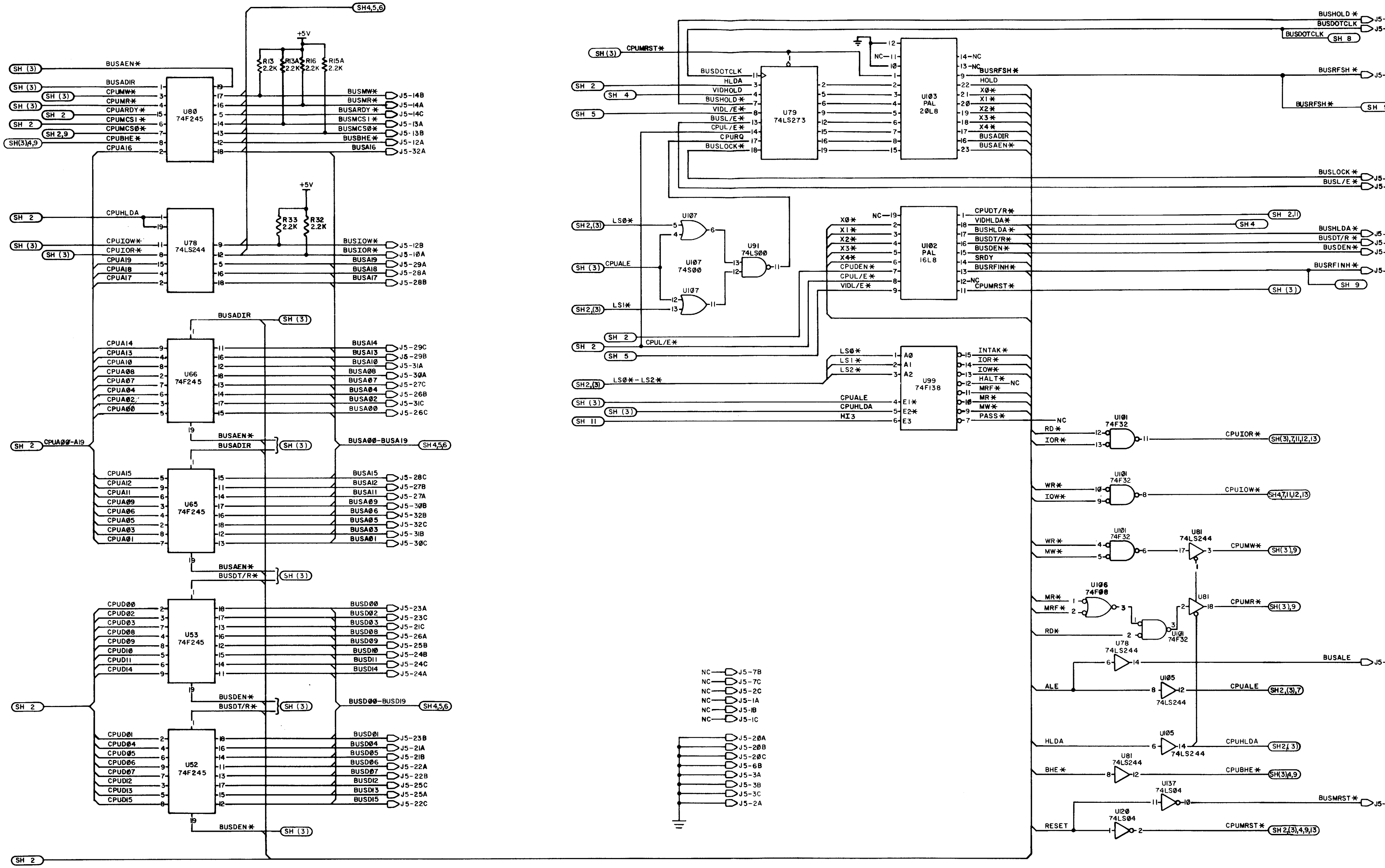
Main Logic Board Schematic 80000203A, Model 2000 Computer
Page 1 of 13

Main Logic Board Schematic 80000203A, Model 2000 Computer
Page 1 of 13



Main Logic Board Schematic 80000203A, Model 2000 Computer
Page 2 of 13

Main Logic Board Schematic 80000203A, Model 2000 Computer
CPU Page 2 of 13



Main Logic Board Schematic 80000203A, Model 2000 Computer
Bus Interface Page 3 of 13

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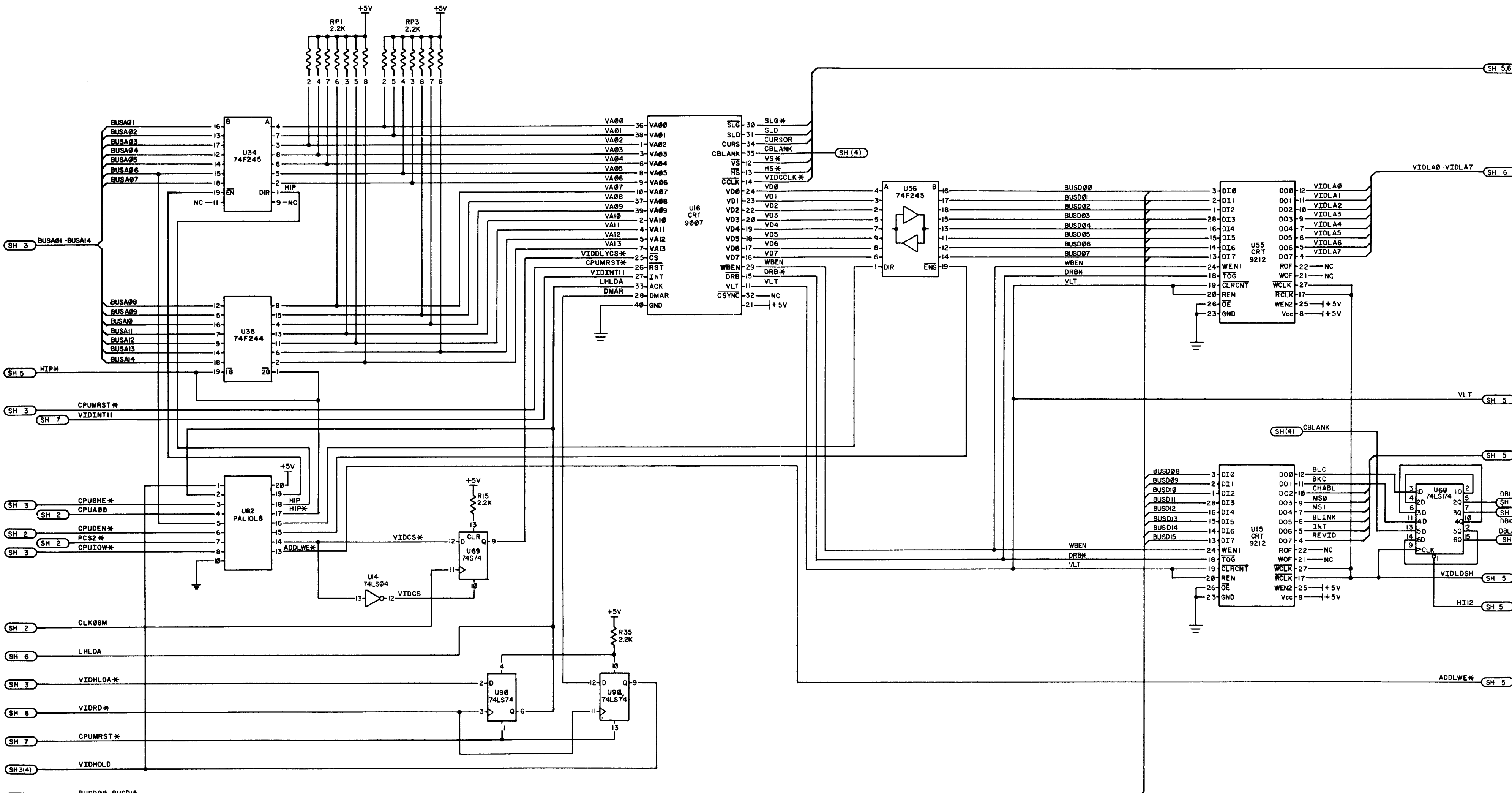
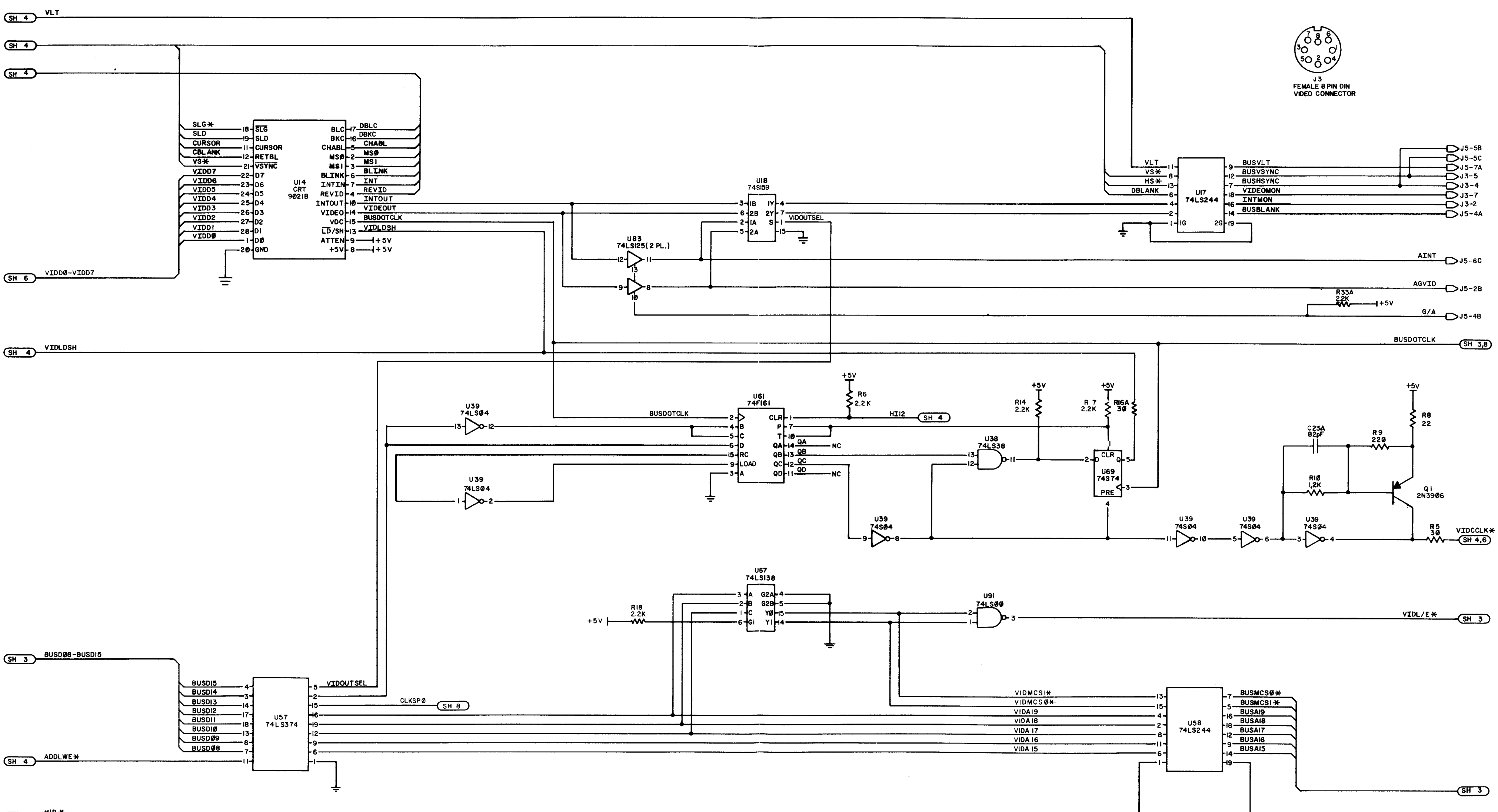
Bus Interface Page 3 of 13



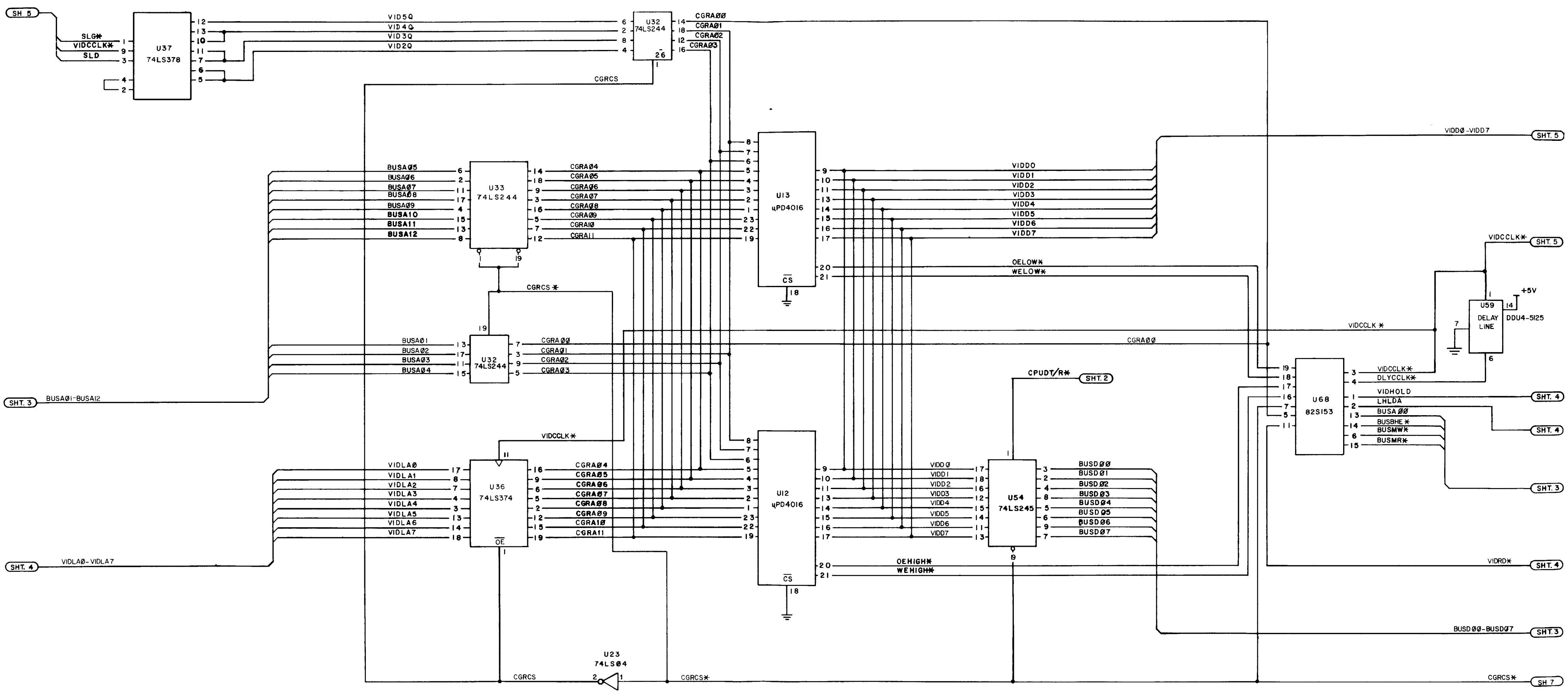
Main Logic Board Schematic 80000203A, Model 2000 Computer
CRT Controller/Main Video Logic   Page 4 of 13

Main Logic Board Schematic 80000203A, Model 2000 Computer
CRT Controller/Main Video Logic Page 4 of 13



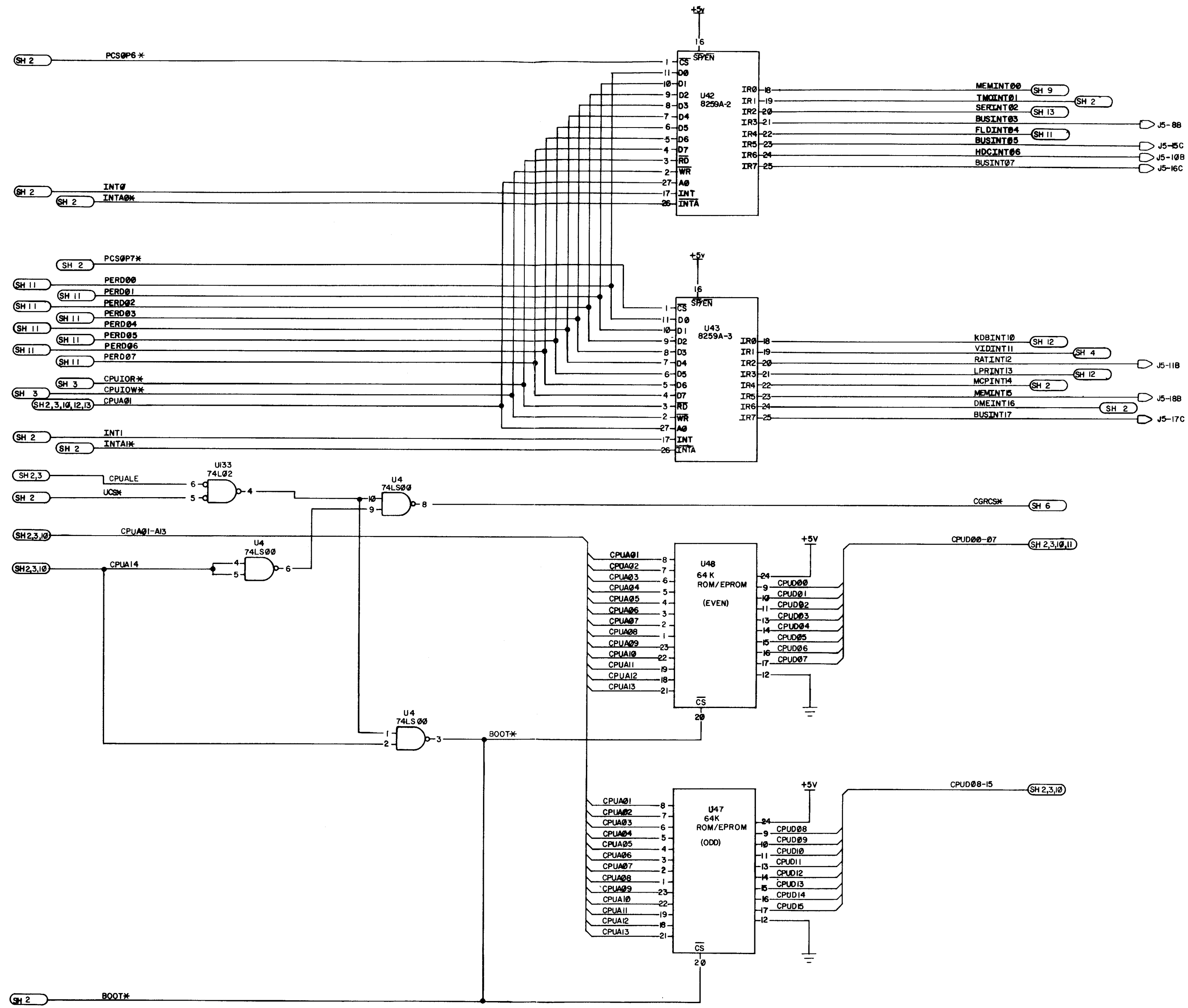
Main Logic Board Schematic 80040203A, Model 2000 Computer
Main Video Logic Page 5 of 13

Main Logic Board Schematic 80040203A, Model 2000 Computer
Main Video Logic Page 5 of 13



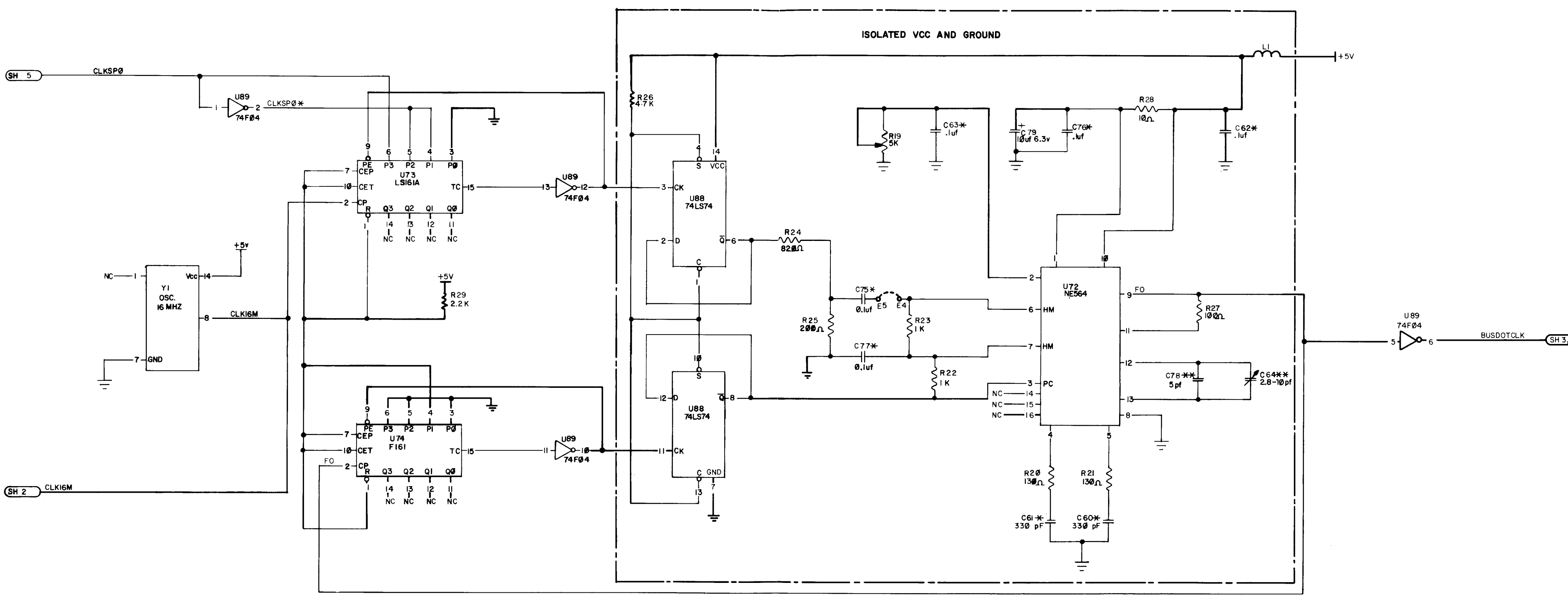
U37 74LS378
U32 74LS244
U33 74LS244
U36 74LS374
U13 uPD4016
U12 uPD4016
U54 74LS245
U68 82S153
U59 DELAY LINE DDU4-5125
U23 74LS04
SH 5
SHT. 3
SHT. 4
SHT. 5
SHT. 2
SH 7
SLG*
VIDCCLK*
SLD
VID5Q
VID4Q
VID3Q
VID2Q
CGRCS
CGRCS*
BUSAØ1-BUSA12
VIDLAØ-VIDLA7
VIDDØ-VIDD7
OELOW*
WELOW*
OEHIGH*
WEHIGH*
CPUDT/R*
VIDHOLD
LHLDA
BUSAØØ
BUSBHE*
BUSMW*
BUSMR*
DLYCCLK*
VIDRD*
BUSDØØ-BUSDØ7
+5V

Main Logic Board Schematic 80000203A, Model 2000 Computer
Character Generator I/F Logic Page 6 of 13



+5V
U42
8259A-2
U43
8259A-3
SP/EN
PCS0P6*
PCS0P7*
INT0
INTA0*
INT1
INTA1*
PERD00
PERD01
PERD02
PERD03
PERD04
PERD05
PERD06
PERD07
CPUIOR*
CPUIOW*
CPUA01
MEMINT00
TMRINT01
SERINT02
BUSINT03
FLDINT04
BUSINT05
HDCINT06
BUSINT07
KDBINT10
VIDINT11
RATINT12
LPRINT13
MCPINT14
MEMINT15
DMEINT16
BUSINT17
J5-8B
J5-15C
J5-10B
J5-16C
J5-11B
J5-18B
J5-17C
U133
74L02
U4
74LS00
CPUALE
UCS*
CGRCS*
CPUA01-A13
CPUA14
BOOT*
U48
64K
ROM/EPROM
(EVEN)
U47
(ODD)
CPUD00-07
CPUD08-15
SH 2
SH 3
SH 4
SH 6
SH 9
SH 11
SH 12
SH 13
SH 2,3
SH2,3,10
SH2,3,10,11
SH2,3,10,12,13

Main Logic Board Schematic 80000203A, Model 2000 Computer
Interrupt Controller/Boot ROM Page 7 of 13



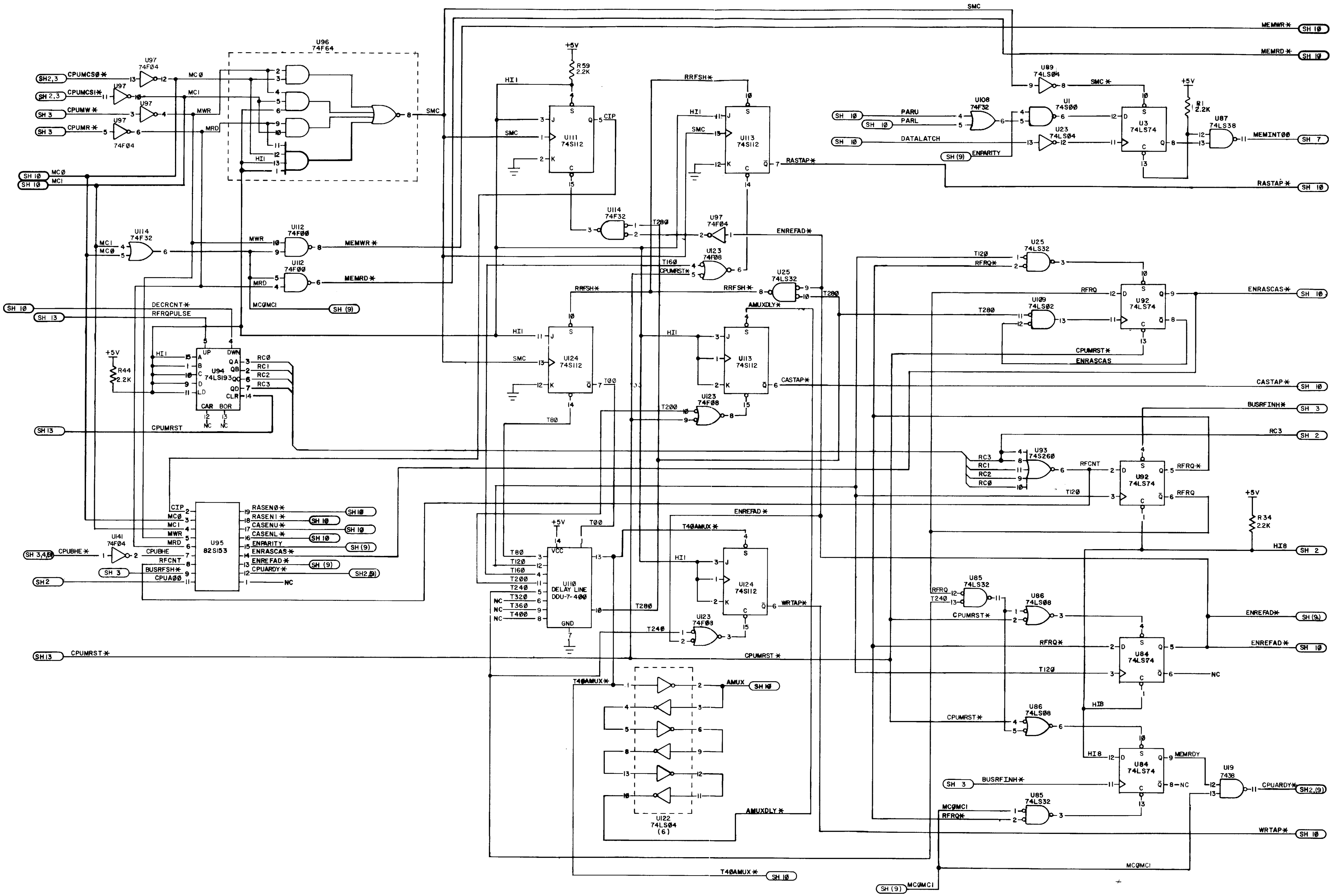
* – MUST BE THOMPSON CSF CAPACITORS

** – MUST BE NPO TEMPATURE COEFFICIENT CAPACITORS

$$FO = \frac{\text{CLK16M} \times 28}{16 \text{ or } 18 \text{ or } 20}$$

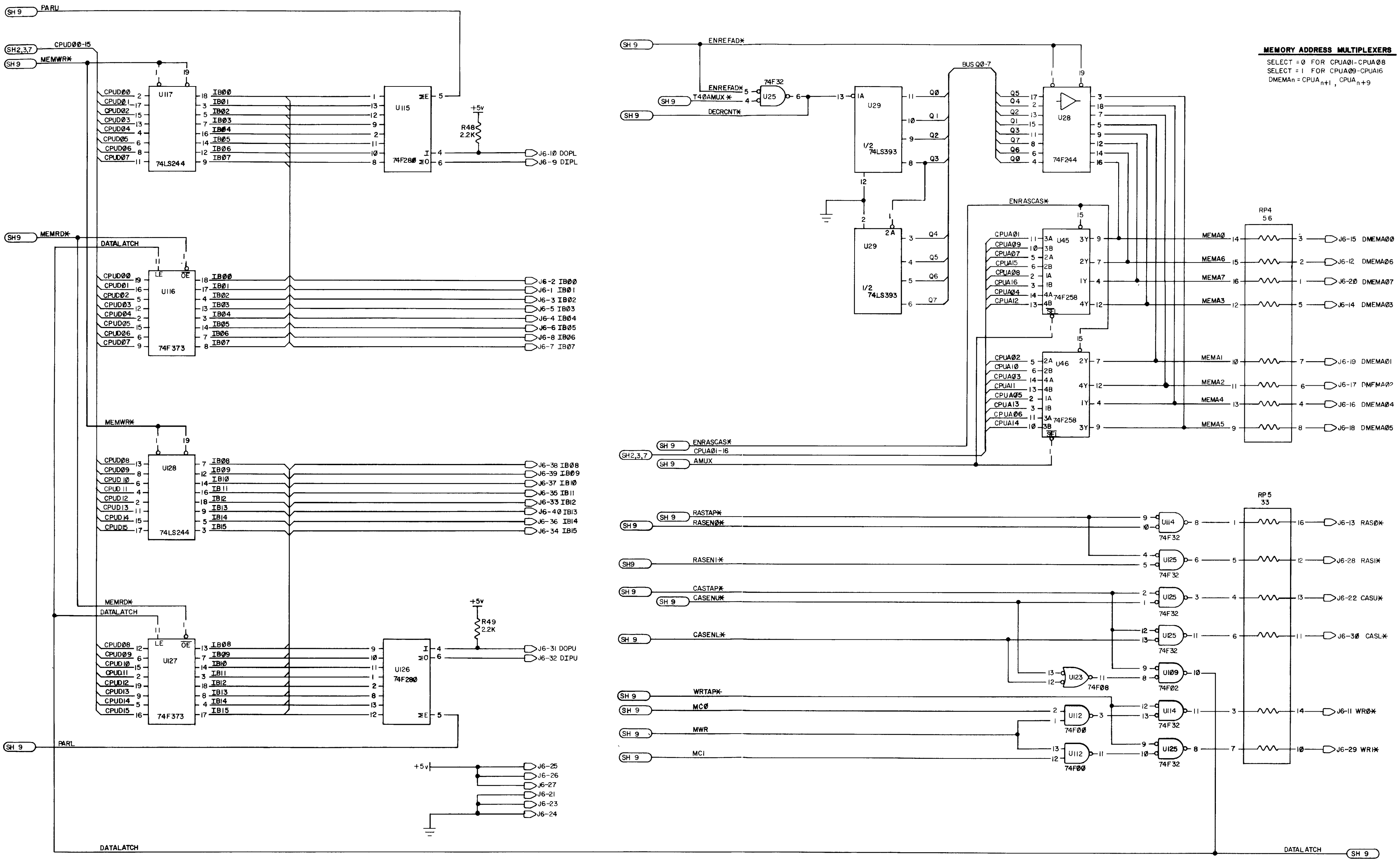
	Fin (MHZ)	
	15.990921	16.ØØØ
Fout (MHZ)	27.984111	28.ØØ
	22.387289	22.4ØØ

Main Logic Board Schematic 80000203A, Model 2000 Computer
Clock/Phase Lock Loop Page 8 of 13



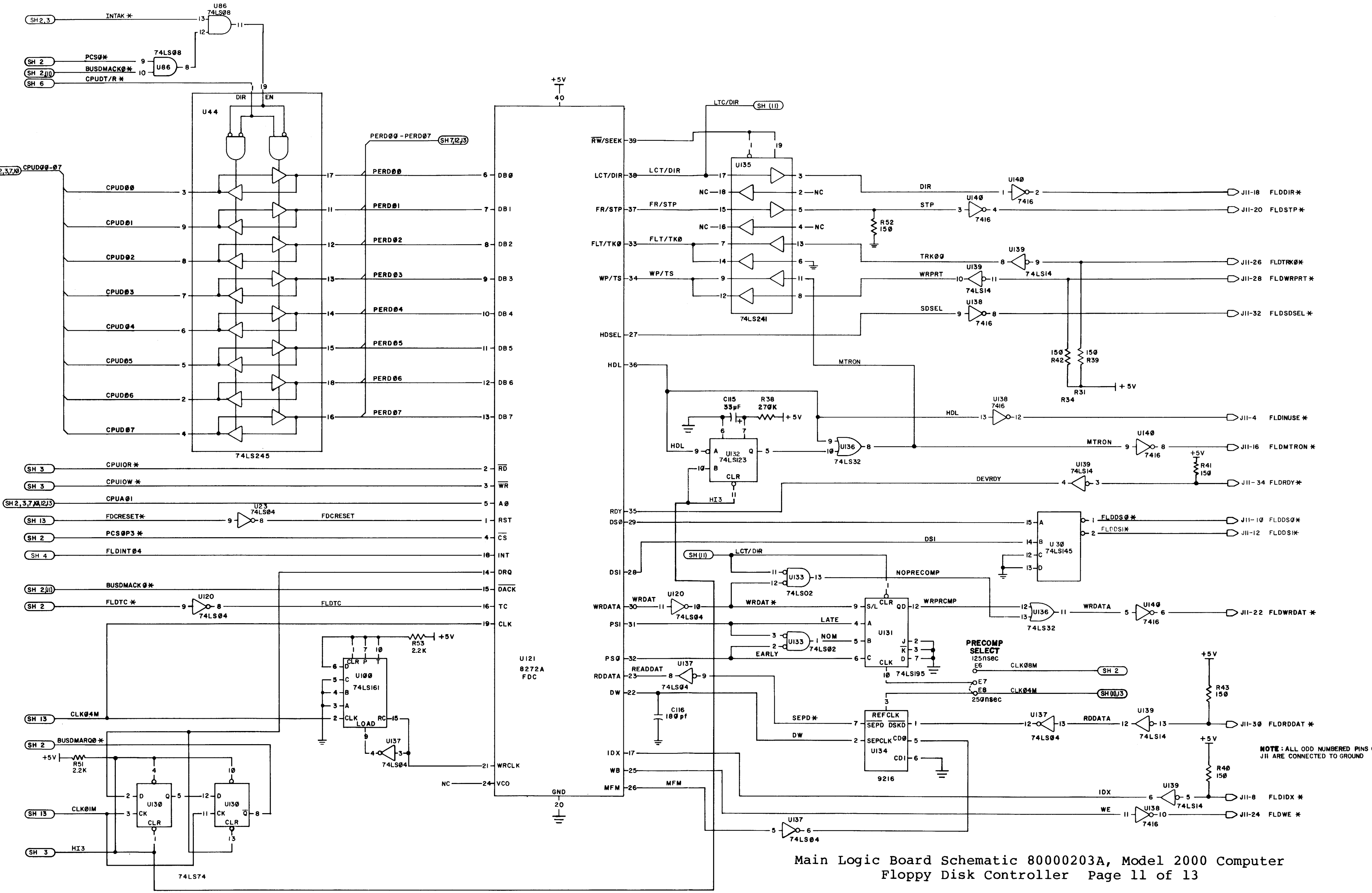
Main Logic Board Schematic 80000203A, Model 2000 Computer
Memory Timing Page 9 of 13

Main Logic Board Schematic 80000203A, Model 2000 Computer
Memory Timing Page 9 of 13



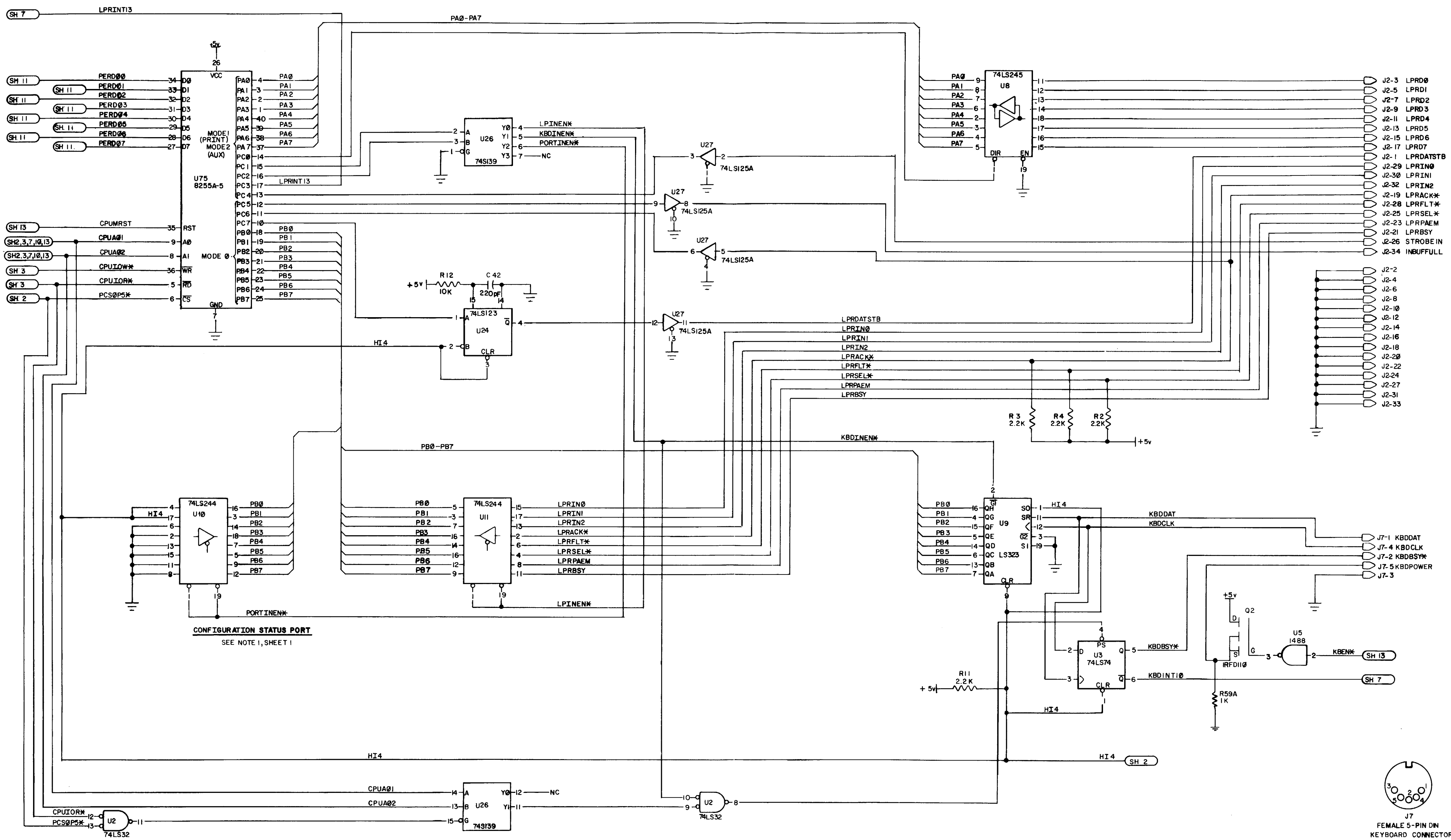
Main Logic Board Schematic 80000203A, Model 2000 Computer
Memory Control Page 10 of 13

Main Logic Board Schematic 80000203A, Model 2000 Computer
Memory Control Page 10 of 13



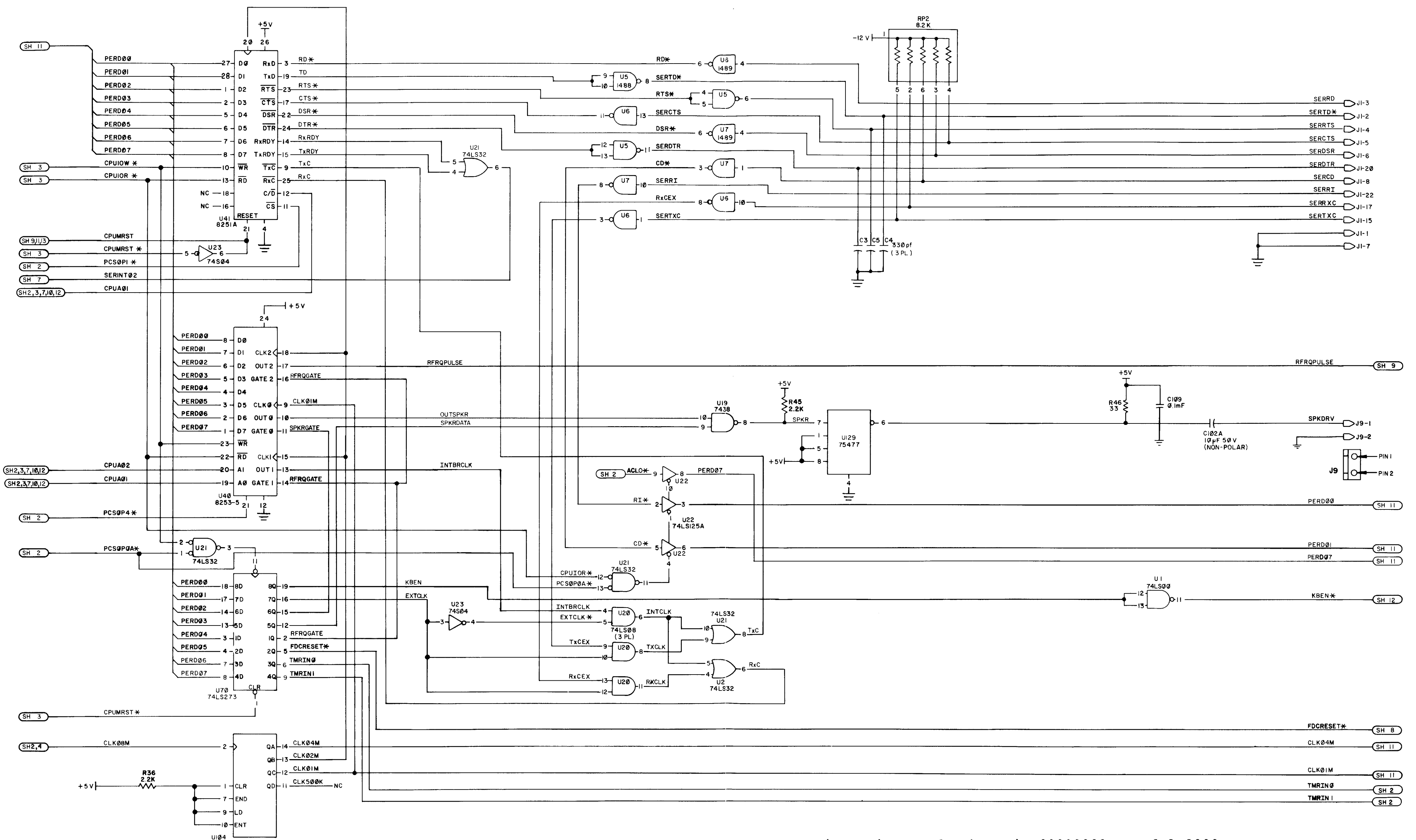
Main Logic Board Schematic 80000203A, Model 2000 Computer
Floppy Disk Controller Page 11 of 13

Main Logic Board Schematic 80000203A, Model 2000 Computer
Floppy Disk Controller Page 11 of 13



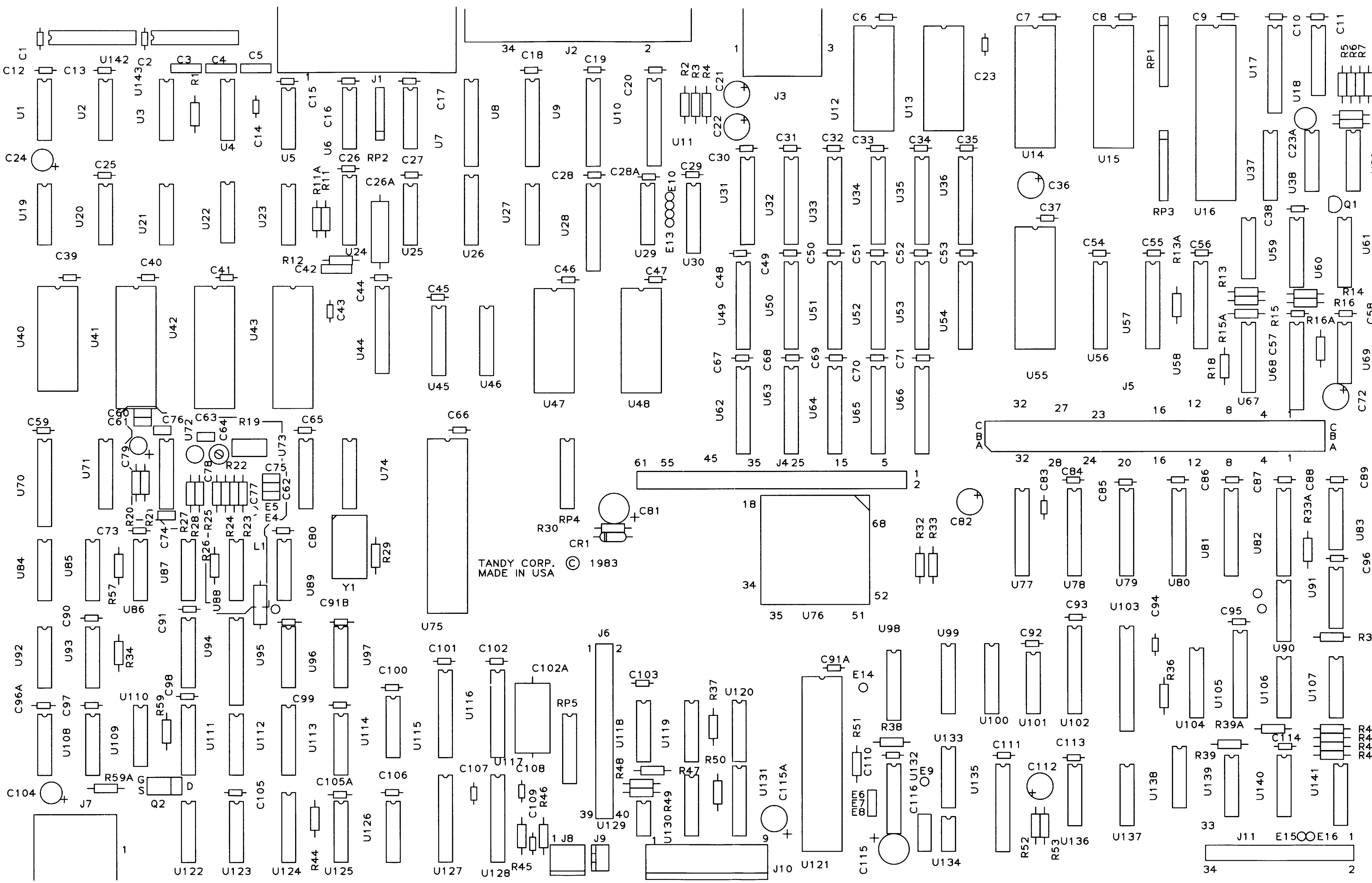
Main Logic Board Schematic 80000203A, Model 2000 Computer
Parallel/Keyboard Interface Page 12 of 13

Main Logic Board Schematic 80000203A, Model 2000 Computer
Parallel/Keyboard Interface Page 12 of 13

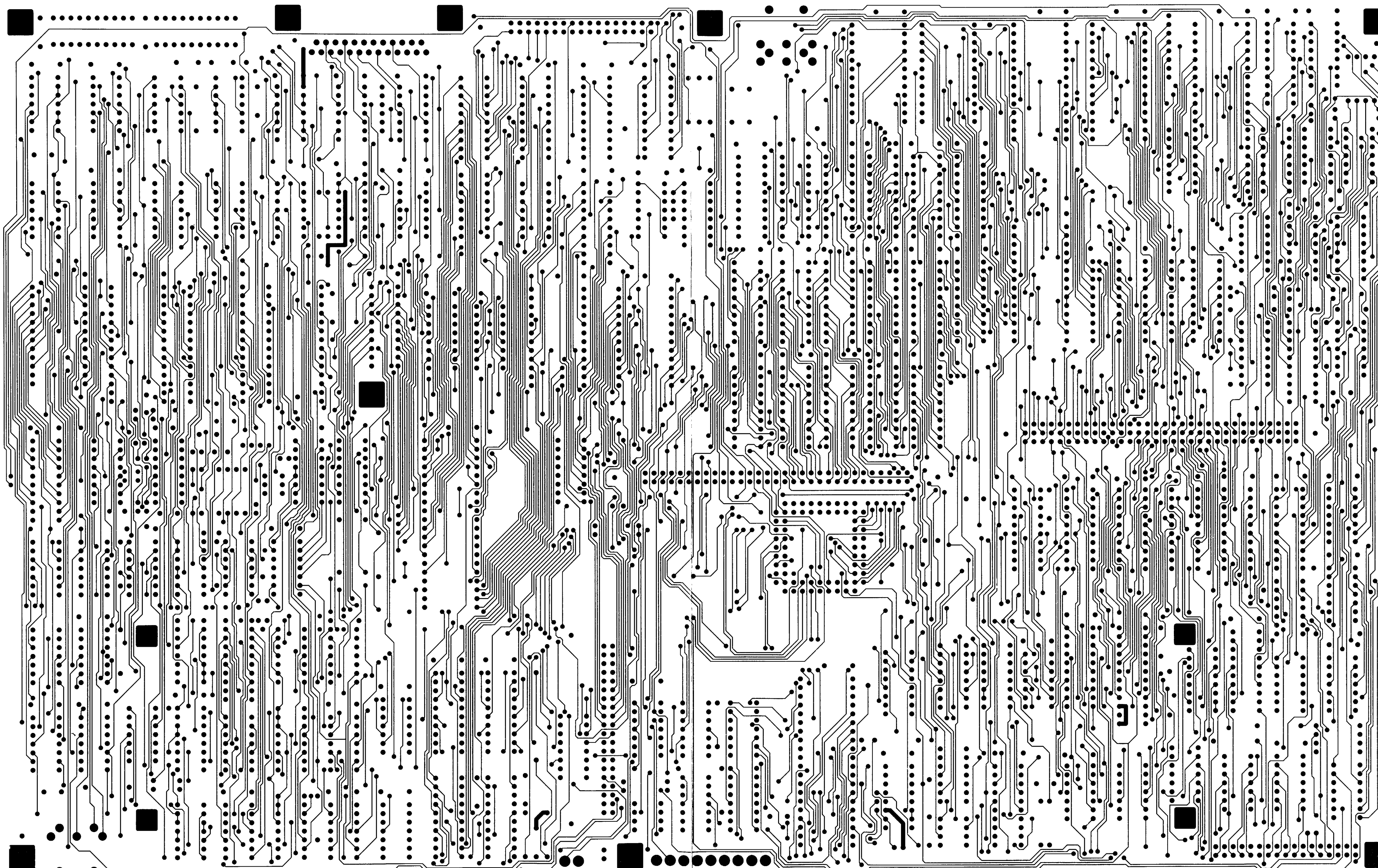


Main Logic Board Schematic 80000203A, Model 2000 Computer
Serial Interface/Programmable Timer Page 13 of 13

Main Logic Board Schematic 80000203A, Model 2000 Computer
Serial Interface/Programmable Timer Page 13 of 13



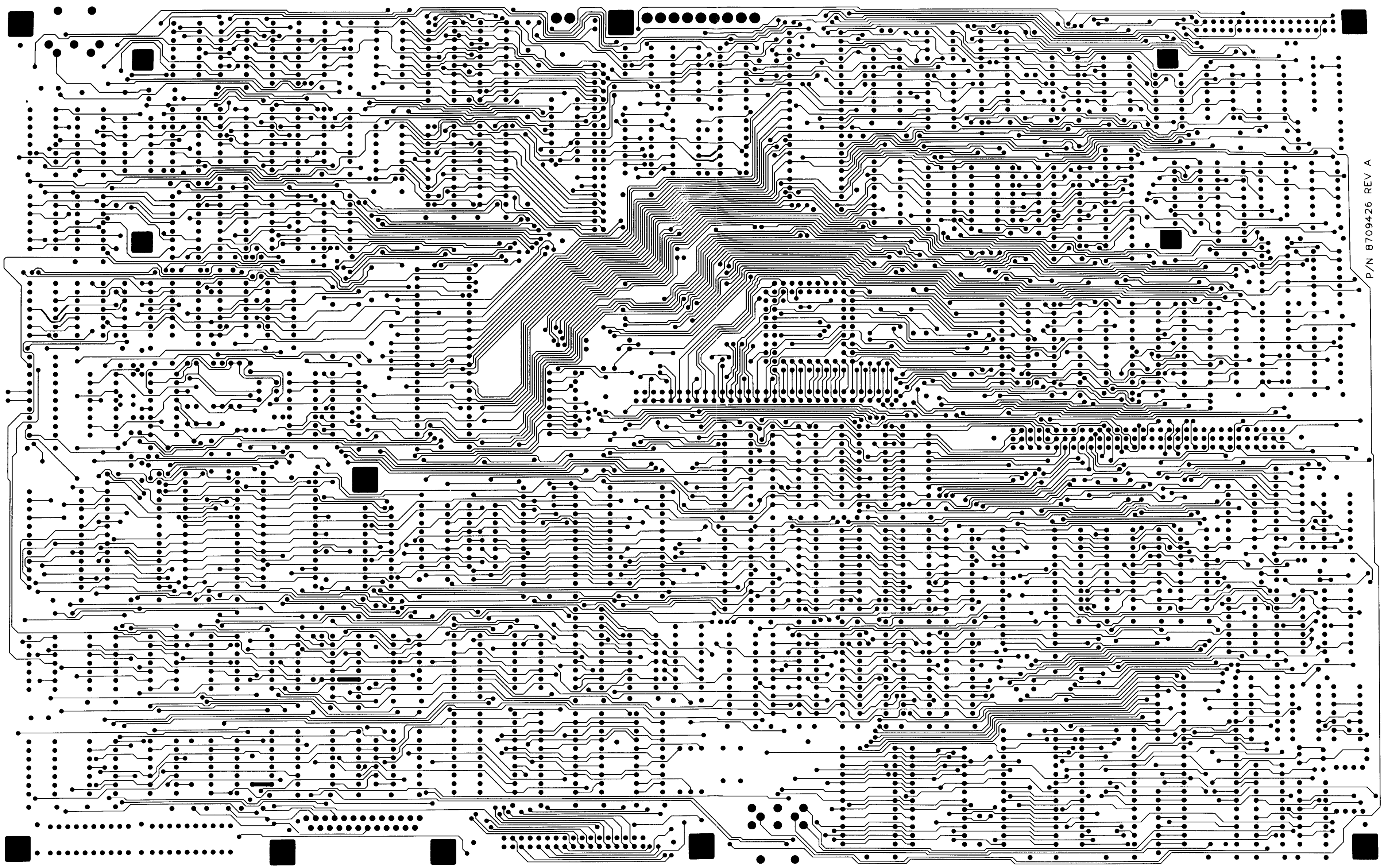
Component Layout 1700245, Main Logic Board 8898800A
Model 2000 Computer Assembly



Circuit Trace 1700245, Component Side
Main Logic PCB Assembly 8898800A

Circuit Trace 1700245, Ground Plane, Component Side
Main Logic PCB Assembly 8898800A

Circuit Trace 1700245, Power Plane, Solder Side
Main Logic PCB Assembly 8898800A



Circuit Trace 1700245, Solder Side
Main Logic PCB Assembly 8898800A

Parts List

Main Logic PCB 8898800A, Model 2000

Item	Sym	Description	Part Number
1	1	Main Logic PCB	8709426
2	1	Socket, 8-Pin DIP (U134)	8509011
3	5	Socket, 20-Pin DIP (U62,68, U82,95,102,103)	8509009
4	5	Socket, 24-Pin DIP (U12,13, U40,47,48)	8509001
5	6	Socket, 28-Pin DIP (U14,15, U41-43, 55)	8509007
6	3	Socket, 40-Pin DIP (U16,75, U121)	8509002
7	1	Socket, 68-Pin Jedec A (U76)	8509017
8	1	Connector, 8-Pin DE8 (J3)	8519203
9	1	Header, 2-Pin (J8)	8519208
10	1	Connector, 9-Pin (J10)	8519191
11	1	Connector, 96-Pin Euro (J5)	8519182
12	1	Connector, Dual 17-Pin (J11)	8519120
13	1	Header, Dual 20-Pin (J6)	8519202
14	1	Connector, 25-Pin (J1)	8519190
15	1	Connector, 5-Pin DIN	8519085
16	1	Connector, 31-Pin (J4)	8519209
17	1	Connector, 34-Pin (J2)	8519198
18	1	Connector, 2-Pin (J9)	8519193
	C1	Capacitor, 470 mfd, 16V Elec Axial	
	C2	Not Used	
	C3	Capacitor, 330 pfd, Dipped Mica 5%	8341337
	C4	Capacitor, 330 pfd, Dipped Mica 5%	8341337
	C5	Capacitor, 330 pfd, Dipped Mica 5%	8341337
	C6	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C7	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C8	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C9	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C10	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C11	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C12	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C13	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C14	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C15	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C16	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C17	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C18	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C19	Capacitor, .1 mfd, 50V Mono Axial	8374104

Parts List

Main Logic PCB 8898800A, Model 2000

Item	Sym	Description	Part Number
	C20	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C21	Capacitor, 68 mfd, 6.3V Tantalum	
	C22	Capacitor, 68 mfd, 6.3V Tantalum	
	C23	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C23a	Capacitor, 82 pfd, 50V Ceramic	
	C24	Capacitor, 68 mfd, 6.3V Tantalum	
	C25	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C26	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C26a	Capacitor, ____________________	_______
	C27	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C28	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C29	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C30	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C31	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C32	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C33	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C34	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C35	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C36	Capacitor, 68 mfd, 6.3V Tantalum	
	C37	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C38	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C39	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C40	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C41	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C42	Capacitor, 220 pfd, Dipped Mica 5%	8341227
	C43	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C44	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C45	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C46	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C47	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C48	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C49	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C50	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C51	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C52	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C53	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C54	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C55	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C56	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C57	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C58	Capacitor, .1 mfd, 50V Mono Axial	8374104

Parts List

Main Logic PCB 8898800A, Model 2000

Item	Sym	Description	Part Number
	C59	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C60	Capacitor, 470 pfd, 50V Cer Disk	
	C61	Capacitor, 470 pfd, 50V Cer Disk	
	C62	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C63	Capacitor, .1 mfd, 50V	8394104
	C64	Capacitor, 2.8-10 pfd, Trimmer	8360310
	C65	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C66	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C67	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C68	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C69	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C70	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C71	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C72	Capacitor, 68 mfd, 6.3V Tantalum	
	C73	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C74	Capacitor, .1 mfd, 50V	8394104
	C75	Capacitor, .1 mfd, 50V	8394104
	C76	Capacitor, .1 mfd, 50V	8394104
	C77	Capacitor, .1 mfd, 50V	8394104
	C78	Capacitor, 5 pfd, 50V Ceramic	8300054
	C79	Capacitor, 10 mfd, 6.3 Tantalum	
	C80	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C81	Capacitor, 10 mfd, 6.3 Tantalum	
	C82	Capacitor, 68 mfd, 6.3V Tantalum	
	C83	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C84	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C85	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C86	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C87	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C88	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C89	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C90	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C91	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C92	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C93	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C94	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C95	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C96	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C97	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C98	Capacitor, .1 mfd, 50V Mono Axial	8374104

Parts List

Main Logic PCB 8898800A, Model 2000

Item	Sym	Description	Part Number
	C99	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C100	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C101	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C102	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C103	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C104	Capacitor, 68 mfd, 6.3V Tantalum	
	C105	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C106	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C107	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C108	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C109	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C110	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C111	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C112	Capacitor, 68 mfd, 6.3V Tantalum	
	C113	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C114	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C115	Capacitor, 33 mfd, 10V Tantalum	
	C116	Capacitor, 180 pfd, Dipped Mica 5%	8341187
	CR1	Diode, 1N4148	8150148
	Q1	Transistor, 2N3906	8100906
	Q2	Transistor, IRFD110, MOSFET	8110110
	R1	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R2	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R3	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R4	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R5	Resistor, 30 ohm, 1/4W 5%	8207030
	R6	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R7	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R8	Resistor, 22 ohm, 1/4W 5%	8207022
	R9	Resistor, 220 ohm, 1/4W 5%	8207122
	R10	Resistor, 1.2 kohm, 1/4W 5%	8207212
	R11	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R12	Resistor, 10 kohm, 1/4W 5%	8207310
	R13	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R14	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R15	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R16	Resistor, 2.2 kohm, 1/4W 5%	8207222

Parts List

Main Logic PCB 8898800, Model 2000

Item	Sym	Description	Part Number
	R17	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R18	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R19	Potentiometer, 5 kohm, Trimpot	
	R20	Resistor, 130 ohm, 1/4W 5%	8207113
	R21	Resistor, 130 ohm, 1/4W 5%	8207113
	R22	Resistor, 1 kohm, 1/4W 5%	8207210
	R23	Resistor, 1 kohm, 1/4W 5%	8207210
	R24	Resistor, 820 ohm, 1/4W 5%	8207182
	R25	Resistor, 200 ohm, 1/4W 5%	8207120
	R26	Resistor, 4.7 kohm, 1/4W 5%	8207247
	R27	Resistor, 100 ohm, 1/4W 5%	8207110
	R28	Resistor, 10 ohm, 1/4W 5%	8207010
	R29	Resistor, 390 ohm, 1/4W 5%	8207139
	R30	Resistor, 10 kohm, 1/4W 5%	8207310
	R31	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R32	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R33	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R34	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R35	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R36	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R37	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R38	Resistor, 270 kohm, 1/4W 5%	8207427
	R39	Resistor, 150 ohm, 1/4W 5%	8207115
	R40	Resistor, 150 ohm, 1/4W 5%	8207115
	R41	Resistor, 150 ohm, 1/4W 5%	8207115
	R42	Resistor, 150 ohm, 1/4W 5%	8207115
	R43	Resistor, 150 ohm, 1/4W 5%	8207115
	R44	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R45	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R46	Resistor, 33 ohm, 1/4W 5%	8207033
	R47	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R48	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R49	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R50	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R51	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R52	Resistor, 150 ohm, 1/4W 5%	8207115
	R53	Resistor, 2.2 kohm, 1/4W 5%	8207222

Parts List

Main Logic PCB 8898800, Model 2000

Item	Sym	Description	Part Number
	RP1	Resistor Pak, 2.2 kohm, 8-Pin SIP	8290039
	RP2	Resistor Pak, 8.2 kohm, 6-Pin SIP	8290036
	RP3	Resistor Pak, 2.2 kohm, 8-Pin SIP	8290039
	RP4	Resistor Pak, 56 ohm DIP 16-Pin	8290034
	RP5	Resistor Pak, 33 ohm DIP 16-Pin	8290044
	U1	IC, 74S00, Quad 2-Input NAND	8010000
	U2	IC, 74LS32, OR Gate	8020032
	U3	IC, 74LS74, Flip Flop	8020074
	U4	IC, 74LS00, NAND Gate	8020000
	U5	IC, MC1488, Driver	8050188
	U6	IC, MC1489, Receiver	8050189
	U7	IC, MC1489, Receiver	8050189
	U8	IC, 74LS245, Transceiver	8020245
	U9	IC, 74LS323, Storage Register	8020323
	U10	IC, 74LS244, Line Driver	8020244
	U11	IC, 74LS244, Line Driver	8020244
	U12	IC, PD4016, 2K x 8 Static RAM	8041116
	U13	IC, PD4016, 2K x 8 Static RAM	8041116
	U14	IC, CRT9021	8040021
	U15	IC, CRT9212	8040212
	U16	IC, CRT9007	8040007
	U17	IC, 74LS244, Line Driver	8020244
	U18	IC, 74S157, Multiplexer	8010157
	U19	IC, 7438, NAND	8000038
	U20	IC, 74LS08, AND Gate	8020008
	U21	IC, 74LS32, OR Gate	8020032
	U22	IC, 74LS125A, Buffer	8020125
	U23	IC, 74LS04, Hex Inverter	8020004
	U24	IC, 74LS123, Multivibrator	8020123
	U25	IC, 74F32, Quad 2-Input OR	8015032
	U26	IC, 74S139, Dual Decoder	8010139
	U27	IC, 74LS125A, Buffer	8020125
	U28	IC, 74F244, Octal Buffer	8015244
	U29	IC, 74LS393, Counter	8020393
	U31	IC, 74LS244, Line Driver	8020244
	U32	IC, 74LS244, Line Driver	8020244
	U33	IC, 74LS244, Line Driver	8020244
	U34	IC, 74F245, Octal Transceiver	8015245
	U35	IC, 74F244, Octal Buffer	8015244
	U36	IC, 74LS374, Flip Flop	8020374
	U37	IC, 74LS378, Hex Flip Flop	8020378

Parts List

Main Logic PCB 8898800, Model 2000

Item	Sym	Description	Part Number
	U38	IC, 74LS38, Buffer	8020038
	U39	IC, 74S04, Hex Inverter	8010004
	U40	IC, 8253-5, Timer	8040253
	U41	IC, 8251A, Interface	8040251
	U42	IC, 8259A2, Interrupt Controller	8040259
	U43	IC, 8259A2, Interrupt Controller	8040259
	U44	IC, 74LS245, Transceiver	8020245
	U45	IC, 74F258, Multiplexer	8015258
	U46	IC, 74F258, Multiplexer	8015258
	U47	IC, 64K Boot ROM, Low	8040035
	U48	IC, 64K Boot ROM, High	8040035
	U49	IC, 74LS273, Flip Flop	8020273
	U50	IC, 74LS245, Transceiver	8020245
	U51	IC, 74LS245, Transceiver	8020245
	U52	IC, 74F245, Octal Transceiver	8015245
	U53	IC, 74F245, Octal Transceiver	8015245
	U54	IC, 74LS245, Transceiver	8020245
	U55	IC, CRT9212	8040212
	U56	IC, 74F245, Octal Transceiver	8015245
	U57	IC, 74LS374, Flip Flop	8020374
	U58	IC, 74LS244, Line Driver	8020244
	U61	IC, 74F161, Binary 4-Bit Counter	8015161
	U62	IC, 82S153, Logic Array	8040153
	U63	IC, 74LS373, Octal Latch	8020373
	U64	IC, 74LS373, Octal Latch	8020373
	U65	IC, 74F245, Octal Transceiver	8015245
	U66	IC, 74F245, Octal Transceiver	8015245
	U67	IC, 74LS138, Decoder	8020138
	U68	IC, 82S153, Logic Array	8040153
	U69	IC, 74S74, Flip Flop	8010074
	U70	IC, 74LS273, Flip Flop	8020273
	U71	IC, 74LS138, Decoder	8020138
	U72	IC, NE564	8040564
	U73	IC, 74LS161A, Shift Register	8020161
	U74	IC, 74F161, Binary 4-Bit Counter	8015161
	U75	IC, 8255A5, Interface	8040255
	U76	IC, 80186	8040186
	U77	IC, 74LS373, Octal Latch	8020373
	U78	IC, 74LS244, Line Driver	8020244
	U79	IC, 74LS273, Flip Flop	8020273
	U80	IC, 74F245, Octal Transceiver	8015245
	U81	IC, 74LS244, Line Driver	8020244

Parts List

Main Logic PCB 8898800, Model 2000

Item	Sym	Description	Part Number
	U82	IC, PAL10L8	8041108
	U83	IC, 74LS125A, Buffer	8020125
	U84	IC, 74LS74, Flip Flop	8020074
	U85	IC, 74LS32, OR Gate	8020032
	U86	IC, 74LS08, AND Gate	8020008
	U87	IC, 74LS38, Buffer8020038	
	U88	IC, 74LS74, Flip Flop	8020074
	U89	IC, 74F04, Hex Inverter	8015004
	U90	IC, 74LS74, Flip Flop	8020074
	U91	IC, 74LS00, NAND Gate	8020000
	U92	IC, 74LS74, Flip Flop	8020074
	U93	IC, 74S260, Dual 5-Input NOR	8010260
	U94	IC, 74LS193, Clock Counter	8020193
	U95	IC, PAL16L8A	8042168
	U96	IC, 74F64, AND/OR Inverter	8015064
	U97	IC, 74F04, Hex Inverter	8015004
	U98	IC, 74LS139, Demultiplexer8020139	
	U99	IC, 74F138,Demultiplexer	8015138
	U100	IC, 74LS161A, Shift Register	8020161
	U101	IC, 74F32, Quad 2-Input OR	8015032
	U102	IC, PAL16L8A	8042168
	U103	IC, PAL16L8A	8042168
	U104	IC, 74LS161A, Shift Register	8020161
	U105	IC, 74LS244, Line Driver	8020244
	U106	IC, 74F08, Quad 2-Input AND	8015008
	U107	IC, 74F32, Quad 2-Input OR	8015032
	U108	IC, 74F00, Quad 2-Input NAND	8015000
	U109	IC, 74F02, Quad 2-Input NOR	8015002
	U111	IC, 74S112, Flip Flop	8010112
	U112	IC, 74F00, Quad 2-Input NAND	8015000
	U113	IC, 74S112, Flip Flop	8010112
	U114	IC, 74F32, Quad 2-Input OR	8015032
	U115	IC, 74F280, Parity Generator	8015280
	U116	IC, 74F373, Octal Latch	8015373
	U117	IC, 74LS244, Line Driver	8020244
	U118	IC, 74LS74, Flip Flop	8020074
	U119	IC, 74LS30, 8-Input NAND	8020030
	U120	IC, 74LS04, Hex Inverter	8020004
	U121	IC, 8272, FDC	8040272

Parts List

Main Logic PCB 8898800, Model 2000

Item	Sym	Description	Part Number
	U122	IC, 74LS04, Hex Inverter	8020004
	U123	IC, 74F08, Quad 2-Input AND	8015008
	U124	IC, 74S112, Flip Flop	8010112
	U125	IC, 74F32, Quad 2-Input OR	8015032
	U126	IC, 74F280, Parity Generator	8015280
	U127	IC, 74F373, Octal Latch	8015373
	U128	IC, 74LS244, Line Driver	8020244
	U129	IC, 75477, Driver	8040477
	U130	IC, 74LS74, Flip Flop	8020074
	U131	IC, 74LS195, Shift Register	8020195
	U132	IC, 74LS123, Multivibrator	8020123
	U133	IC, 74LS02, Quad NOR	8020002
	U134	IC, FDC9216, Data Separator	8040216
	U135	IC, 74LS241, Octal Buffer	8020241
	U136	IC, 74LS32, OR Gate	8020032
	U137	IC, 74LS04, Hex Inverter	8020004
	U138	IC, 7416, Hex Inverter	8000016
	U139	IC, 74LS14, Hex Inverter	8020014
	U140	IC, 7416, Hex Inverter	8000016
	U141	IC, 74LS04, Hex Inverter	8020004
	Y1	Oscillator, 16 MHz	

7.2 Power Supplies

The Model 2000 Microcomputer uses two different power supplies, depending on the configuration of the features incorporated into the unit. The microcomputer which contains two internal floppy disk drives uses a 95W power supply mounted in the Main Unit assembly contained in a metal enclosure. It supplies voltages for the internal systems of the microcomputer.

7.2.1 Main Power Supply #8790056 (95W)

This power supply operates from a 110-120 Vac, 60 Hz input. It may be converted to operate with a 220-240 Vac source if desired. This conversion must be done by a qualified service technician.

The power supply circuit is protected from abnormally high currents by either a 3 amp (for 120 Vac) or 2 amp (for 240 Vac) fuse mounted on the PC board. The power supply is further protected by a circuit which will shut the power supply down if excessively high current (5.1V = 15 amps, +12 or -12V = 8 amps) or low voltage (below 90 Vac for 110-120 volt operation, or 180 Vac for 220-240 Vac operation) is encountered. A "snubber" circuit protects the power supply against excessive voltage spikes.

The AC input is filtered by an EMI (electro-magnetic interference) filter.

The voltage outputs of the main power supply in the Model 2000 are +5 volts, +12 volts, and -12 volts. The outputs are filtered and have over-voltage and under-voltage protection circuits.

7.2.1.1 Technical Specifications

Environment:

Temperature:	Operating	0 to 50C (32-122F)
	Storage	-40 to 85C (-40-185F)
Humidity:	Operating	85% RH @ 35C
	Storage	95% RH @ 35C

Input Voltage:
90 to 135 Vac rms/180 to 270 Vac rms, 47 to 63 Hz

Input Surge Current:
70 amps maximum

Efficiency:
70% minimum at full load with 115 Vac rms input

Output Voltages:
V1, +5.05 Vdc
V2, +12 Vdc
V3, -12 Vdc
V4, +12 Vdc

Output Power:
Continuous 95 watts maximum

Output Current:

		Load	
	Output	Minimum	Maximum
Condition 1	V1	3.5 A	13.25 A
	V2	.25 A	2.1 A
	V3	.005 A	.20 A
	V4	0.0 A	.32 A

Output Ripple Voltage:

V1 (5.05 Vdc)	50 mV p-p
V2 (+12 Vdc)	150 mV p-p
V3 (-12 Vdc)	150 mV p-p
V4 (+12 Vdc)	150 mV p-p

Note: Ripple is the composite 100/120 Hz ripple due to the line, plus the high frequency ripple due to the power oscillator. Common mode noise which may be observed due to oscilloscope connections should be ignored.

Output Voltage Regulation:

After initially setting the output voltages, output voltage tolerances under all conditions of rated line, load, and temperature should remain within the following limits:

V1 (+5.1 Vdc)	+ 3%
V2 (+12 Vdc)	@ 5%
V3 (-12 Vdc)	@8.3%, -25%
V4 (+12 Vdc)	+10%

Over-Current Protection:

V1: Maximum short circuit current is 15 amps.
V2: Maximum short circuit current is 8 amps.
V3: Maximum short circuit current is 8 amps.
V4: Maximum short circuit current is 8 amps.

No damage will result when any output is short circuited continuously with 50 milliohms or less.

Over-Voltage Protection

The +5.1 Vdc circuit is protected with a "crowbar" circuit with a trip range of 5.8 to 6.8 Vdc.

Hold-Up Time at Continuous Max Load:

Nominal Line	16 msec minimum
Low Line	10 msec minimum

7.2.1.2 Troubleshooting The Power Supply

Equipment Required

1. Isolation transformer, 250 VA minimum rating. Dangerously high voltages are present in this power supply. For the safety of the person doing the testing, use an isolation transformer. The 250 VA rating is necessary to keep the AC waveform from being clipped off at the peaks. These power supplies have peak charging capacitors and draw maximum power at the peak of the AC waveform.

2. Variable Transformer (Variac). Use to vary the input voltage. A 10 amp, 1.4 KVA rating is recommended.

3. Voltmeter for measuring DC voltages to 400 Vdc and AC voltages to 150 Vac. Two digital voltmeters are recommended.

4. Oscilloscope with X10 and X100 probes.

5. Ohmmeter

6. Load board with connector. See Figure 1 for a schematic of the load board.

7. 35 Vdc power supply

	Minimum Load	Ohms	Maximum Load	Ohms
+5 Volt	3.5A	1.4	13.5A	0.38
+12 Volt	0.25 A	48	2.1A	5.7
-12 Volt	0.05A	240	0.2A	60

Table 7-6. Load Board Values, 95W Power Supply

Table 1 lists the resistor values required to simulate the minimum load conditions and the maximum load conditions of the 95W Power Supply. The ohms values are measured at the connector and include interconnecting wiring.

The ohms values may be obtained with adjustable resistors or by paralleling several resistors. Be sure the resistors are rated for the current and power they must handle.

The variable resistors must be measured and set when they are hot.

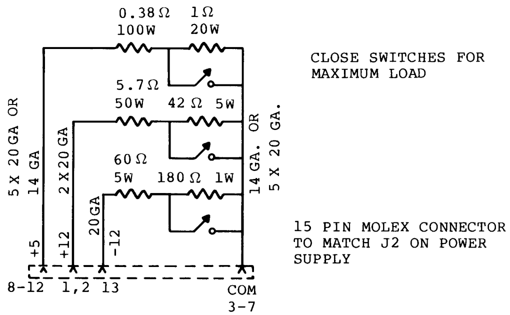


Figure 7-23. Load Box

Figure 7-23 shows recommended resistors and wire sizes for constructing a load box for the 95W Power Supply. The switches can be SPST toggle switches such as Radio Shack's 275-651. All parts can be mounted on an aluminum chassis. Figure 7-24 is a completed load box.

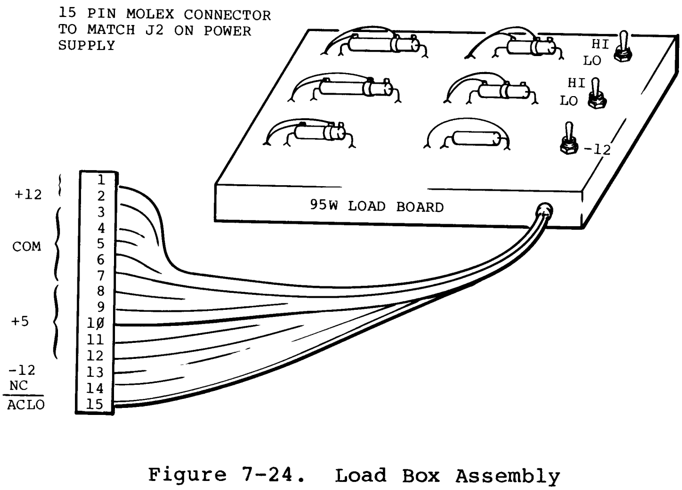


Figure 7-24. Load Box Assembly

Visual Inspection

Remove the power supply from the chassis where it is mounted. Check the power supply for broken, burned, or obviously damaged components. Visually check the fuse. If in doubt, check the fuse with an ohmmeter. Look for overheated or burned areas on the back of the circuit board.

Initial Testing

Connect a +35 volt power source to J3 through two resistors as shown in Figure 7-25. Observe the base of Q15 with the oscilloscope. The waveform should look like Figure 7-26.

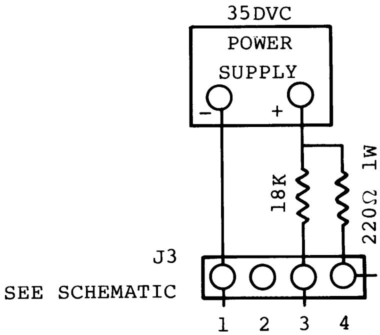


Figure 7-25. Test Circuit

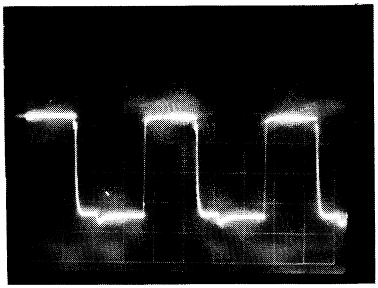
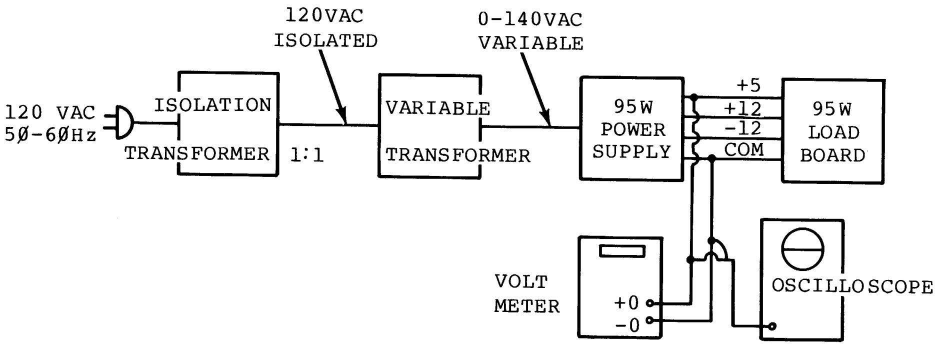


Figure 7-26. Waveform

If it does not, or if no waveform is present, there is a problem with U3 or Q12-15. Do not proceed further until this is repaired. See the No Output section.

Setup Procedure

Set up the test equipment as shown in Figure 7-27. Monitor the AC input voltage and the regulated +5 volt output. Use 50 mV/div. sensitivity and AC coupling on the oscilloscope. Load the 95W Power Supply with its minimum load as specified in Table 7-6. Bring the AC input voltage up slowly with the variable transformer while monitoring the +5 volt output with the oscilloscope and voltmeter. The supply should start with approximately 90 Vac applied and should regulate at +5 Vdc. If the output has reached +5 volts, do a performance test as shown in Paragraph 7.2.1.3.



BE SURE THE INPUT VOLTAGE JUMPER IS CONNECTED FROM E8 TO E9.

Figure 7-27. Test Equipment Setup

No Output

If the power supply does not produce correct output voltages, one or more components have failed. A No Output condition is most likely caused by a shorted or open component in the primary circuitry but may also be caused by a fault in the secondary circuitry.

A. Check the fuse and replace if necessary.

B. Check for shorts and opens in the primary circuit semiconductors. Check the diode bridge BR1, power transistors Q12-15, and catch diode CR11 for shorted junctions. A shorted junction will measure zero ohms in-circuit. Replace any shorted components.

C. Check for shorts and opens in the secondary circuit. Use an ohmmeter to measure from each output to secondary common with the output loads disconnected. Look for shorted rectifiers and capacitors. If the +12 volt output is shorted, also check crowbar SCR Q6.

D. Check the primary DC with the fuse intact. Connect a 35 Vdc power supply to J3 as shown in Figure 3. Start with the variable transformer set to 0 Vac. Monitor the DC voltage from Pin 1 of T1 to primary common. With an input of 95 Vac, there should be about 260 Vdc. If not, check the fuse, rectifier BR1, and thermistors RT1 and RT2.

E. Check Q15 waveforms Look for base drive on the base of Q15 (see Figure 6). The transistor should be switching. Check the collector waveform with a X100 probe (see Figure 7). If base drive is missing, check pin 8 of U3 (see Figure 8). See if U3 has +16 Vdc on pin 10. Check the chip oscillator on pin 5 (see Figure 9).

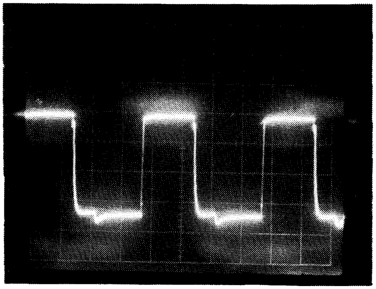


Figure 7-28. Base of Q15

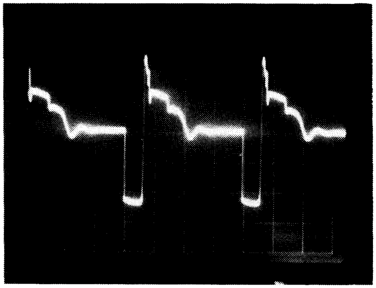


Figure 7-29. Q15 Collector Waveform

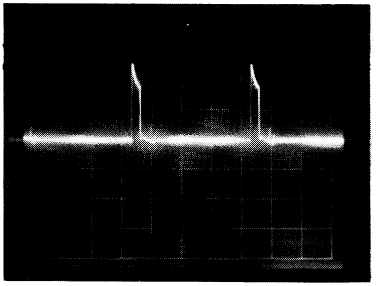


Figure 7-30. Waveform of U3, Pin 8

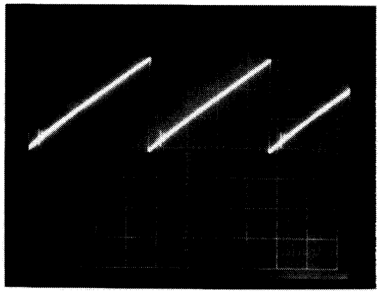


Figure 7-31. Chip Oscillator, Pin 5

Low Outputs

A. All Outputs Are Low. If all outputs are low, check that the voltage selection jumper is in the proper position.

B. +5 Volt Output. The power supply regulates the +5 volt output directly. If the +5V adjustment, R10, is not set correctly, the other outputs will be too high or too low.

7.2.1.3 Performance Test

The following specifications should be met when the power supply is operated under minimum and maximum loads and input voltages.

Output	Min	Max	Ripple(max)
+5.1V	4.95	5.25	50 mV p-p
+12 V	12.36	12.36	150 mV p-p
-12 V	11	15	150 mV p-p

Apply 115 Vac to the line input. Measure the +5.1 V output under full loading. Adjust R10 for a reading between 5.05 and 5.15 volts. Measure the +12.0 volt output under full loading. Adjust R8 for a reading between 11.95 and 12.15 volts.

7.2.1.4 System Description

Basic Principle

A switching power supply circuit employs a high-speed semiconductor switch to control the storage and release of electrical energy in an inductor and provide regulated DC output voltages with a minimum loss of energy in heat-dissipating elements. There are several schemes for achieving this result which differ primarily in the arrangement of the basic circuit elements. These elements include a switch, an inductor, a rectifier, a capacitor and a DC voltage source.

An arrangement well-suited for economical power supplies with rated power outputs under 100 watts is the FLYBACK CONVERTER shown in Figure 7-32. The waveforms in Figure 7-33 are used to describe the operation of the Flyback Converter circuit. For the purpose of this discussion, we will assume that the duration of the "ON" time equals the duration of the "OFF" time.

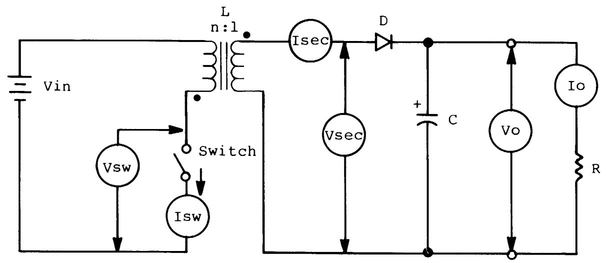


Figure 7-32. Basic Flyback Converter

When the switch is closed (ON) at time ta, Vin is impressed across the primary winding of inductor L and the current Isw increases linearly from zero until the switch opens (OFF) at time tb. Note that Isec is zero while the switch is closed. This is because Vsec is negative with respect to Vo, thus reverse-biasing diode D. Note that Vsw is also zero while the switch is closed.

When the switch opens at time tb, the magnetic field of L instantly collapses and reverses polarity. At this moment, Vsw is equal to Vin plus the voltage across L just before the switch opened (also equal to Vin). Therefore, at the instant the magnetic field reverses polarity, Vsw = 2Vin.

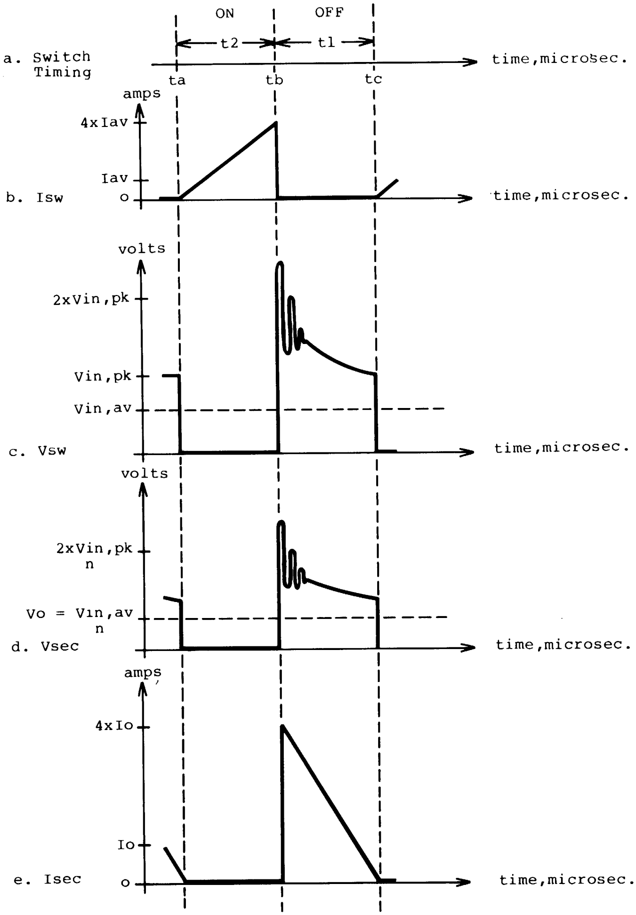


Figure 7-33. Waveforms for Figure 7-32

During the interval when the switch is open (tb to tc), thesecondary voltage, Vsec, is a replica of the primary voltage Vsw. Diode D is now forward biased due to the polarity of the inductor windings and because the turns ratio, n, is such that:

$$Vsec \times n > Vo$$

This biasing replenishes the charge in capacitor C that was delivered to the load R during the ta-tb interval. This is the "flyback" interval and is so named because the inductor releases the energy stored in its magnetic field while the switch is OFF.

Several other facts are illustrated by the waveforms of Figure 7-33. First, the voltage Vsw across the switch decays exponentially from 2Vin to Vin during the "OFF" interval. This is because the inductor and the switch timing are adjusted to transfer all of the energy that was stored in the inductor while the switch was ON into the secondary while the switch is OFF. (Observe that Isec DECREASES linearly with time to zero at the end of the "OFF" time period.) This is known as resetting the core. Thus, at time tc when the switch is ready to turn on again, the DC input voltage Vin is again available to charge the inductor. Also at this time, all currents in the inductor are zero.

Second, since we have assumed that Isw increases linearly with time and that the ON and OFF time periods are equal (50% duty cycle), the average current in the primary, Isw (av), is 1/4 the peak current Isw. Also, the average current in the secondary, which is equal to the load current Io, is 1/4 the peak current in the secondary.

Third, the turns ratio is set by the ratio of the average primary voltage (Vsw) over a full cycle at its lowest value to the maximum permissible output voltage, Vo. The lowest Vsw value occurs at low AC line and maximum output load. In practice, the actual turns ratio, the ratio of peak-to-average voltages and currents, and the duty cycle may be adjusted to compensate for circuit losses.

Fourth, notice the ringing or oscillation that appears on the peak portion of Vsw and Vsec. This oscillation occurs at the resonant frequency of the leakage inductance of the inductor L and the parasitic capacitance of the circuit. The parasitic capacitance includes the interwinding capacitance of the inductor and stray capacitance of the switch. If this oscillation is not damped by a suitable means, the peak voltages may easily exceed the breakdown rating of the switch or the insulation of the inductor.

Block Diagram

The basic circuit illustrated in Figure 7-34 can be divided into three functional blocks: Input DC supply, primary, and secondary. To make use of this model, we need to expand it to provide control for the switch timing and to include sufficient circuitry to satisfy performance and reliability.

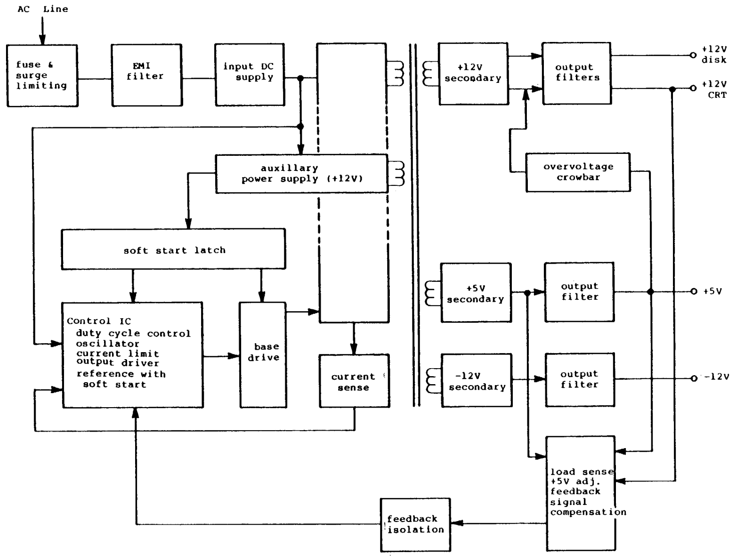


Figure 7-34. Block Diagram.

The other blocks provide additional output voltages, add safety or protective features, reduce circuit noise, and develop signals for use by the control section. The control section continuously operates the bipolar transistor switch and varies the proportion of ON time to OFF time in response to changes in the AC input line voltage or output load current. This is accomplished by feeding back a signal from the output terminals that instructs the control section to increase or decrease the ON time to compensate for a change in the output voltage.

The DC voltage supply to the control section is controlled by the latch circuit when AC power is first applied to the power supply. A built-in timing circuit allows the input DC supply filter capacitor to become fully charged before power is appliea to the control section. After the control section circuit starts and secondary voltages reach their regulated output levels, the auxiliary power supply provides the required DC voltage to operate the control seciton. The latch is reset when the current limit or under-voltage sensors operate, thus removing DC voltage to the Control IC.

There are three secondary or output voltages in addition to the auxiliary supply: +5.1 volt, +12 volt, and -12 volt. The +5.1 and +12 voltages are regulated by the control circuit response to the frequency compensated feedback control signal which comes from the load sense section. Since the load sensing occurs on the secondary side, an optical coupler circuit is necessary to provide safety isolation between the primary side common ground and the secondary side common ground.

All the secondary voltages, including the auxiliary +12 volts, share the same magnetic flux linkage in the transformer core and are controlled by the flyback inductor. Any change in secondary load currents causes a change in the shared magnetic flux. This change in the flux of the inductor sets up an EMF (electromotive force) which causes a flux in opposition to the one which resulted from the change in load current. Thus, the original change tends to be counteracted and the current delivered to the load remains constant.

The output filters reduce the remaining ripple voltage components of the AC line and switching frequencies to levels low enough to prevent interference with the circuits operated by the supply. Switching frequency components conducted through the AC input terminals are suppressed by the EMI filter to avoid interference with other equipment connected to the power line.

The overvoltage crowbar senses an abnormal rise in the +5.1 volt output and short-circuits the voltage line to the common secondary ground, thus tripping the current limiting circuit which finally shuts down the supply.

The surge limiter at the AC line input prevents the input filter capacitor in-rush current surge from exceeding component ratings or unnecessarily tripping external fuses.

7.2.1.5 Theory of Operation
Power Supply Assembly 8790056 (95W Tandy)

PRIMARY CIRCUITS

The input AC is fed through an EMI filter (C33-C36, C41, and T2) before being fed to the rectifier. A bridge rectifier and filter capacitors are connected directly across the AC line to provide the DC input voltage to the power supply. For 115V operation, a jumper from E8 to E9 converts the rectifier to voltage-doubler operation. The power supply fuse, a 3 ampere (120V) or 2 ampere (240V), protects the power supply against abnormally high currents.

Auxiliary Power Supply

The auxiliary power supply (winding 9-10 on T1, half-wave rectifier CR9, and filter C37) supplies power to U3 and the base drive circuitry of Q15. The voltage output is approximately +15 volts but surges to +31 volts during start-up.

Kick-Start Latch

Start-up of the circuit is initiated by the kick-start latch. When power is first applied, C37 starts charging through R42. When the voltage on C37 reaches 31 volts, zener diode CR10 conducts, turning on Q10 which then turns on Q11. With Q11 on, Q10 is held on and the power in C37 is delivered to U3 and the base drive circuitry for Q15. Q15 starts switching and the auxiliary power supply comes on to deliver +15 volts to C37.

Control Section

U2, U3, and Q12-14 make up the control section. U3 has three major functions: (1) an internal voltage reference, (2) a pulse generator, and (3) an error amplifier. The internal reference on pin 12 is +5.0 Vdc. This provides the reference for the comparators and the power for the photo transistor in U2.

The pulse generator frequency is controlled by R37 and C27. The generator output is on pins 8 and 9 and is a square wave that controls Q15.

The comparator inputs on pins 1 and 2 sense the propervoltage regulation by comparing +5 volts on pin 2 to the voltage on pin 1 coming from U2. The other comparator inputs on pins 13 and 14 detect faulty operating conditions. Pin 13 is compared to the +5 volts on pin 14 and the pulse generator will stop if pin 13 falls below +5 volts.

Base Drive

The output transistor U3 forms a Darlington pair with Q14 to provide the necessary drive current through C29 to turn on Q15. Q12 and Q13 are biased on during turn-off to cause Q15 to turn off faster.

Current Limit

Transistors Q8 and Q9 form the current limiting latch. R44 is the current sense resistor. Excess current through Q15 and R44 will cause the voltage across R44 to exceed 0.6 volts, turning on Q9. This then turns on Q8, holding on Q9 and pulling pin 13 of U3 below the +5 Vdc reference on pin 14, causing the oscillator in U3 to stop.

Under-Voltage Lockout

Resistors R24 and R26 form a voltage divider from the input DC to ground. The voltage from the divider goes to pin 13 of U3. If the AC input voltage drops below 90 Vac (180 Vac for 230 V operation), the voltage at pin 13 will drop below the +5 volt reference on pin 14, causing the oscillator to stop.

Snubber

CR11, R45, C38, and C39 provide snubbing to prevent excessive voltage spikes from developing across Q15 during the flyback of T1 when Q15 is biased off.

SECONDARY CIRCUITS

Secondary Outputs

There are three separate secondary output voltages: +5 volts, +12 volts, and -12 volts.

The +5 volts comes from two paralleled windings, each feeding two paralleled rectifiers (CR13-CR14) for improved current handling and heat sinking. A pi-section filter, formed by C6, C10, C11, C12, L2, and C9 filters the +5 volts. R9, C7, R16, and C13 are snubbers to protect the low voltage diodes CR13 and CR14 against transients.

The +12 volts is rectified by CR2 and filtered by a pi-section filter formed by C8, L1, and C42. Transistors Q1 and Q2 and the saturable reactor L3 provide improved 12 volt regulation with varying output loading conditions.

The -12 volts is rectified by CR4 and filtered by a pi-section filter formed by C21, L4, and C20. U5 provides the -12 volt regulation and CR3 and CR12 protect U5 aga|?$@ reverse voltages.

Load Sense And Feedback Development

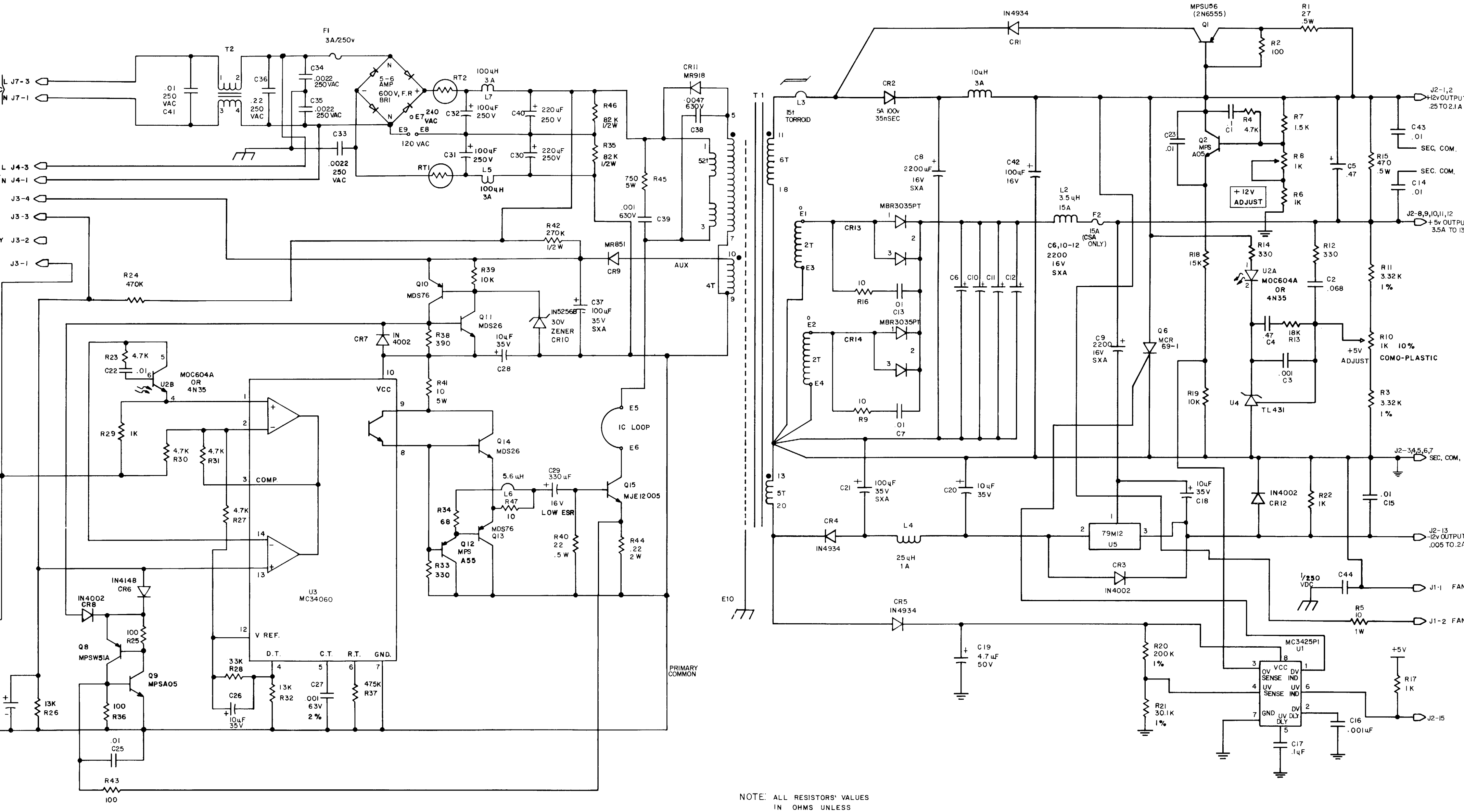
U2 is an opto coupler, containing one light-emitting diode and one phototransistor. The phototransistor controls a comparator in U3 as discussed previously in the Control Section. The LED is controlled by Q3 which senses the +5 volts through a resistive divider that includes R10. this is the regulating feedback path from the secondary circuitry to the primary circuitry.

Overvoltage Crowbar

To prevent the +5 volts from exceeding a safe level, SCR Q6 "crowbars" or short circuits the +5 volt output. This energizes the current limiting circuit in the primary circuitry and the oscillator stops. Q6 is controlled by U11.

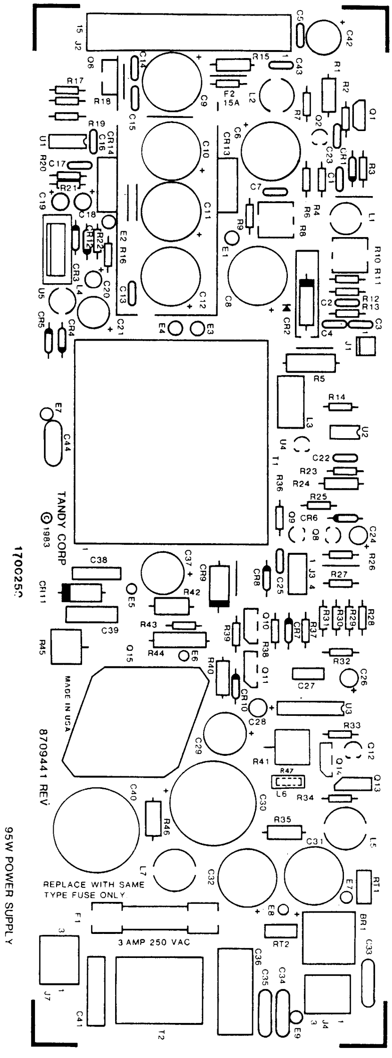
UV And OV Sense

U1 provides UV (under voltage) and OV (over voltage) sense. CR5 conducts during the forward conduction of T1, providing power for U1 and a UV sense signal from R20 and R21. This UV sense provides a TTL UV AC LOW* on pin 6, fully isolated from the primary circuitry. R18 and R19 generate the OV sense signal for U1 pin3 and this controls Q6 via pin 1 of U1.

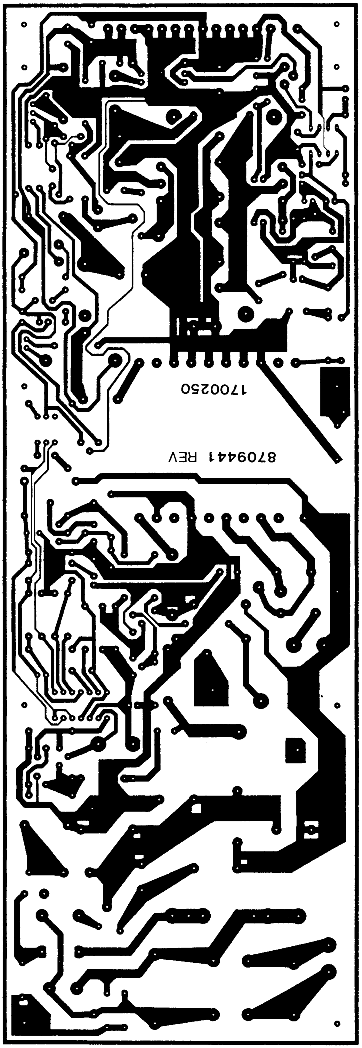


Schematic 8000213, 95W Power Supply

Schematic 8000213, Power Supply Assembly 8790056 (95W)



Power Supply Component Layout 1700250, PCB Assembly 8790056



Circuit Trace 1700250, 95W Power Supply 8790056

Parts List

Power Supply Assembly 8790056 (95W Tandy)

Item	Sym	Description	Part Number
1	1	Printed Circuit Board	8709441
2	1	Bracket, Heatsink (CR13,14)	8729229
3	1	Heatsink, Diode (CR2)	8729227
4	1	Heatsink, Transistor (Q1)	
5	1	Heatsink, Transistor (Q7)	8549026
6	1	Heatsink, Transistor (Q15)	8549021
7	1	Mount, Transistor (Q15)(with studs)	8549022
8	1	Insulator, TO-3, Cond. Rubber (Q15)	8539043
9	1	Label, DANGER High Voltage	8789889
10	1	Label, CAUTION-Heat Sink	8789888
11	1	Label, Serial Number	8789999
12	2	Screw, #4-40 x 3/8" (Q4,5)	8569002
13	2	Washer, #4 Split Lock (Q4,5)	8589021
14	1	Nut, #4-40 KEPS (Q6)	8579003
15	2	Nut, #6-32 KEPS(Q13, 14)	8579004
16	1	Current Loop, E5 to E6	8433201
17	2	Tab, .110" Faston (E7,8)	8529044
18	1	Jumper, With .110" Faston Connector	8432020
19	1	Socket, IC (U1)	8509011
20	1	Socket, IC (U2)	8509015
21	1	Socket, IC (U3)	8509008
22	2	Clip, Fuse (F1)	8559058
23	2	Nut, #6-32 Zinc Plated (Q15)	8579034
24	1	Screw, #4-40 x 1/4" PPH (Q6)	8569031
25	2	Screw, #6-40 x 1/4" (CR13,14)	8569098
26	1	Washer, Shoulder (Q6)	8589026
	C1	Capacitor, .100 mfd, 63V 10% Metal	8394104
	C2	Capacitor, .068 mfd, 63V 10% Metal	8393684
	C3	Capacitor, .001 mfd, 50V 20% Mtl	8392014
	C4	Capacitor, .47 mfd, 35V 10% Tant	8334474
	C5	Capacitor, .47 mfd, 35V 10% Tant	8334474
	C6	Capacitor, 2200 mfd, 16V 20% Radial	8328221
	C7	Capacitor, .01 mfd, 63V 20% Metal	8393104
	C8	Capacitor, 2200 mfd, 16V 20% Radial	8328221
	C9	Capacitor, 2200 mfd, 16V 20% Radial	8328221
	C10	Capacitor, 2200 mfd, 16V 20% Radial	8328221
	C11	Capacitor, 2200 mfd, 16V 20% Radial	8328221
	C12	Capacitor, 2200 mfd, 16V 20% Radial	8328221
	C13	Capacitor, .01 mfd, 63V 20% Metal	8393104

Parts List

Power Supply Assembly 8790056 (95W Tandy)

Item	Sym	Description	Part Number
	C14	Capacitor, .01 mfd, 63V 20% Metal	8393104
	C15	Capacitor, .01 mfd, 63V 20% Metal	8393104
	C16	Capacitor, .001 mfd, 50V 20% Mtl	8392014
	C17	Capacitor, .100 mfd, 63V 10% Metal	8394104
	C18	Capacitor, 10 mfd, 35V 20% Radial	8326103
	C19	Capacitor, 4.7 mfd, 50V 20% Radial	8325474
	C20	Capacitor, 10 mfd, 35V 20% Radial	8326103
	C21	Capacitor, 100 mfd, 35V 20% Radial	8327103
	C22	Capacitor, .01 mfd, 63V 20% Metal	8393104
	C23	Capacitor, .01 mfd, 63V 20% Metal	8393104
	C24	Capacitor, 10 mfd, 35V 20% Radial	8326103
	C25	Capacitor, .01 mfd, 63V 20% Metal	8393104
	C26	Capacitor, 10 mfd, 35V 20% Radial	8326103
	C27	Capacitor, .001 mfd, 63V 2% Poly	8392104
	C28	Capacitor, 10 mfd, 35V 20% Radial	8326103
	C29	Capacitor, 330 mfd, 16V 20% Radial	8327331
	C30	Capacitor, 220 mfd, 250V 20% Radial	8327227
	C31	Capacitor, 100 mfd, 250V 20% Radial	8327106
	C32	Capacitor, 100 mfd, 250V 20% Radial	8327106
	C33	Capacitor, 2200 pfd, 250V Cer Disk	8302226
	C34	Capacitor, 2200 pfd, 250V Cer Disk	8302226
	C35	Capacitor, 2200 pfd, 250V Cer Disk	8302226
	C36	Capacitor, .22 mfd, 250V 20% Met	8394226
	C37	Capacitor, 100 mfd, 35V 20% Radial	8327103
	C38	Capacitor, .0047 mfd, 630V 10% Poly	8392477
	C39	Capacitor, .001 mfd, 630V 10% Poly	8392017
	C40	Capacitor, 220 mfd, 250V 20% Radial	8327227
	C41	Capacitor, .01 mfd, 250V 20% Met	8393106
	C42	Capacitor, 1000 mfd, 16V 20% Radial	8328102
	C43	Capacitor, .01 mfd, 63V 20% Metal	8393104
	C44	Capacitor, .1 mfd, 250V 20% Metal	8394106
	CR1	Diode, 1N4934	8150934
	CR2	Diode, 5 Amp, 35 nsec	8160050
	CR3	Diode, 1N4001	8150001
	CR4	Diode, 1N4934	8150934
	CR5	Diode, 1N4934	8150934
	CR6	Diode, 1N4148 (Switching)	8150148
	CR7	Diode, 1N4001	8150001
	CR8	Diode, 1N4001	8150001
	CR9	Diode, MR851	8160851
	CR10	Diode, 1N5256B, Zener	8150256

Parts List

Power Supply Assembly 8790056 (95W Tandy)

Item	Sym	Description	Part Number
	J1	Connector, 2 Pin Vertical	8519214
	J2	Connector, 15 PIn	8519194
	J3	Connector, 4 Pin	8519163
	J4	Connector, 3 Pin	8519153
	J5	NA	
	J6	NA	
	J7	Connector, 3 Pin	8519153
	L1	Inductor, 10 uH, 3A 10%	8419007
	L2	Inductor, 3.5 uH, 15A 10%	8419032
	L3	Inductor, Torroid	8419036
	L4	Inductor, 25 uH, 1A 10%	8419034
	L5	Inductor, 100 uH, 3A 10%	8419009
	L6	Coil, 5.6 uH, 10%	8419037
	L7	Inductor, 100 uH, 3A 10%	8419009
	Q1	Transistor, 2N6555, PNP, 1A 80V	8100555
		Transistor, MPS-U56, PNP, .6A 40V	8100056
	Q2	Transistor, MPSA05, NPN, 40V	8110005
	Q3	NA	
	Q4	NA	
	Q5	NA	
	Q6	SCR, MCR69-1, 25A 50PIV	8140691
	Q7	IC, 79M12, Voltage Regulator	8050912
	Q8	Transistor, MPSW51A, PNP, 1A 40V	8101051
	Q9	Transistor, MPSA05, NPN, 40V	8110005
	Q10	Transistor, MDS76, PNP, 3A 40V	8100076
	Q11	Transistor, MDS26, NPN, 3A 40V	8100026
	Q12	Transistor, MPSA55, PNP, .6A 40V	8100055
	Q13	Transistor, MDS76, PNP, 3A 40V	8100076
	Q14	Transistor, MDS26, NPN, 3A 40V	8100026
	Q15	Transistor, MJE12005, NPN, 8A 1500V	8111005
	R1	Resistor, 27 ohm, 1/2W 5%, CF	8217027
	R2	Resistor, 100 ohm, 1/4W 5%, CF	8207110
	R3	Resistor, 3.32 kohm, 1/4W 1%, MF	8200232
	R4	Resistor, 4.7 kohm, 1/4W 5%, CF	8207247
	R5	Resistor, 10 ohm, 1W 5%, CF	8247616
	R6	Resistor, 1 kohm, 1/4W 5%, CF	8207210
	R7	Resistor, 1.5 kohm, 1/4W 5%, CF	8207215
	R8	Potentiometer, 1 kohm, 20%	8279211
	R9	Resistor, 10 ohm, 1/4W 5%, CF	8207010

Parts List

Power Supply Assembly 8790056 (95W Tandy)

Item	Sym	Description	Part Number
	R10	Potentiometer, 1 kohm, 20%	8279211
	R11	Resistor, 3.32 kohm, 1/4W 1%, MF	8200232
	R12	Resistor, 330 ohm, 1/4W 5%, CF	8207133
	R13	Resistor, 18 kohm, 1/4W 5%, CF	8207318
	R14	Resistor, 330 ohm, 1/4W 5%, CF	8207133
	R15	Resistor, 470 ohm, 1/2W 5%, CF	8217147
	R16	Resistor, 10 ohm, 1/4W 5%, CF	8207010
	R17	Resistor, 1 kohm, 1/4W 5%, CF	8207210
	R18	Resistor, 15 kohm, 1/4W 5%, CF	8207315
	R19	Resistor, 10 kohm, 1/4W 5%, CF	8207310
	R20	Resistor, 200 kohm, 1/4W 1%, MF	8200420
	R21	Resistor, 30.1 kohm, 1/4W 1%, MF	8200330
	R22	Resistor, 1 kohm, 1/4W 5%, CF	8207210
	R23	Resistor, 4.7 kohm, 1/4W 5%, CF	8207247
	R24	Resistor, 470 kohm, 1/2W 5%, CF	8217447
	R25	Resistor, 100 ohm, 1/4W 5% CF	8207110
	R26	Resistor, 13 kohm, 1/4W 5%, CF	8207313
	R27	Resistor, 4.7 kohm, 1/4W 5%, CF	8207247
	R28	Resistor, 33 kohm, 1/4W 5%, CF	8207333
	R29	Resistor, 1 kohm, 1/4W 5%, CF	8207210
	R30	Resistor, 4.7 kohm, 1/4W 5%, CF	8207247
	R31	Resistor, 4.7 kohm, 1/4W 5%, CF	8207247
	R32	Resistor, 13 kohm, 1/4W 5%, CF	8207313
	R33	Resistor, 330 ohm, 1/4W 5%, CF	8207133
	R34	Resistor, 68 ohm, 1/4W 5%, CF	8207068
	R35	Resistor, 82 kohm, 1/2W 5%, CF	8217382
	R36	Resistor, 100 ohm, 1/4W 5% CF	8207110
	R37	Resistor, 47.5 kohm, 1/4W 1%, MF	8200347
	R38	Resistor, 390 ohm, 1/4W 5% CF	8207139
	R39	Resistor, 10 kohm, 1/4W 5%, CF	8207310
	R40	Resistor, 22 ohm, 1/2W 5%, CF	8217022
	R41	Resistor, 10 ohm, 5W 5%, WW	8248010
	R42	Resistor, 270 kohm, 1/2W 5%, CF	8217427
	R43	Resistor, 100 ohm, 1/4W 5%, CF	8207110
	R44	Resistor, .22 ohm, 2W 5%, MOF	8248022
	R45	Resistor, 750 ohm, 5W 5%, WW	8248175
	R46	Resistor, 82 kohm, 1/2W 5%, CF	8217382
	R47	Resistor, 10 ohm, 1/4W 5%, CF	8207010
	RT1	Thermistor, 10 ohm @ 25C, Coated	8298010
	RT2	Thermistor, 10 ohm @ 25C, Coated	8298010

Parts List

Power Supply Assembly 8790056 (95W Tandy)

Item	Sym	Description	Part Number
	T1	Transformer, Power, 95W Flyback	8790057
	T2	Choke, Common Mode, 1.24 mH/Side	8790058
	U1	IC, MC3425P, Voltage Protector	8050425
	U2	IC, 4N35, Optoisolator	8170035
	U3	IC, MC34060, Switching Regulator	8060060
	U4	IC, TL431, Positive Shunt Regulator	8060428

7.2.2 Auxiliary Power Supply #8790025 (38W, Hard Disk Drive Only, Astec AA11330)

When the microcomputer is equipped with a built-in hard disk drive, an additional 38W power supply is required to supply voltage to the hard disk drive only. This supply delivers approximately +15 volts in normal operation, but surges to +31 volts durin@ start-up. It is contained in the same housing as the @5W power supply in the Main Unit of the computer.

7.2.2.1 Troubleshooting the Power Supply

Equipment for Test Set Up

1. Isolation Transformer (Minimum of 500 VA rating)

CAUTION

Dangerously high voltages are present in this power supply. For the safety of the individual doing the testing, please use an isolation transformer. The 500 VA rating is needed to keep the AC waveform from being clipped off at the peaks. These power supplies have peak charging capacitors and draw full power at the peak of the AC waveform.

2. 0-280 Variable Transformer (Variac)
   Used to vary input voltage. Recommend 10 Amp, 1.4 KVA rating minimum.

3. Voltmeter
   Needed to measure DC voltages to 50 VDC and AC voltages to 400 Vac. Recommend two digital multimeters.

4. Oscilloscope
   Need X10 probe.

5. Load Board with Connectors
   See Table 7-7 for values of loads required. The entries on the table for Safe Load Power is the minimum power ratings for the load resistors used.

6. Ohmmeter

7. Wattmeter

Setup Procedure

Set up as shown in Figure 7-35. You will want to monitor the input voltage and the output voltage of the regulated bus, which is the +5 Volt output with DVMs. Also monitor the +5 Volt output with the oscilloscope using 50 mv/division sensitivity. The DVM monitoring the +5 Volt output can also be used to check the other outputs. See text under NO OUTPUT for test points within power supply.

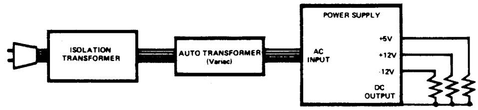


Figure 7-35. Test Setup

Visual Inspection

Check power supply for any broken, burned, or obviously damaged components. Visually check fuse. If there is any question, check with an ohmmeter.

OUTPUT	MIN LOAD	LOAD R	SAFE LOAD POWER	MAX LOAD	LOAD R	SAFE LOAD POWER
+5	0.45A	11.11 ohm	5W	2.5A	2 ohm	25W
+12	0.3A	0.40 ohm	8W	2.02A	24.24 ohm	50W
-12	0	0	0	0	120 ohm	2W

Table 7-7. Load Board Values

Start-Up

First note the position of the input voltage select wire. This wire can be found at the end of the PCB opposite the input/output connectors. Make sure that the jumper wire is in the proper voltage location.

Load the power supply with minimum load as specified in Table 7-7. Bring power up slowly with the variable transformer while monitoring the +5 Volt output with the scope and DVM and the input with a DVM and wattmeter. If the wattmeter shows significant power with low AC power being applied, shut down and refer to section following on NO OUTPUT. The supply should start with approximately 80-120 Vac applied and should regulate when 95 Vac is applied. If the output has reached +5 volts, do a performance test as shown in PERFORMANCE TEST which follows.

NO OUTPUT

1. Check Fuse. If the fuse is blown, replace it but do not apply power until the cause of failure is found.

2. Preliminary Check On Major Primary Components. Check thermistor (R1), diode bridge (DB1), power transistor (Q2), and catch diode (D3), turn-off transistor (Q1), emitter resistor (R10), and diode (D1) for shorted junctions. If any component is found shorted, replace it.

3. Preliminary Check On Major Secondary Components. Using an ohmmeter from output common to each output (with output loads disconnected), check for shorted rectifiers or capacitors. If +12 volt output is shorted, also check crowbar SCR (SCR1) and zener (Z1).

4. Check For B+. Set up power supply and attach X10 scope probe ground to end of R11 closest to input capacitors. Slowly turn up power and check for B+ on the (+) terminal of the diode bridge (DB1). With the input at 95 Vac, this point should be 120-140 Vdc. If this is not measured, check the fuse, thermister (R1), DB1, R2, D3, and input capacitors C6 and C7.

5. Check Q2 Waveforms. Using X10 probe on the case of T03 package of Q2, check the collector waveform. The transistor should be switching, with the correct waveform shown in Figure 7-36. If this is not present, check for a shorted junction on Q2.

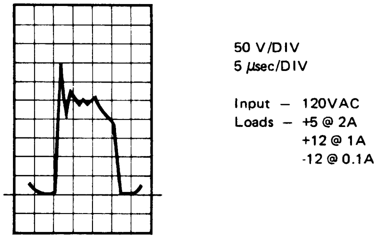


Figure 7-36. Q2 Collector Waveform

If OK, check the base waveform as shown in Figure 7-37. The base of Q2 is the uppermost of the two center leads on the back of Q2 heat sink. If this waveform is not present, check L3, Q1, and D1, secondary components Q3, D11, D12, D5, and L4. If any of the semiconductors is found shorted or if an inductor is open, replace it.

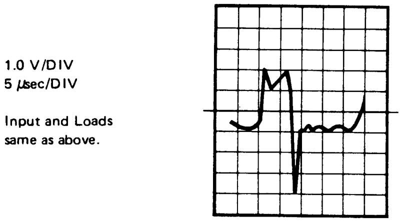


Figure 7-37. Q2 Base Waveform

Performance Test

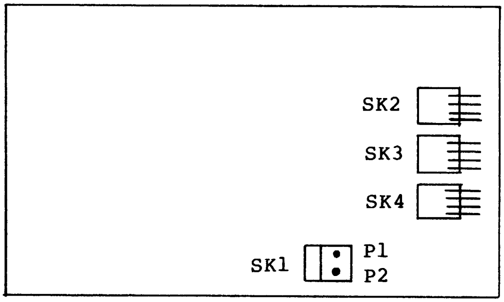
Each of the test conditions noted below should be set up and results noted to be within the limits specified.

Test	Input	+5 Load	+12 Load	-12 Load
1	95VAC	Max	Max	Max
2	128VAC	Max	Max	Max
3·	120VAC	Max	Min	Min
4	128VAC	Min	Min	Min
5	95VAC	Min	Min	Min

VOLTAGE AND RIPPLE SPECIFICATION				
OUTPUT	MIN	MAX	NO LOAD	RIPPLE
+5	4.75V	5.25V		50mV P-P
+12	11.40V	12.60V		150mV P-P
-12	11.00V	15.00V		150mV P-P

* Applies to resistive load only. Not under system operating conditions.

Table 7-8. Performance Tables

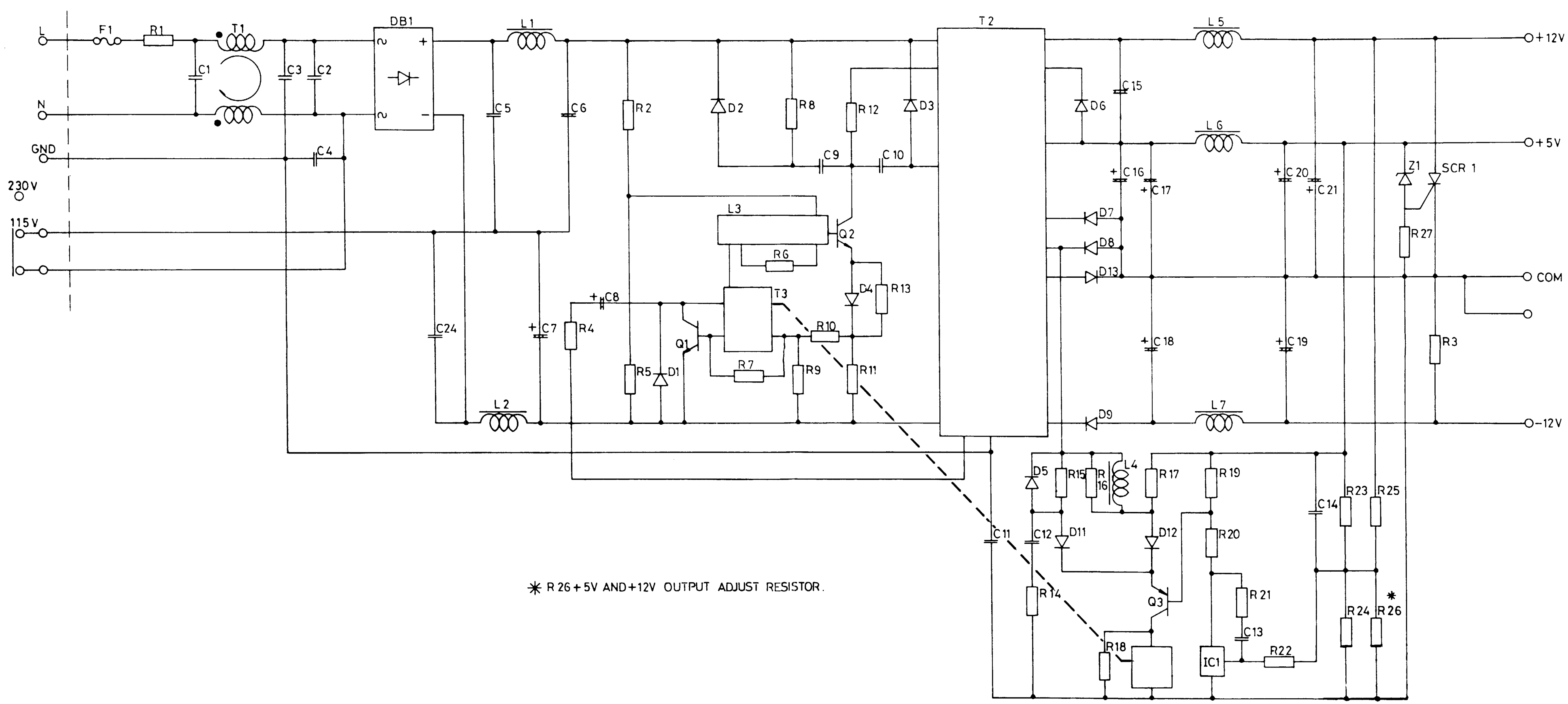


For SK1
P1 - Neutral
P2 - Line

For SK 2,3,4
P1 - -12V 0.1A Max.
P2 - +12V 2.02A Max.
P3 - Common
P4 - +5V 2.5A Max.

Figure 7-38. Power Pin Assignments

R	R1 R4 R2 R5 R6—R13 R14—R18 R19—R27 R3
C	C1 C2,3,4 C24 C5 C6,7,8 C9 C10 C11 C12 C13—C21
L/T	T1 L2 L1 T3 L3 T2 L4—L7
Q/D	D1 Q1 D2 Q2 D4 D3 D5—D9 D11—D13 Q3
MISC	F1 DB1 IC1 Z1 SCR 1



Schematic, Power Supply 8790025 (Astec AA11330)

Schematic, Power Supply 8790025 (Astec AA11330)

Parts List

Power Supply 8790025 38W (Astec AA11330)

Item Sym	Description	Part Number
C1	Capacitor, .01 mfd, 250V 20%	068-10300010
C2	Capacitor, .1 mfd, 250V 20%	068-10400010
C3	Capacitor, 4700 pfd, 400V 20% Cer	055-47220001
C4	Capacitor, 4700 pfd, 400V 20% Cer	055-47220001
C5	Capacitor, .22 mfd, 250V 20% Poly	058-22400130
C6	Capacitor, 100 mfd, 250V 20% Elec	057-10120170
C7	Capacitor, 100 mfd, 250V 20% Elec	057-10120170
C8	Capacitor, 220 mfd,10V +50/-10 Elec	057-22120080
C9	Capacitor, 470 pfd, 2KV 10%, Cer	055-47154426
C10	Capacitor, .01 mfd, 1KV 20%, Cer	055-10368925
C11	Capacitor, .01 mfd, 1KV 20%, Cer	055-10368925
C12	Capacitor, .22 mfd, 100V 20% Poly	058-22400160
C13	Capacitor, .022 mfd, 50V 20% Poly	058-22300090
C14	Capacitor, .22 mfd, 100V 20% Poly	058-22400160
C15	Capacitor, 1000 mfd, 25V Elec	057-10220040
C16	Capacitor, 1000 mfd, 25V Elec	057-10220040
C17	Capacitor, 1000 mfd, 25V Elec	057-10220040
C18	Capacitor, 330 mfd, 16V Elec	057-33120120
C19	Capacitor, 330 mfd, 16V Elec	057-33120120
C20	Capacitor, 470 mfd, 25V Elec	057-47120110
C21	Capacitor, 2200 mfd, 16V Elec	057-22220020
C22	Not Used	
C23	Not Used	
C24	Capacitor, .22 mfd, 250V 20%	058-22400130
D1	Rectifier, RGP10A	226-10400050
D2	Rectifier, RGP10J	226-10400060
D3	Rectifier, RGP10M	226-10400100
D4	Rectifier, 1N4001GP	226-10400080
D5	Silicon Diode, 1N4606	212-10700210
D6	Rectifier Assembly	853-00200190
D7	Rectifier Assembly	853-00200190
D8	Rectifier Assembly	853-00200190
D9	Rectifier, RGP10B	226-10400070
D10	Not Used	
D11	Silicon Diode, 1N4606	212-10700210
D12	Silicon Diode, 1N4606	212-10700210
D13	Rectifier, 1N4001GP	226-10400080
DB1	Bridge Rectifier, KBP10	226-30500010

Parts List

Power Supply 8790025 38W (Astec AA11330)

Item Sym	Description	Part Number
IC1	IC, TL431CLP Regulator	211-10800100
L1	Filter Choke Coil Assembly	852-20100140
L2	Filter Choke Coil Assembly	852-20100140
L3	Base Choke	328-00100030
L4	Choke, 1.5 mH	328-00100010
L5	Filter Choke Coil Assembly	852-20100180
L6	Filter Choke Coil Assembly	852-20100180
L7	Choke Coil	328-00100060
Q1	Transistor, SD467, NPN	209-11700460
Q2	Transistor, Power	853-00400050
Q3	Transistor, SD561, PNP	210-11700350
R1	Thermistor, 4 ohm, 10%	258-40970015
R2	Resistor, 330 kohm, 1/2W 5%	240-33406033
R3	Resistor, 220 ohm, 1W 5%, Metal Ox	248-22106052
R4	Resistor, 33 ohm, 2W 5% Metal Ox	248-33006063
R5	Resistor, 1 kohm, 1/4W 5%	240-10206022
R6	Resistor, 27 ohm, 1/4W 5%	240-27006022
R7	Resistor, 68 ohm, 1/4W 5%	240-68006022
R8	Resistor, 120 ohm, 1W 5% Metal Ox	248-12106052
R9	Resistor, 10 ohm, 1/4W 5%	240-10006022
R10	Resistor, 10 ohm, 1/4W 5%	240-10006022
R11	Resistor, .75 ohm, 1W 5% Metal Flm	247-07586054
R12	Resistor, 1 ohm, 1W 5% Metal Film	247-10086054
R13	Resistor, 5.6 ohm, 1/4W 5%	240-56906022
R14	Resistor, 68 ohm, 1/4W 5%	240-68006022
R15	Resistor, 270 ohm, 1/2W 5%	240-27106033
R16	Resistor, 270 ohm, 1/2W 5%	240-27106033
R17	Resistor, 8.2 ohm, 1/4W 5%	240-82906022
R18	Resistor, 560 ohm, 1/4W 5%	240-56106022
R19	Resistor, 56 ohm, 1/4W 5%	240-56006022
R20	Resistor, 56 ohm, 1/4W 5%	240-56006022
R21	Resistor, 12 kohm, 1/4W 5%	240-12306022
R22	Resistor, 470 ohm, 1/4W 5%	240-47106022
R23	Resistor, 4.7 kohm, 1/4W 2%	247-47015022
R24	Resistor, 68 kohm, 1/4W 5%	240-68306022
R25	Resistor, 22 kohm, 1/4W 2%	247-22025022
R26	Resistor, 2.7 kohm, 1/4W 2%	247-27015022
R27	Resistor, 12 ohm, 1/4W 5%	240-12006022

Parts List

Power Supply 8790025 38W (Astec AA11330)

Item Sym	Description	Part Number
SCR1	Silicon Controlled Rectifier, C122F	227-13000010
T1	Transformer, Common Mode	852-20200950
T2	Transformer, Power	851-10200940
T3	Transformer, Control	852-10200680
Z1	Zener Diode, 5.6V, 1W 5%	222-56086002

7.3 Disk Drives

The Model 2000 Computer may be equipped with either two 5-1/4" Floppy Diskette Drives (Model 26-5103) or one 5-1/4" Floppy Diskette and one Hard Disk Drive (Model 26-5104). All drives are mounted in the Main Unit. The associated 38W power supply required for the Hard Disk Drive version is also integrally mounted to the main power supply inside the Main Unit also. The Hard Disk Controller PCB is mounted in the Card Cage assembly at the rear of the Main Unit in the upper-most slot of the card cage. Its power is supplied from the motherboard of the Main Unit.

7.3.1 Floppy Diskette Drives (Mitsubishi M4853)

The Model 26-5103 contains two floppy disk drives. They are accessible from the front of the Main Unit. Removal for replacement or repair is accomplished according to instructions given in Paragraph 3.1.2. The service manual for this type drive is included at the rear of the Model 2000 Service Manual.

7.3.2 Hard Disk Drive (Tandon TM503)

The Model 26-5104 contains one floppy disk drive and one hard disk drive. The floppy disk drive is mounted in the lower position accessible from the front of the Main Unit and the hard disk drive is mounted internally to the Main Unit. It is accessible for service or repair as noted in Paragraph 3.1.2 also. Service information is contained in the service manual located at the rear of the Model 2000 Service Manual. The Hard Disk Drive is a 10 megabyte (formatted) Tandon TM502. It has two 5-1/4" platters, each of which have two read/write surfaces. Each surface has its own dedicated read/write head attached to a common stepper arm mechanism and 306 cylinders which gives a total of 1224 tracks for the drive.

7.3.3 Hard Disk Controller PCB 8898807

The Hard Disk Controller (HDC) PCB assembly is located in the card cage assembly of the Main Unit and accessible from the rear of the Main Unit. It resides in the upper-most slot of the four positions available in the card cage. It is interconnected to the Hard Disk Drive assembly by a cable assembly connected to the rear of the card. It is a 5" x 10" 2-sided board which is mounted to a custom chassis pan which makes installation and removal of the board simple. The HDC is designed to provide all data and control signals for one internal and one external 5-1/4" Winchester technology drive.

The HDC is connected to the Model 2000 motherboard via a 96 position Euro-type connector (J5). Eight data lines are passed through an AMD 8304 (U34) non-inverting transceiver. The lower eight address lines (A0 - A7) are driven onto the HDC by a 74LS244 (U33). Other host control input and output signals are buffered by another 74LS244 (U32).

7.3.3.1 Port Decoding

The Model 2000 HDC is I/O mapped to use nine 8-bit ports from 0270H to 027EH and also 026CH, with only even port locations used. The ports are in the larger range of addresses assigned to the signal PCS4*. When PCS4* is active, it indicates an I/O to a port in the range from 0200H to 027FH. PCS4* is qualified with address line A0 to produce the signal P4SEL*, which indicated an even port address in this range. This is further qualified with A4, A5, and A6 to produce DCRCS*, which indicates one of eight HDC registers between 0270H and 027EH is being accessed. A 74S138 (U21) is used to decode an access of port 026CH to trigger a software reset one-shot. The following table shows the HDC ports and their addresses.

Port Address	Register Assigned
026CH	Software Reset
0270H	Data Register
0272H	Error/Write Precomp
0274H	Sector Count
0276H	Sector Number
0278H	Cylinder LSB
027AH	Cylinder MSB (Bits D0 and D1)
027CH	SDH
027EH	Status/Command

7.3.3.2 Drive Control Logic

The heart of the HDC consists of the WD1010 (U18) and the WD1100-11 (U12). The WD1010 is an MOS/LSI device which performs the functions of a Winchester Disk Controller/Formatter. The WD1010 has an 8-bit bidirectional data bus through which it communicates with the bus transceiver. Selection of the eight internal registers is accomplished through the use of three address lines (A1, A2, and A3), the signal DCRCS*, and either RE* or WE*. RE* and WE* are the signals RD*IB and WR*IB after passing through an LS367 which is enabled by the signal CSI*. When CSI* is inactive, the outputs of the LS367 are tri-stated, allowing the WD1010 to output the signals RE* and WE* to the WD1100-11 and the sector buffer. When the WD1010 wishes to do this, it activates the output BCS* (U18-1) which disables CSI* and produces the signal DISHDB. DISHDB is the inverted BCS* and it is used to disable the bus data transceiver U34. A read of the HDC status register at this time will give a busy indication and no access to the HDC should be attempted until the busy condition no longer exists.

The WD1100-11 is essentially a gate array device which performs several important drive control functions. First, it provides the drive and head select control output signals to the drive interface. Also, it contains two internal one-shots, one of which is used to shape the incoming drive data to a specified pulse width and the other to control the pulse width of the signal DRUN which tells the WD1010 to begin searching for a sector ID field. Finally, the WD1100-11 is used as a sector buffer manager controlling the data flow between the WD1010 and the host system.

The sector buffer (U6) is a 2K x 8-bit static RAM with an access time of 150 nsec or faster. Data from the drive is loaded into it by the WD1010 and WD1100-11 for the host to read and data is loaded into it by the host for the WD1010 to use in formatting or writing to the drive.

The WD1010 and WD1100-11 provide a drive interface compatible with Seagate ST506-type drives. The data and control signals for the internal primary drive are passed to connector J4. The data for the external secondary drive is found on J2 and the control cable for the external drive is connected to J1. Having separate control signal drivers for both drives allows both drives to be terminated at the drive instead of terminating only the last logical drive in a daisy-chain type connection.

7.3.3.3 Data Recovery

System Clock

The fundamental clock is provided by Y1, a 20 MHz crystal oscillator. This is divided to a 10 MHz clock called 2XDR by one-half of U31. 2XDR is again divided by 2 in U16 to produce the signal WCLK, a 5 MHz square wave which provides the internal timing for the WD1010.

Phase Comparator

The phase comparator circuitry is comprised of a PAL16RA (U16), a 60-nsec delay line (U9), and three D-type flip-flops (U26 and one-half of U25).

When data is being inspected from the drive, its phase relationship with respect to the VCO clock must be determined. The function of this circuitry is to provide windows during which the leading edge of the incoming data bit is compared to the leading edge of the VCO output. The windows are approximately 50 nsec in width. A window is initiated by the leading edge of any data bit as it enters U26-3 (INDATA). The window is terminated by the same data bit, edge-delayed 60 nsec by U9, at U26-11 (DLYDATA) or by the VCO output (OSC*) at U25-3. When both DLYDATA and OSC* arrive at the detector, it is reset (by U15-12) until the next data bit arrives. When DLYDATA arrives first, it sets its detector latch to produce a pump-up condition to speed up the VCO. When OSC* arrives at its detector latch first, it produces a pump-down condition to slow down the VCO.

Error Amplifier and VCO

The error amplifier consists of a quad transistor pack (U22), and a low-pass filter. U22 is wired as a balanced current mirror device which sources or sinks current to the filter stage. Whenever the phase comparator determines the VCD is running slower that the incoming data stream, the error amp receives pump-up pulses. The filter integrates the resulting output of U22-8 and provides an average increase in the voltage reference to the VCO (TP7), causing the VCO to speed up. Similarly, whenever the phase detector determines the VCO is running faster than the incoming data stream, the error amp receives pump-down pulses. These are also integrated by the filter and produce an average decrease in the VCO voltage reference (TP7), causing the VCO to slow down.

The VCO is a 74LS124 (U30) which is initially set by adjusting C8 to produce a free-running frequency of 10 MHz at TP5.

Write Precompensation

Write precompensation is accomplished by two means: (1) by activating the signal RWC on the drive control bus, and (2) by writing data 12 nsec early or late on cylinders in the specified precompensation area. WD1010 will activate RWC when the drive heads step inward past a pre-programmed cylinder. The drive will use this signal to initiate reduction of write current in the heads at this time. WD1010 continually produces the signals EARLY* and LATE* which are fed into the PAL (U16) along with the signal RWC. When RWC is active, U16 outputs a delayed and latched (by 2XDR) version of EARLY* and LATE* called EELD and LELD. When RWC is not active, the signal NE is produced by U16. EELD, LELD, and NE are then used as enables for U10 to determine which version of write data is passed on to the data driver (U4). The three versions of write data are produced by U9 which has output taps of 12, 24, 36, 48, and 60 nsec. The input to U9 is produced by the PAL output (U16-12) INDATA. INDATA is either write data (WDATA) when write gate (WGATE) is active, or read data (RDATA) when WGATE is inactive.

7.3.3.4 Controller Alignment

1. Move jumper plug from E2-E3 to E1-E2. This feeds a 4 MHz square wave into the WD1100-11 data input.

2. Adjust R4 until a high-going pulse of between 75-80 nsec is seen at TP8. This is the signal DLYDATA.

3. Adjust R3 until the signal DRUN at RP3 just begins to toggle. This is a preliminary adjustment and will be refined later.

4. Replace the jumper plug to position E2-E3.

5. Adjust trim capacitor C8 until a 100 nsec square wave is seen at TP5 and the DC level of the VCO voltage reference (TP7) is between 2 and 3 volts.

6. Using a diagnostic program such as "JHDSYS", format the diagnostic track.

7. Execute a continuous read of that track.

8. Set the scope for a 2 msec sweep rate. Trigger Channel 1 with index (rising edge). You should see two index pulses spaced about 17 msec apart.

9. Place channel 2 scope probe on TP3 (DRUN). Adjust R3 until you can most clearly define 17 distinct pulses on channel 2 between the two index pulses on channel 1. Watch the pass counter of the read program to ensure that no errors are occuring.

10. Recheck the 100 nsec square wave at TP5 and the DC reference voltage at TP7. Look for a stable setting, making adjustments as needed according to Step 5.

7.3.3.5 HDC Register Specifications

The following is a list of the HDC registers and their specific functions. For more information on programming, refer to the WD1010 data sheets.

1. 026CH Software Reset

Any read or write to this port will trigger a 10 µsec reset pulse to the HDC.

2. 0270H Data Register

This is the port through which data is transferred via the sector buffer between the host and the drive.

3. 0272H Write - Precomp. Register

The value written to this port is equal to 1/4 the cylinder number where the WD1010 will begin precompensation.

Read - HDC Error Register

If the error bit in the status register is set, then this port is read to determine the error.

Bit 0 - Not Used
Bit 1 - Track 0 Error
Bit 2 - Aborted Command
Bit 3 - Not Used
Bit 4 - ID Not Found
Bit 5 - Not Used
Bit 6 - CRC Error In Data Fld
Bit 7 - Bad Block Detected

4. 0274H Sector Count Register

Indicates the number of sectors to be transferred.

5. 0276H Sector Number Register

Loaded with the number of the sector to be accessed (except during format when this is loaded with the number of bytes to be put in gaps 1 and 3 on the disk).

6. 0278H Cylinder LSB

Loaded with the lower eight bits of the cylinder to be accessed.

7. 027AH Cylinder MSB

Loaded with the upper two bits of the cylinder to be accessed (only bits 0 and 1 are usable. This gives a ten-bit binary limit to total number of cylinders.)

8. 027CH SDH Register

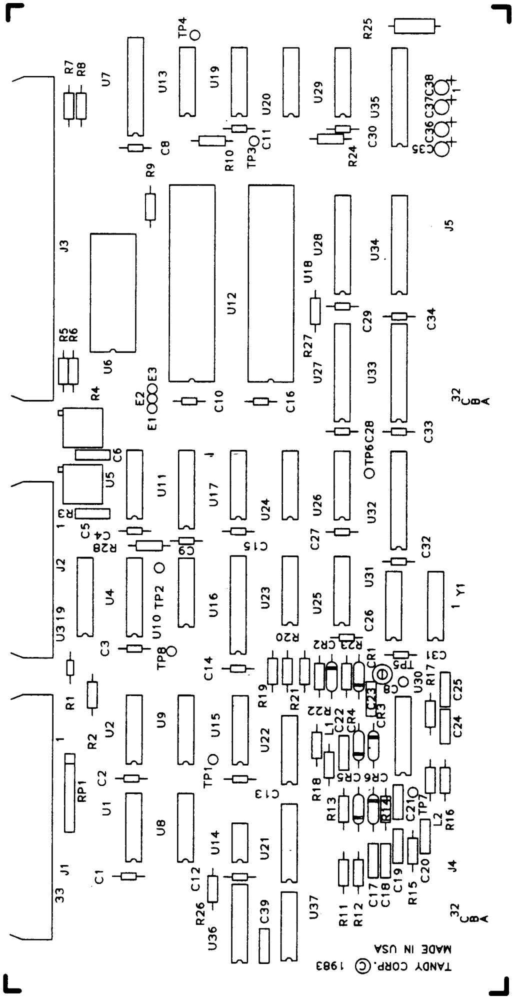
This is loaded with the desired sector size, drive select, and head select information using the following format (bit 7 = 0)

Bits 6	5	Sector Size		Bits 2	1	0	Head Selected
0	0	256		0	0	0	HD 0
0	1	512		0	0	1	HD 1
1	0	1024		0	1	0	HD 2
1	1	128		0	1	1	HD 3
1	0	0	HD 4				
1	0	1	HD 5				
1	1	0	HD 6				
1	1	1	HD 7				

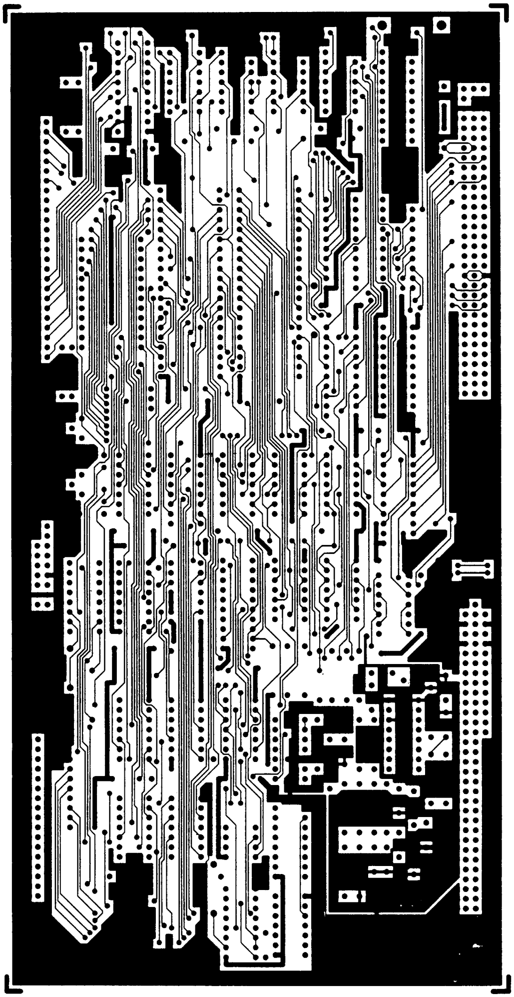
Bits 4	3	Drive Selected
0	0	Drive 0
0	1	Drive 1

Schematic 8000201, HDC PCB Assembly 8898807
Page 1 of 2

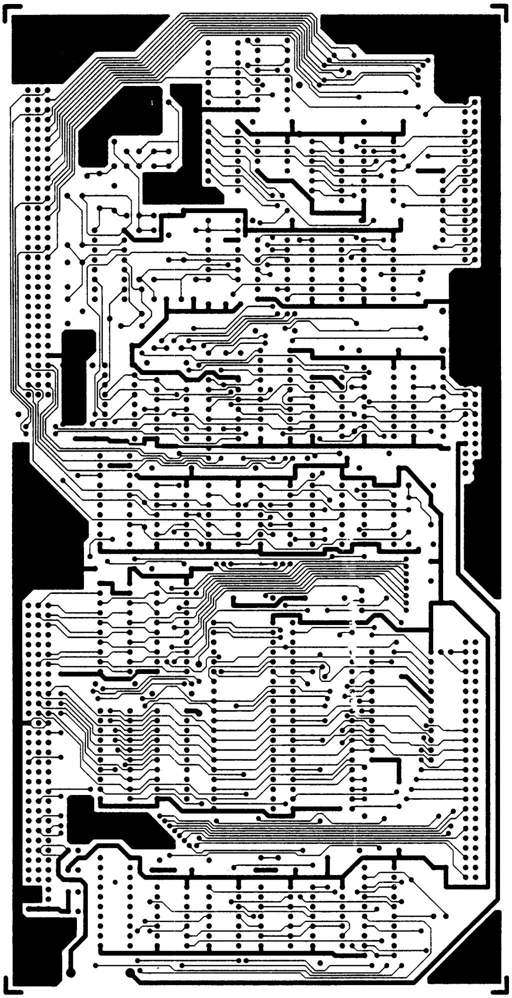
Schematic 8000201, HDC PCB Assembly 8898807
Page 2 of 2



Component Layout, HDC PCB Assembly 8898807



Circuit Trace, HDC PCB Assembly 8898807
Component Side



Circuit Trace, HDC PCB Assembly 8898807
Solder Side

Parts List

Hard Disk Controller Assembly 889B022

Item	Sym	Description	Part Number
1	1	Chassis, Controller/Interface PCB	8729277
2	2	Nylatch Plunger	8590149
3	2	Nylatch Grommet	8590148
4	1	Insulator, PCB	8539051
5*	1	HDC PCB Assembly	8898807
6	1	Cable Assembly, HDC	8709485
7	2	Screw, #2-56 x 5/16" (Conn. Mtg)	8569212
8	6	Screw, #4-40 x 3/16" (PCB Mtg)	8569220

*See separate parts list

Parts List

Hard Disk Controller Board Assembly 8898807 (8-17-83)

Item	Sym	Description	Part Number
1	1	Hard Disk Controller PCB	8709484
2	10	Staking Pin	8529014
3	1	Connector, 64-Pin DIN (J4)	
4	1	Connector, 96-Pin DIN (J5)	
5	1	Connector, 50-Pin (J3)	
6	1	Connector, 20-Pin (J2)	
7	1	Connector, 34-Pin (J1)	
8	1	Socket, 20-Pin (U16)	8509009
9	1	Socket, 24-Pin (U6)	8509001
10	2	Socket, 40-Pin (U12,18)	8509002

C1	Capacitor, .1 mfd, 50V Mono	8374104
C2	Capacitor, .1 mfd, 50V Mono	8374104
C3	Capacitor, .1 mfd, 50V Mono	8374104
C4	Capacitor, .1 mfd, 50V Mono	8374104
C5	Capacitor, 150 pfd, 50V CerDisk NPO	8301153
C6	Capacitor, 150 pfd, 50V CerDisk NPO	8301153
C8	Capacitor, Trim	
C9	Capacitor, .1 mfd, 50V Mono	8374104
C10	Capacitor, .1 mfd, 50V Mono	8374104
C11	Capacitor, .1 mfd, 50V Mono	8374104
C12	Capacitor, .1 mfd, 50V Mono	8374104
C13	Capacitor, .1 mfd, 50V Mono	8374104
C14	Capacitor, .1 mfd, 50V Mono	8374104
C15	Capacitor, .1 mfd, 50V Mono	8374104
C16	Capacitor, .1 mfd, 50V Mono	8374104
C17	Capacitor, .1 mfd, 50V Mono	8374104
C18	Capacitor, .1 mfd, 50V Mono	8374104
C19	Capacitor, .0068 mfd, 50V Cer Disk	8302684
C20	Capacitor, 150 pfd, 50V CerDisk NPO	8301153
C21	Capacitor, 330 pfd, 50V CerDisk NPO	8301332
C22	Capacitor, .1 mfd, 50V Mono	8374104
C23		
C24	Capacitor, .1 mfd, 50V Mono	8374104
C25	Capacitor, .01 mfd, 50V Cer Disk	8303104
C26	Capacitor, .1 mfd, 50V Mono	8374104
C27	Capacitor, .1 mfd, 50V Mono	8374104
C28	Capacitor, .1 mfd, 50V Mono	8374104
C29	Capacitor, .1 mfd, 50V Mono	8374104
C30	Capacitor, .1 mfd, 50V Mono	8374104
C31	Capacitor, .1 mfd, 50V Mono	8374104
C32	Capacitor, .1 mfd, 50V Mono	8374104

Parts List

Hard Disk Controller Board Assembly 8898807

Item Sym	Description	·-t Number
C33	Capacitor, .1 mfd, 50V Mono	8374104
C34	Capacitor, .1 mfd, 50V Mono	8374104
C35	Capacitor, 100 mfd, 16V Elec Radial	8327101
C36	Capacitor, 100 mfd, 16V Elec Radial	8327101
C37	Capacitor, 100 mfd, 16V Elec Radial	8327101
C38	Capacitor, 100 mfd, 16V Elec Radial	8327101
CR1	Diode, 1N4148	8150148
CR2	Diode, 1N4148	8150148
CR3	Diode, 1N4148	8150148
CR4	Diode, 1N4148	8150148
CR5	Diode, 1N4148	8150148
CR6	Diode, 1N4148	8150148
L1	Inductor, 4.7 mH	8419017
L2	Inductor, 4.7 mH	8419017
R1	Resistor, 100 ohm, 1/4W 5%	8207110
R2	Resistor, 100 ohm, 1/4W 5%	8207110
R3	Resistor, 10 kohm, Trimpot	8279312
R4	Resistor, 10 kohm, Trimpot	8279312
R5	Resistor, 4.7 kohm, 1/4W 5%	8207247
R5	Resistor, 4.7 kohm, 1/4W 5%	8207247
R6	Resistor, 4.7 kohm, 1/4W 5%	8207247
R7	Resistor, 4.7 kohm, 1/4W 5%	8207247
R8	Resistor, 4.7 kohm, 1/4W 5%	8207247
R9	Resistor, 4.7 kohm, 1/4W 5%	8207247
R10	Resistor, 1 kohm, 1/4W 5%	8207210
R11	Resistor, 200 ohm, 1/4W 1%	8200120
R12	Resistor, 2.37 kohm, 1/4W 1%	
R13	Resistor, 2.37 kohm, 1/4W 1%	
R14	Resistor, 330 ohm, 1/4W 5%	8207133
R15	Resistor, 680 ohm, 1/4W 5%	8207168
R16	Resistor, 4.7 kohm, 1/4W 5%	8207247
R17	Resistor, 5.6 kohm, 1/4W 5%	8207256
R18	Resistor, 2.61 kohm, 1/4W 1%	
R19	Resistor, 1 kohm, 1/4W 5%	8207210
R20	Resistor, 1 kohm, 1/4W 5%	8207210
R21	Resistor, 1 kohm, 1/4W 5%	8207210
R22		
R23		
R24	Resistor, 4.7 kohm, 1/4W 5%	8207247
R25	Resistor, 22 ohm, 1/2W 5%	8217022

Parts List

Hard Disk Controller Board Assembly 8898807

Item Sym	Description	Part Number
RP1	Resistor Pak, 220/330 ohm SIP	8290019
U1	IC, 7438, 2-Input NAND	8000038
U2	IC, 74F04, Hex Inverter	8015004
U3	IC, 3486, Quad Receiver	8050486
U4	IC, 3487, Quad Driver	8050487
U5	IC., 74LS293, Binary Counter	8020293
U6	IC, HM6116, 2K x 8 RAM 150 nsec	8046116
U7	IC, 74LS244, Octal Buffer	8020244
U9	IC, DDU-4-5060, Delay Line	
U10	IC, 74S64, AND/OR Inverter	8010064
U11	IC, 74LS367, Hex Bus Driver	8020367
U12	IC, WD1100-11	8041111
U13	IC, 74F32, Quad 2-Input OR	8015832
U15	IC, 74S10, 3-Input NAND	8010010
U16	IC, PAL16R6A	8041166
U17	IC, 74LS14, Hex Inverter	8020014
U18	IC, WD1010	8041010
U19	IC, 74F32, Quad 2-Input OR	8015832
U20	IC, 74F04, Hex Inverter	8015004
U22	IC, MPQ6700, Transistor Array	
U23	IC, 7438, 2-Input NAND	8000038
U24	IC, 7438, 2-Input NAND	8000038
U25	IC, 74F74, Flip Flop	8015074
U26	IC, 74F74, Flip Flop	8015074
U27	IC, 74LS244, Octal Buffer	8020244
U28	IC, AM8304, Bus Transceiver	8060304
U29	IC, 74F08, Quad 2-Input AND	8015008
U30	IC, 74S124, Voltage Con. Osc.	8010124
U31	IC, 74F74, Flip Flop	8015074
U32	IC, 74LS244, Octal Buffer	8020244
U33	IC, 74LS244, Octal Buffer	8020244
U34	IC, AM8304, Bus Transceiver	8060304
Y1	Crystal Osc., 20 MHz	8409029

7.4 Motherboard

7.4.1 Introduction

The Model 2000 Mother Board is a part of the Card Cage/Mother Board sub-assembly which provides a simple method of adding optional features to the main unit.

The Mother Board assembly consists of a printed circuit board with four 96-pin male reverse DIN eurocard connectors (DIN 41612) to accommodate the option card(s); a 96-pin female reverse DIN eurocard connector for connection to the Main Logic Board; a 6-pin Molex connector which supplies DC power to the Mother Board and the option card(s) via the DC power harness; and various resistor networks for terminating the signals on the expansion connectors.

7.4.2 Theory of Operation

All of the signals available on the option card connectors are provided for general interface to the Main Logic Board. The only exceptions are seven signals which are specifically used by the graphics option card and are available only on the bottom connector (J18). The following table describes the signal interface and connector pin assignments for option card connector J15-J18.

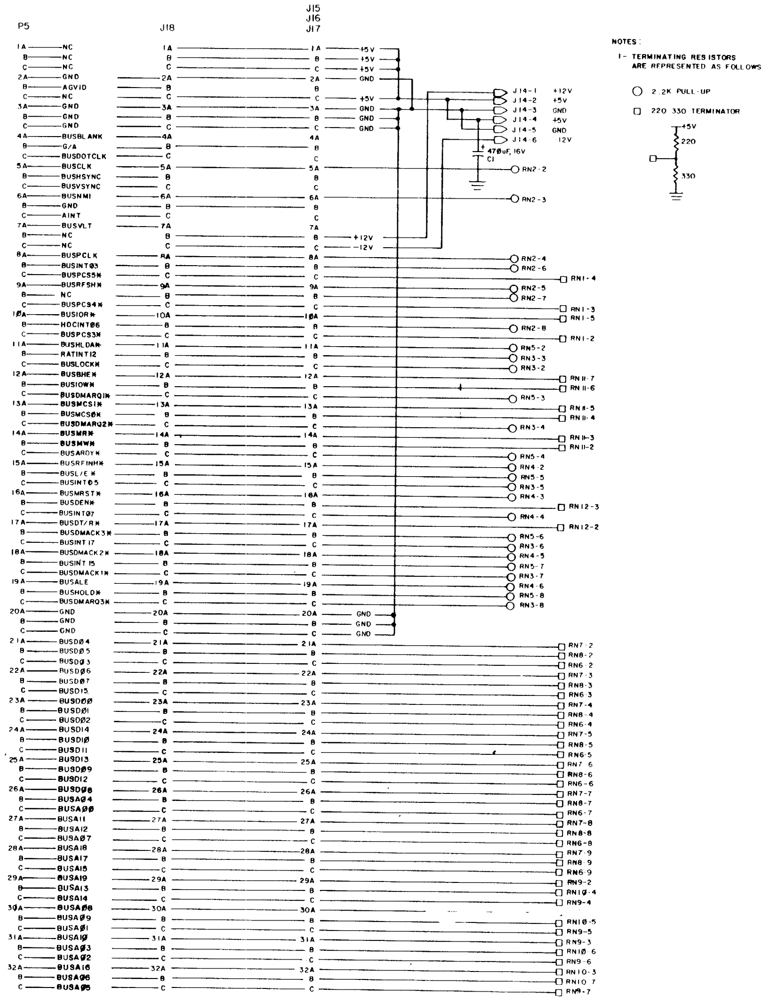
Description	Mnemonic	Pin Number
20-bit Address Bus	BUSA00-BUSA19	26b-32c
16-bit Data Bus	BUSD00-BUSD15	21a-26a
Memory Chip Select	BUSMCS0*, BUSMCS1*	13b, 13a
Peripheral Chip Select	BUSPCS3*, BUSPCS4*,	10c, 9c,
BUSPCS5*	8c	
Interrupt Control	BUSINT03, BUSINT05,	8b, 15c,
HDCINT06, BUSINT07,	10b, 16c,	
RATINT12, MEMINT15,	11b, 18b,	
BUSINT16, BUSINT17	9b, 17c	
Non-Maskable Interrupt	NMI*	6a
DMA Request	BUSDMARQ1*, BUSDMARQ2*,	12c, 13c,
BUSDMARQ3*	19c	
DMA Acknowledge	BUSDMACK1*, BUSDMACK2*,	18c, 18a,
BUSDMACK3*	17b	
Memory Read and Write	BUSMR*, BUSMW*	14a, 14b
I/O Read and Write	BUSIOR*, BUSIOW*	10a, 12b
Master Reset	BUSMRST*	16a
Address Latch Enable	BUSALE	19a

Data Transmit/Receive	BUSDT/R*	17a
Data Enable	BUSDEN*	16b
System Bus Control	BUSHOLD*, BUSHLDA*,	19b, 11a,
BUSLOCK*, BUSBHE*,	11c, 12a,	
BUSL/E*	15b	
Asynchronous Ready	BUSARDY*	14c
Memory Refresh Control	BUSRFSH*, BUSRFINH*	9a, 15a
8 MHz Processor Clock	BUSPCLK	8a
System Clock (not used)	BUSCLK	5a
Video Dot Clock	BUSDOTCLK	4c
Video Vertical Sync	BUSVSYNC	5c
Video Horizontal Sync	BUSHSYNC	5b
Video Blanking	BUSBLANK	4a
Video Intensity	AINT	6c
Video Control	BUSVLT, AGVID, G/A	7a, 2b, 4b

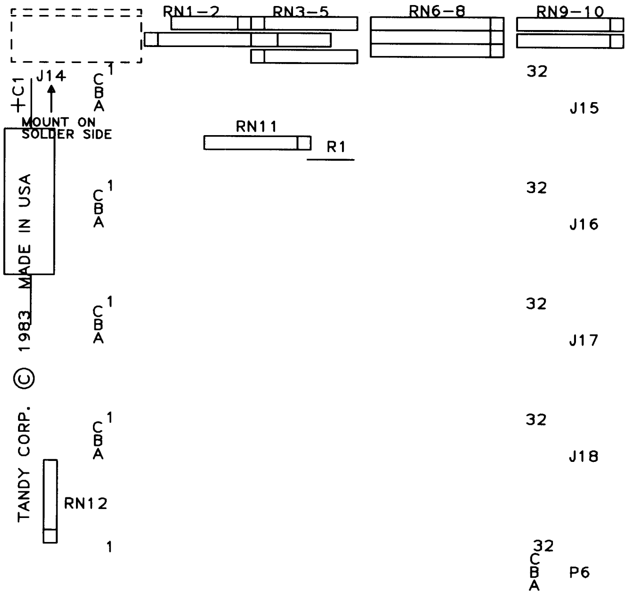
DC power is supplied directly to the Mother Board through a 6-pin Molex connector (J14). Pin assignments for DC power are shown in the table below.

Connector		
J14	J15-J18	
+12 Volts	1	7b
-12 Volts	6	7c
+5 Volts	2, 4	1a, 1b, 1c, 2c
Ground	3, 5	2a, 3a, 3b, 3c,
6b, 20a, 20b, 20c		

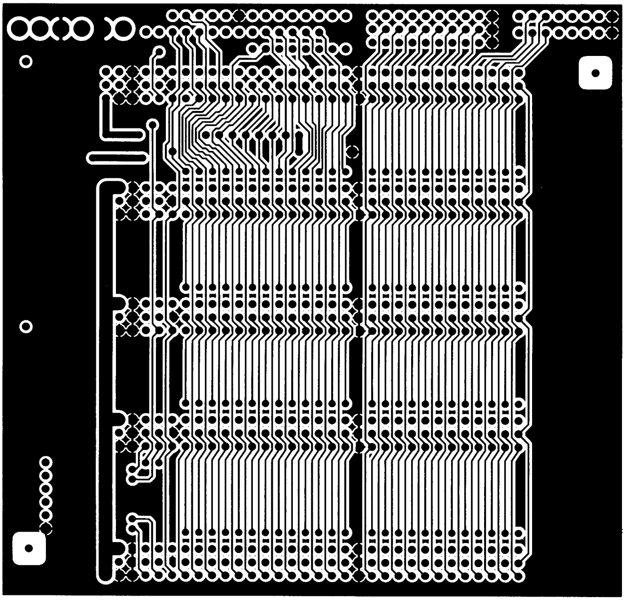
All of the signals, except the video signals, that are used by the option cards have been terminated on the Mother Board. Resistor networks have been used to either pull up the signal with a 2.2 kohm resistor to +5 volts or establish a 3-volt level using a 220 ohm/330 ohm split termination. See the schematic to determine the termination on each signal.



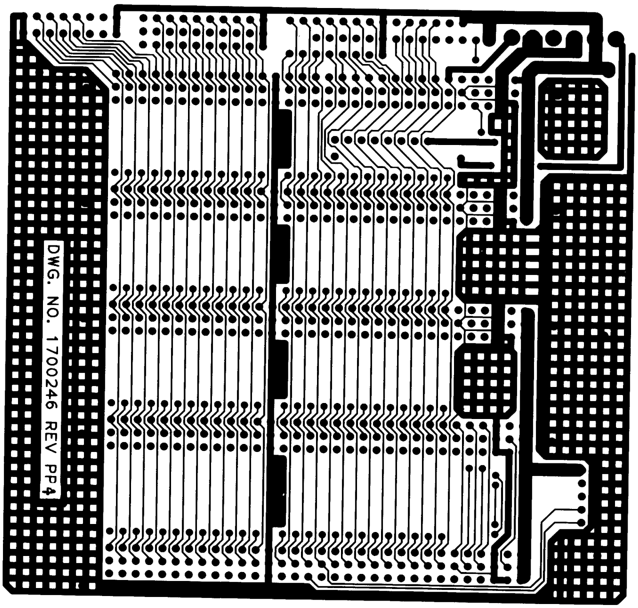
Schematic 8000212, Mother Board



Component Layout, Mother Board PCB Assembly 8898803



Circuit Trace, Mother Board PCB Assembly 8898803
Component Side



Circuit Trace, Mother Board PCB Assembly 8898803
Solder Side

Parts List

Mother Board Assembly 8898803

Item	Sym	Description	Part Number
1	1	Mother Board PCB	8709431
2	1	Connector, 96-pin Rt. Ang. Fem (P6)	8519181
3	1	Connector, 6-pin Straight (J14)	8519186
4	4	Connector, 96-pin Male (J15-18)	8519182
5	1	Serial Number Tag, PCB	87891045
6	2	Screw, #2-56 x 3/8" PPH	8569201
7	2	Nut, #2-56	8579042

R1	Resistor, 0 ohm	8290000
RN1	Res. Pak, 220/330 ohm 6-pin SIP	8
RN2	Res. Pak, 2.2 kohm 8-pin SIP	8290039
RN3	Res. Pak, 2.2 kohm 8-pin SIP	8290039
RN4	Res. Pak, 2.2 kohm 6-pin SIP	8290043
RN5	Res. Pak, 2.2 kohm 8-pin SIP	8290039
RN6	Res. Pak, 220/330 ohm 10-pin SIP	8290020
RN7	Res. Pak, 220/330 ohm 10-pin SIP	8290020
RN8	Res. Pak, 220/330 ohm 10-pin SIP	8290020
RN9	Res. Pak, 220/330 ohm 8-pin SIP	8290019
RN10	Res. Pak, 220/330 ohm 8-pin SIP	8290019
RN11	Res. Pak, 220/330 ohm 8-pin SIP	8290019
RN12	Res. Pak, 220/330 ohm 6-pin SIP	8

7.5 128K RAM PCB

7.5.1 INTRODUCTION

The Model 2000 has the capablility of 256K words of memory, with parity, located on the Main Logic Board. This memory is separated into two sections: a 128K word System Memory board and a 128K word Internal Expansion Memory board. The System Memory is mapped from 00000H to 1FFFFH and the Internal Expansion Memory is mapped from 20000H to 3FFFFH.

7.5.2 THEORY OF OPERATION - 128K SYSTEM RAM

The System RAM board consists of a 6.3 inch by 2.5 inch printed circuit board with eighteen high speed dynamic Random Access Memories (RAM's). Each RAM device is organized as 65,536 one bit words with a maximum access time of 150 nanoseconds. Bulk decoupling of the +5 volt power bus to the RAM's is provided by 100 microfarad, 6.3 volt dipped tantalum electrolytic capacitors. Also, each device is decoupled with a 0.1 microfarad capacitor across its Vcc (pin 8) and ground (pin 16) pins.

Interface to the memory control and timing sections on the Main Logic Board is accommplished through a special pin header which mates with a 40-pin, bottom entry connector (P11) on the System RAM board. Signal pin assignments for P11 are shown in Table 1. The System RAM board also interfaces to the Internal Expansion RAM board through a 40-pin, right angle receptacle (P13). Table 2 specifies pin assignments for P13.

7.5.3 SIGNAL DEFINITION

The following list defines each signal available on the System RAM connectors. For specific memory control and timing specifications see Section 7.1.8 of the Main Logic Board theory of operation.

ADDRESS RANGE	00000H-1FFFFH	20000H-3FFFFH
Write Input	WR0*	WR1*
Row Address Select	RAS0*	RAS1*
WORD SEGMENT	UPPER	LOWER
Column Address Select	CASL*	CASU*
Data Input Parity	DIPL	DIPU
Data Output Parity	DOPL	DOPU
8-bit Memory Address Bus	DMEMA00-DMEMA07	
16-bit Memory Data Bus	IB00-IB15	

7.5.4 Troubleshooting

Memory Read or Write errors can be determined by using the memory diagnostic routines that are available for the Model 2000.

After initializing the test program, a top of memory algorithm is executed to determine how much memory has been installed in the Model 2000 under test. If the response to the memory size inquiry does not agree with the amount of memory the user has installed, it can be assummed that either the memory installation was not performed correctly or the memory boards installed are defective. The user should check all connectors to insure proper and complete mating before attempting to isolate a defective board and/or component.

Once the user is confident of the installation integrity, the memory diagnostic test may be run. There are three tests that are available: a read/write data test; a long modified address test and a short modified address test.

The data test writes a known data pattern to all memory locations. The data is then read back and compared to the known data pattern for errors. Errors generated by this test would indicate a problem either on the data/address bus interface to memory or with the decoders associated with the memory array.

The modified address test has two versions: the long test will test the RAM 65,536 times per pass (0000H-FFFFH) and the short test will test the RAM 256 times per pass (0000-00FF). The number of tests per pass is determined by a 16-bit mask register which is incremented by one for each write/read cycle through the entire memory array (i.e., 00000H-7FFFFH for 512K). The data pattern written is the result of the exclusive-OR of the high address segment register (16-bit) with the result of the exclusive-OR of the lower address segment or offset (16-bit) and the mask register. This data pattern is written through the memory array and then read and compared to check for accuracy. Errors that occur will be listed individually in the error table that specifies the data written, the data read, the exclusive-OR of the data written and the data read, and the address where the error occurred. In most cases, this will indicate which RAM chip in a particular bank has failed.

It is recommended that all three RAM tests should be used to verify correct operation of the RAM installed in the unit. Although these tests do not exercise every combination of bits that can be written throughout the full RAM capacity, they exercise enough write/read operations to achieve a fairly reliable test of memory I/O and data recovery to isolate most common memory failures. A complete test that exercises every bit in an array is impractical because of the extreme number of bit combinations, especially in larger memory arrays. For a 16-bit system, there are $16(2^n)$ combinations, where n equals the memory size (e.g., 128K,256K,512K), that must be written, read and compared to complete the full test. In comparison, the modified address method reduces the amount of time it takes to complete a pass but even the long modified address test on a 512K memory array will take approximately 30 hours to complete.

Table 7-9. P11 Pin Assignments

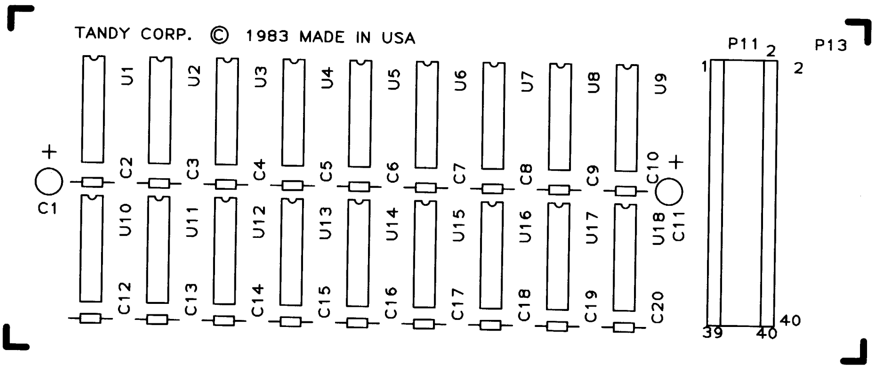
System RAM To Main Logic Board Interface

PIN #	SIGNAL	PIN #	SIGNAL
01	IB01	02	IB00
03	IB02	04	IB04
05	IB03	06	IB05
07	IB07	08	IB06
09	DIPL	10	DOPL
11	WR0*	12	DMEMA06
13	RAS0*	14	DMEMA03
15	DMEMA00	16	DMEMA04
17	DMEMA02	18	DMEMA05
19	DMEMA01	20	DMEMA07
21	GROUND	22	CASU*
23	GROUND	24	GROUND
25	+5 VOLTS	26	+5 VOLTS
27	+5 VOLTS	28	RAS1*
29	WR1*	30	CASL*
31	DOPU	32	DIPU
33	IB12	34	IB15
35	IB11	36	IB14
37	IB10	38	IB08
39	IB09	40	IB13

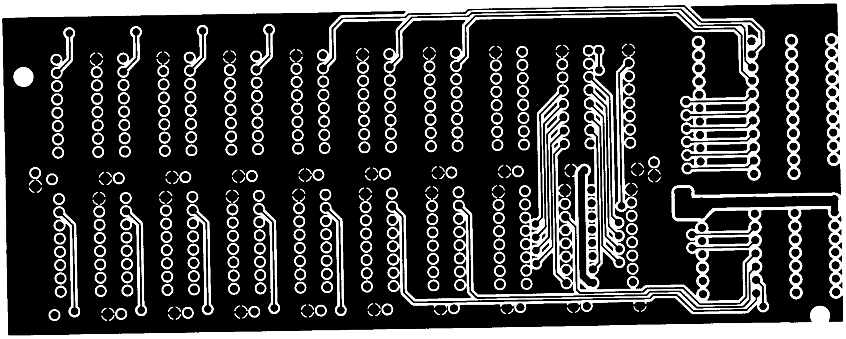
Table 7-10. P13 Pin Assignments

System RAM To Internal Expansion RAM Interface

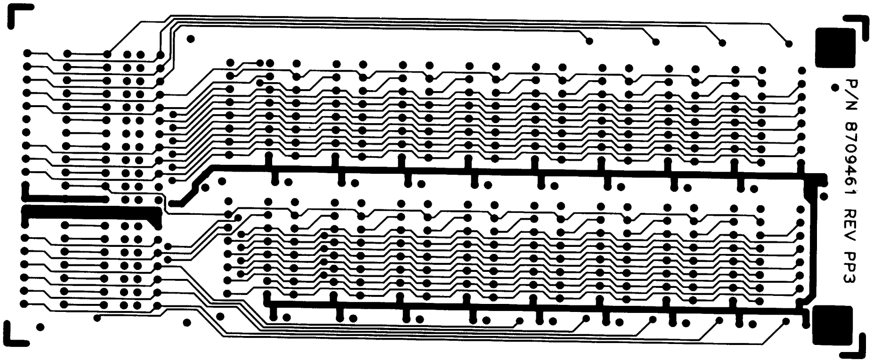
PIN #	SIGNAL	PIN #	SIGNAL
01	IB01	02	IB00
03	IB02	04	IB04
05	IB03	06	IB05
07	IB07	08	IB06
09	DIPL	10	DOPL
11	NO CONNECTION	12	DMEMA06
13	NO CONNECTION	14	DMEMA03
15	DMEMA00	16	DMEMA04
17	DMEMA02	18	DMEMA05
19	DMEMA01	20	DMEMA07
21	GROUND	22	CASU*
23	GROUND	24	GROUND
25	+5 VOLTS	26	+5 VOLTS
27	+5 VOLTS	28	RAS1*
29	WR1*	30	CASL*
31	DOPU	32	DIPU
33	IB12	34	IB15
35	IB11	36	IB14
37	IB10	38	IB08
39	IB09	40	IB13



Component Layout, System RAM PCB Assembly 8898806



Circuit Trace, System RAM PCB Assembly 8898806
Component Side



Circuit Trace, System RAM PCB Assembly 8898806
Solder Side

Parts List

128K Internal RAM Board Assembly 8898806

Item	Sym	Description	Part Number
1	1	128K RAM PCB	8709461
2	2	Connector, 20-Pin Bottom Entry(P11)	8519199
3	1	Connector, 40-Pin (P13)	8519200
4	1	PCB Serial Number Label	87891043
C1		Capacitor, .1 mfd, 50V Mono Axial	8374104
C2		Capacitor, .1 mfd, 50V Mono Axial	8374104
C3		Capacitor, .1 mfd, 50V Mono Axial	8374104
C4		Capacitor, .1 mfd, 50V Mono Axial	8374104
C5		Capacitor, .1 mfd, 50V Mono Axial	8374104
C6		Capacitor, .1 mfd, 50V Mono Axial	8374104
C7		Capacitor, .1 mfd, 50V Mono Axial	8374104
C8		Capacitor, .1 mfd, 50V Mono Axial	8374104
C9		Capacitor, .1 mfd, 50V Mono Axial	8374104
C10		Capacitor, 100 mfd, 6V Tant. Rad.	8337100
C11		Capacitor, .1 mfd, 50V Mono Axial	8374104
C12		Capacitor, .1 mfd, 50V Mono Axial	8374104
C13		Capacitor, .1 mfd, 50V Mono Axial	8374104
C14		Capacitor, .1 mfd, 50V Mono Axial	8374104
C15		Capacitor, .1 mfd, 50V Mono Axial	8374104
C16		Capacitor, .1 mfd, 50V Mono Axial	8374104
C17		Capacitor, .1 mfd, 50V Mono Axial	8374104
C18		Capacitor, .1 mfd, 50V Mono Axial	8374104
C19		Capacitor, .1 mfd, 50V Mono Axial	8374104
C20		Capacitor, 100 mfd, 6V Tant. Rad.	8337100
U1		IC, MCM6665-15 RAM	8041665
U2		IC, MCM6665-15 RAM	8041665
U3		IC, MCM6665-15 RAM	8041665
U4		IC, MCM6665-15 RAM	8041665
U5		IC, MCM6665-15 RAM	8041665
U6		IC, MCM6665-15 RAM	8041665
U7		IC, MCM6665-15 RAM	8041665
U8		IC, MCM6665-15 RAM	8041665
U9		IC, MCM6665-15 RAM	8041665
U10		IC, MCM6665-15 RAM	8041665
U11		IC, MCM6665-15 RAM	8041665
U12		IC, MCM6665-15 RAM	8041665
U13		IC, MCM6665-15 RAM	8041665
U14		IC, MCM6665-15 RAM	8041665
U15		IC, MCM6665-15 RAM	8041665
U16		IC, MCM6665-15 RAM	8041665
U17		IC, MCM6665-15 RAM	8041665
U18		IC, MCM6665-15 RAM	8041665

7.6 Keyboard Assembly

The keyboard for the Tandy Model 2000 computer is a 90-key keyboard with twelve function keys, numeric keypad, and special purpose keys for paging. It is connected to the Main Unit by a coiled cable and may be operated from a location up to 4 feet from the main unit. Figure __ shows the interconnecting cable connector to the keyboard assembly. The cable assembly may be disconnected from the keyboard assembly during repair if desired (see Paragraph 6.4 for disassembly procedures).

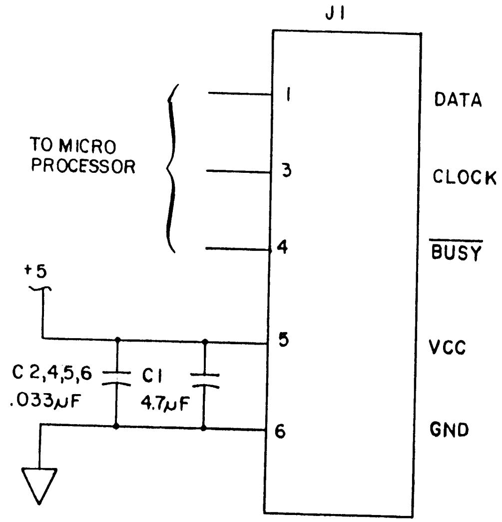


Figure 7-39. Keyboard Assembly Connector

7.6.1 Keyboard Specifications

The keyboard is a fully encoded type with microprocessor control. Power required by the keyboard is +5 Vdc supplied from the Main Unit.

1. Key Type - all keys generate "make" and "break" codes. See Table 7-11 for key codes. Break codes are formed by adding 80H to the make code. Keys 49 and 71 have alternate action which "makes" on one actuation of the key and "breaks" on succeeding actuation. No code is generated for these two keys when the key is released.

2. Number of Keys - 90

3. Repeat Strobe - there is a repeat strobe of 66 to 111 msec when any key is depressed for more that 1 second with the exception of SHIFT, CTRL, CAPS, ENTER and NUMBER LOCK.

7.6.2 Key Code Chart

Key Number	Legend	Scan Code
1	F1	3B
2	F2	3C
3	F3	3D
4	F4	3E
5	F5	3F
6	F6	40
7	F7	41
8	F8	42
9	F9	43
10	F10	44
11	F11	59
12	F12	5A
13	INSERT	55
14	DELETE	53
15	BREAK	54
16	ESC	01
17	1 !	02
18	2 @	03
19	3 #	04
20	4 $	05
21	5 %	06
22	6 ^	07
23	7 &	08
24	8 *	09
25	9 (	0A
26	0)	0B
27	- _	0C
28	= +	0D
29	BACKSPACE	0E
30	ALT	38
31	PRINT	37
32	7 (backslash)	47
33	8 (Tilde)	48
34	9 PG UP	49
35	TAB	0F
36	Q	10
37	W	11
38	E	12
39	R	13
40	T	14
41	Y	15
42	U	16
43	I	17
44	O	18
45	P	19

Key Number	Legend	Scan Code
46	{ [	1A
47	}]	1B
48	HOLD	46
49	NUM LOCK	45
50	4 :	4B
51	5	4C
52	6	4D
53	CTRL	1D
54	A	1E
55	S	1F
56	D	20
57	F	21
58	G	22
59	H	23
60	J	24
61	K	25
62	L	26
63	; :	27
64	' "	28
65	ENTER	1C
66		29
67	HOME	58
68	1 END	4F
69	2 (Grave)	50
70	3 PG DN	51
71	CAPS	3A
72	SHIFT	2A
73	Z	2C
74	X	2D
75	C	2E
76	V	2F
77	B	30
78	N	31
79	M	32
80	, <	33
81	. >	34
82	/ ?	35
83	SHIFT	36
84		2B
85		4A
86		4E
87	0	52
88	.	56
89	ENTER	57
90	(Space Key)	39

91 thru 95 - reserved for International

7.6.3 Keyboard Timing

Figure 7-40 is the timing chart for the Model 2000 Keyboard Assembly.

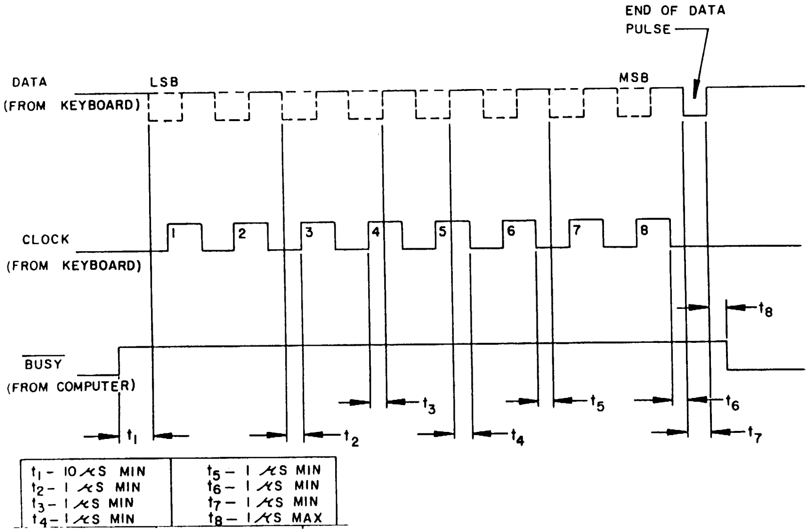


Figure 7-40. Keyboard Assembly Timing Chart

7.6.4 Keyboard Layout

Shown below is the keyboard layout and number designation of the keys on the Model 2000 keyboard. They should be used with Table 7-11 (Key Code Chart) for determining data signal transmitted by the keyboard.

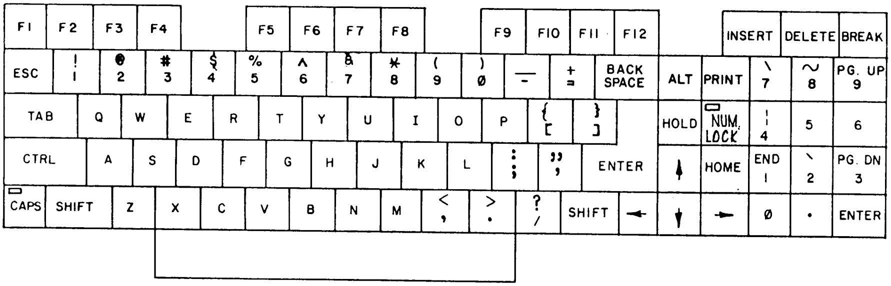
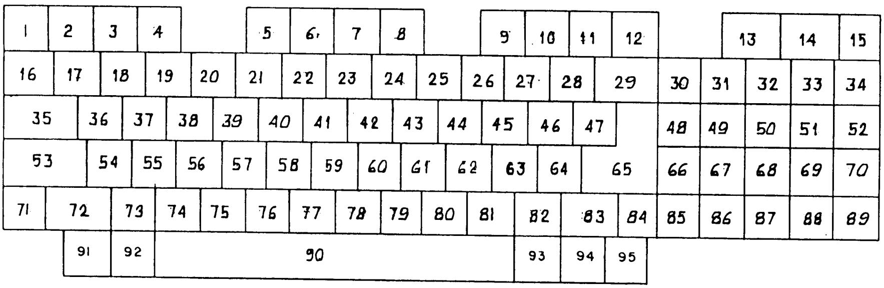
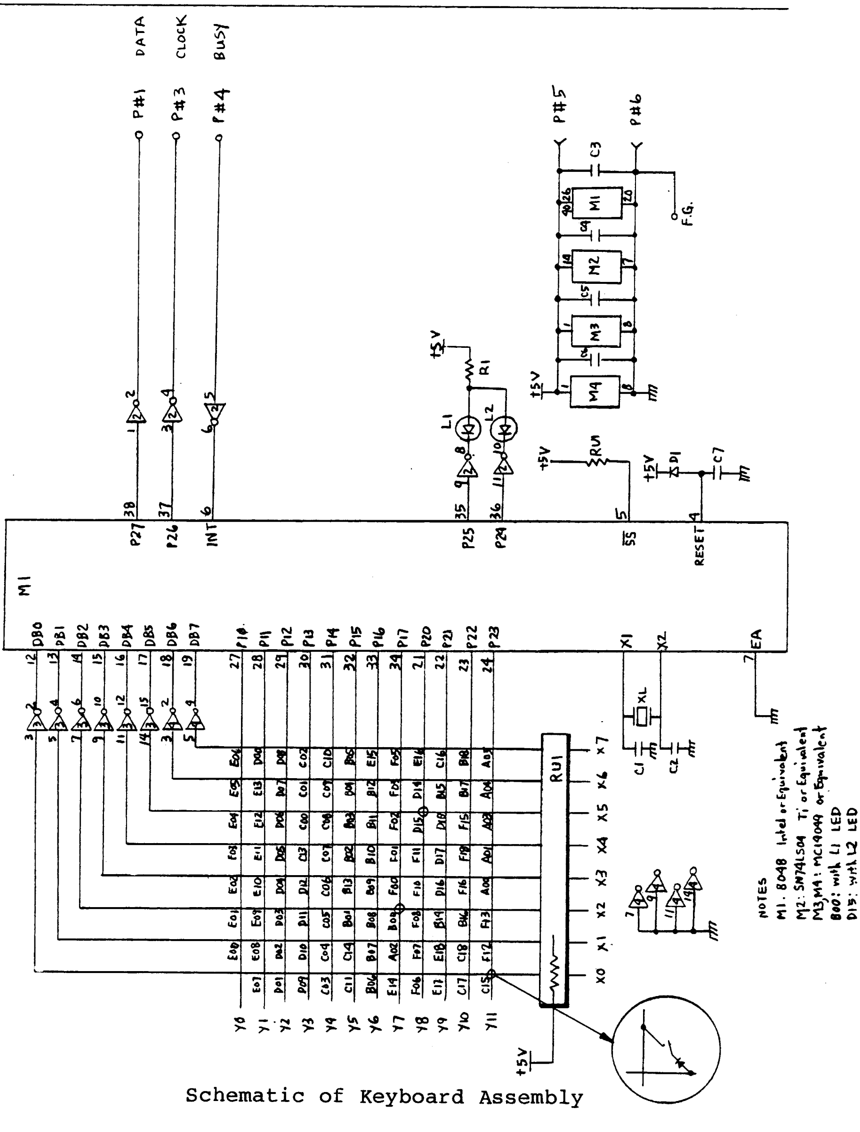


Figure 7-41. Keyboard Identification



NOTE: KEYS 91 THRU 95 NOT USED ON U.S. VERSION, USED ON INTERNATIONAL VERSION ONLY

Figure 7-42. Key Number Identification



Schematic of Keyboard Assembly

8/ Parts Lists/Exploded Views

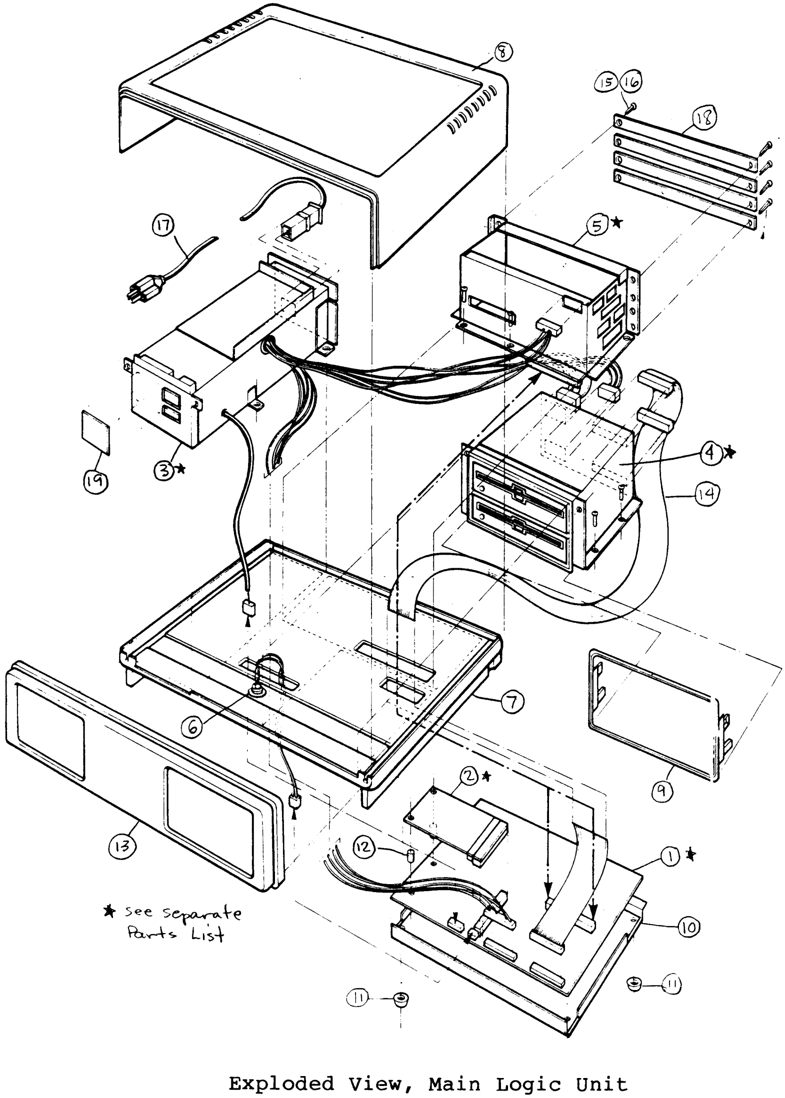
Contained in this section of the manual are parts lists and exploded views and parts lists for the various subassemblies of the Radio Shack Model 2000 Microcomputer. This section has been divided into major subassembly components to facilitate its use. These sections include the Main Logic Unit (with associated subassembly drawings/parts lists), and the Keyboard Assembly. The Display Unit and Internal Floppy Disk Drive/Hard Disk Drive Assemblies are described in Appendices at the end of this manual. Other optional features are described and listed in supplements which support the particular option.

Pictorial representation contained in the exploded views may vary slightly from the actual unit due to improvements incorporated into the unit after printing of this manual. For information concerning variations, contact Technical Support in Fort Worth, Texas.

Parts List

Main Logic Unit Assembly

Item	Sym	Description	Part Number
1	1	Main Logic PCB Assembly	889B001
2	1	128K RAM Board Assembly	8898806
3	1	Power Supply Assembly	889B003
4	1	Mini-Floppy Disk Drive Assembly	889
5	1	Card Cage Assembly	889
6	1	Speaker Assembly	889
7	1	Bottom, Case	8719320
8	1	Top, Case	8719319
9	1	Bezel, Disk Drive (Mitsubishi)	8719401
1		Bezel, Disk Drive (Tandon)	8719355
2		Handle, Disk Drive (Tandon)	8719353
10	1	Chassis, Main Logic PCB	8729240
11	4	Foot, Case	8719370
12	2	Standoff, RAM Board	8590150
13	1	Bezel, Front	8719318
14	1	Cable Assembly, Floppy Disk Signal	8709447
15	1	Cable Assembly, DC Power	8709444
16	1	Cable Assembly, Power Reset	8709464
17	1	Power Cord, AC	8709468
18	4	Panel, Card Cage	8729233
8		Plunger, Nylatch	8590149
19	1	Logo	8719330

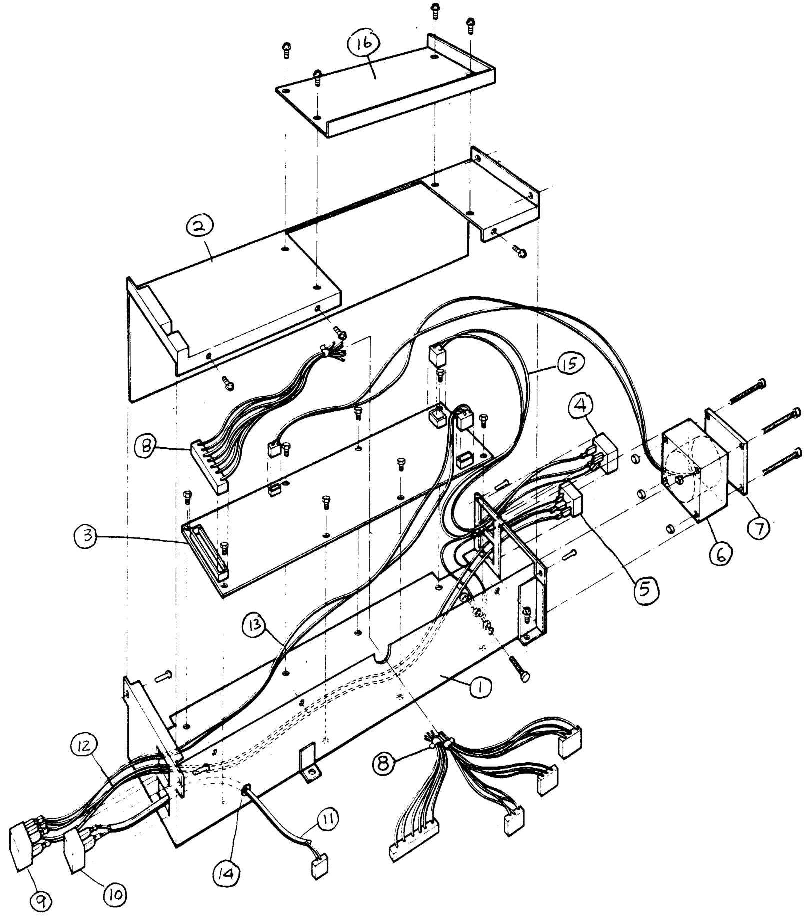


Exploded View, Main Logic Unit

Parts List

Power Supply Assembly 88898003 (95W Tandy)

Item	Sym	Description	Part Number
1	1	Weldment, Lower Enclosure	8729256
2	1	Enclosure, Upper	8729231
3	1	Power Supply PCB Assembly	8790056
4	1	Convenience Outlet	8519195
5	1	AC Inlet	8519207
6	1	Fan, DC	8790407
7	1	Guard, Finger	8719369
8	1	Cable Assembly, DC Main Power	
9	1	Switch, Power	8489073
10	1	Switch, Reset	8489071
11	1	Cable Assembly, Reset	8709464
12	1	Cable Assembly, AC Power In	8709471
13	1	Cable Assembly, Power Switch	8709467
14	1	Bushing, Reset Harness	
15	1	Cable Assembly, Auxiliary Power	8709466
16	1	Cover, Power Supply	8729230
17	1	Fuse, AC (5 x 20 mm)	8479021

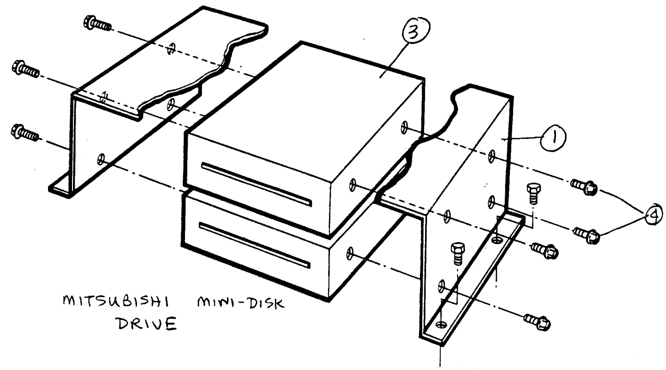


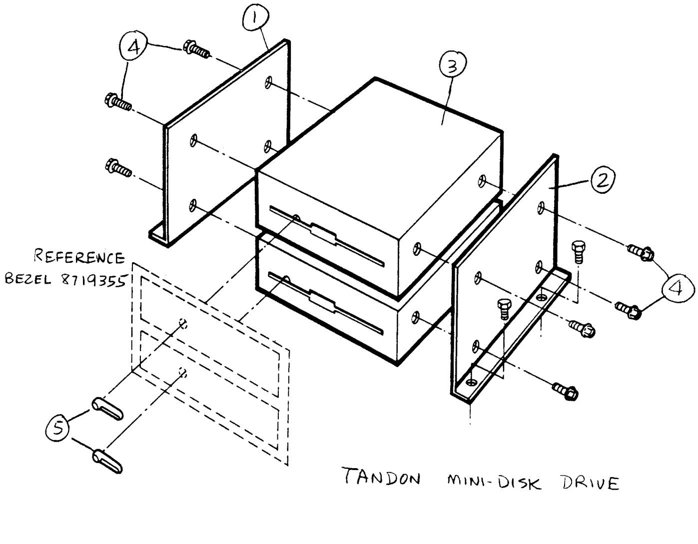
Exploded View, Power Supply Assembly 889B003

8.1.2 Mini-Floppy Disk Drive Assembly

Item	Sym	Description	Part Number
1	1	Bracket, LH Mounting (Tandon Drive)	8729235
1		Bracket, Mtg (Mitsubishi Drive)	8719401
2	1	Bracket, RH Mounting (Tandon Drive)	8729236
3	2	Drive, Mini-Floppy Disk (Tandon)	8790122
2		Drive, Mini-Floppy Disk(Mitsubishi)	8790124
4	8	Screw, #6-32 x 1/4" PSL MS	8569218
5	2	Handle, Disk Drive (Tandon)	8719353

Note: For additional breakdown of parts for individual disk drive types, see addendum section at the back of this Model 2000 Service Manual.



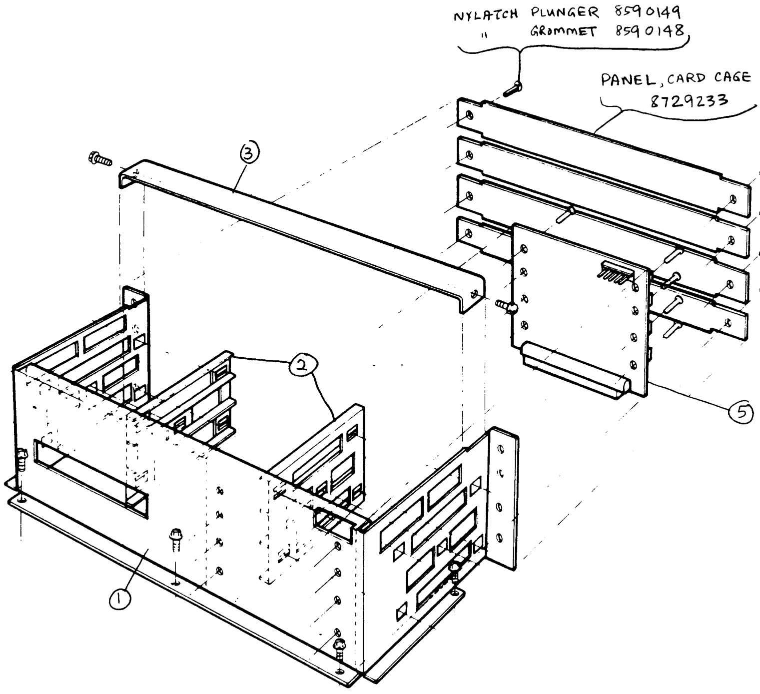


Exploded View, Disk Drive Assemblies

Parts List

Card Cage Assembly, Model J Microcomputer

Item	Sym	Description	Part Number
1	1	Card Cage	8729234
2	2	Guide, Card Cage	8719333
3	1	Brace, Card Cage	8729255
4	1	Motherboard PCB Assembly	8898803
5	8	Screw, #2-56 x 5/16" PPH MS	8569212
6	2	Screw, #6 x 5/16" PSL TCS	8569214

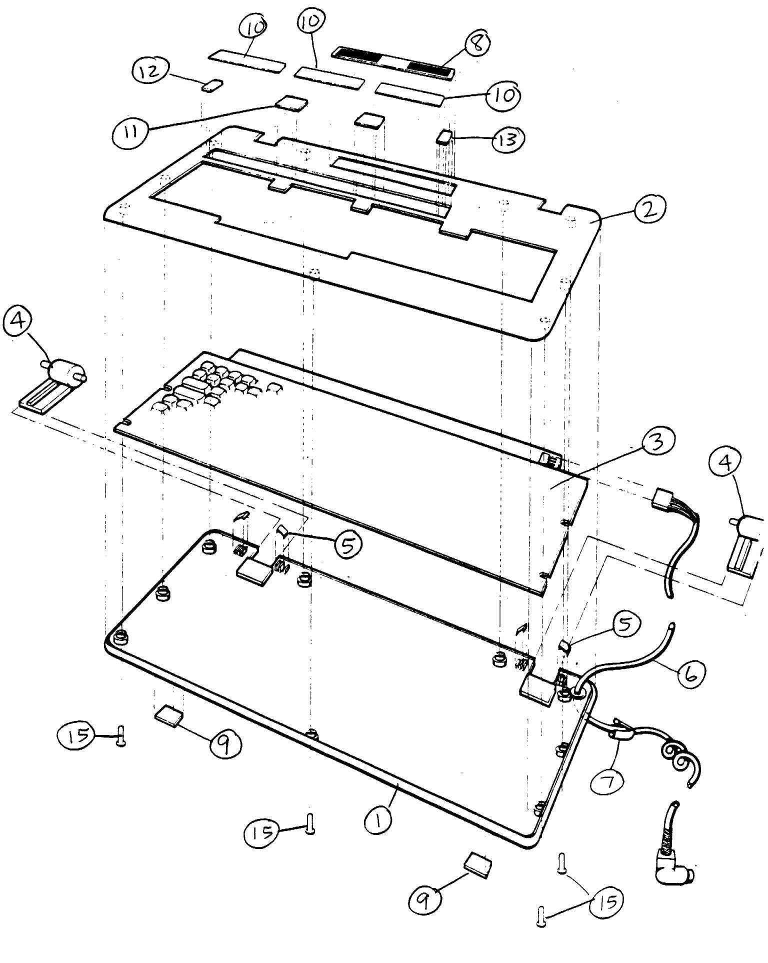


Exploded View, Card Cage Assembly

Parts List

Keyboard Assembly, Model 2000 Microcomputer

Item	Sym	Description	Part Number
1	1	Case, Keyboard Bottom	8719335
2	1	Case, Keyboard Top	8719334
3	1	Keyboard PCB Assembly	8080033
4	2	Support, Keyboard	8719336
5	4	Spring, Keyboard Support	8739014
6	1	Cable Assembly, Keyboard	8709472
7	1	Strain Relief, Cable	8590145
8	1	Logo	8719329
9	2	Pad, Keyboard Friction	8591004
10	3	ID Card, Function Key	87891012
11	1	Center Guide, ID Card	8719371
12	1	Left Guide, ID Card	8719373
13	1	Right Guide, ID Card	8719372
14	4	Screw, #6 x 1/2" PPH PTF Zn	8569079
15	5	Screw, #6 x 7/16" PPH PTF Zn	8569229



Exploded View, Keyboard Assembly

8.3 Display Unit

For the exploded view/parts listing for the display monitor,refer to the addendum sections to the Model 2000 computer. These sections contain detailed exploded views and parts list for both the monochrome and color monitor.

9.1 Internal 128K Expansion RAM

9.1.1 Introduction

The standard 128K word memory capacity of the Model 2000 may be extended to 256K words without using any option card slots by the addition of the 128K word Internal Expansion RAM board. This board is configured, with parity, to reside from address 20000H to 3FFFFH.

9.1.2 Theory Of Operation

There are eighteen high speed dynamic Random Access Memories (RAM's) on the 5.8 inch by 2.5 inch printed circuit board which makes up the Internal Expansion RAM board. Each RAM device is organized as 65,536 one bit words with a maximum access time of 150 nanoseconds. Bulk decoupling of the +5 volt power bus to the RAM's is provided by 100 microfarad, 6.3 volt dipped tantalum electrolytic capacitors. Also, each device is decoupled with a 0.1 microfarad capacitor across its Vcc (pin 8) and ground (pin 16) pins.

Interface to memory control and timing logic is accomplished through 40-pin right angle pin header (J13) on the Internal Expansion RAM board which mates with the right angle receptacle (P13) on the System RAM board. The following table defines the pin assignments on the interface connector (J13).

9.1.3 Signal Definition

The following list defines each signal available on the Internal Expansion RAM connector. For specific memory control and timing specifications see section   of the Main Logic Board theory of operation.

WORD SEGMENT	UPPER	LOWER
Column Address Select	CASU*	CASL*
Data Input Parity	DIPU	DIPL
Data Output Parity	DOPU	DOPL
Write Input	WR1*	
Row Address Select	RAS1*	
8-bit Memory Address Bus	DMEMA00-DMEMA07	
16-bit Memory Data Bus	IB00-IB15	

9.1.4 Troubleshooting

Memory Read or Write errors can be determined by using the memory diagnostic routines that are available for the Model 2000.

After iniatilizing the test program, a top of memory algorithm is executed to determine how much memory has been installed in the Model 2000 under test. If the response to the memory size inquiry does not agree with the amount of memory the user has installed, it can be assummed that either the memory installation was not performed correctly or the memory boards installed are deffective. The user should check all connectors to insure proper and complete mating before attempting to isolate a defective board and/or component.

Once the user is confident of the installation integrity, the memory diagnostic test may be run. There are three tests that are available: a read/write data test; a long modified address test and a short modified address test.

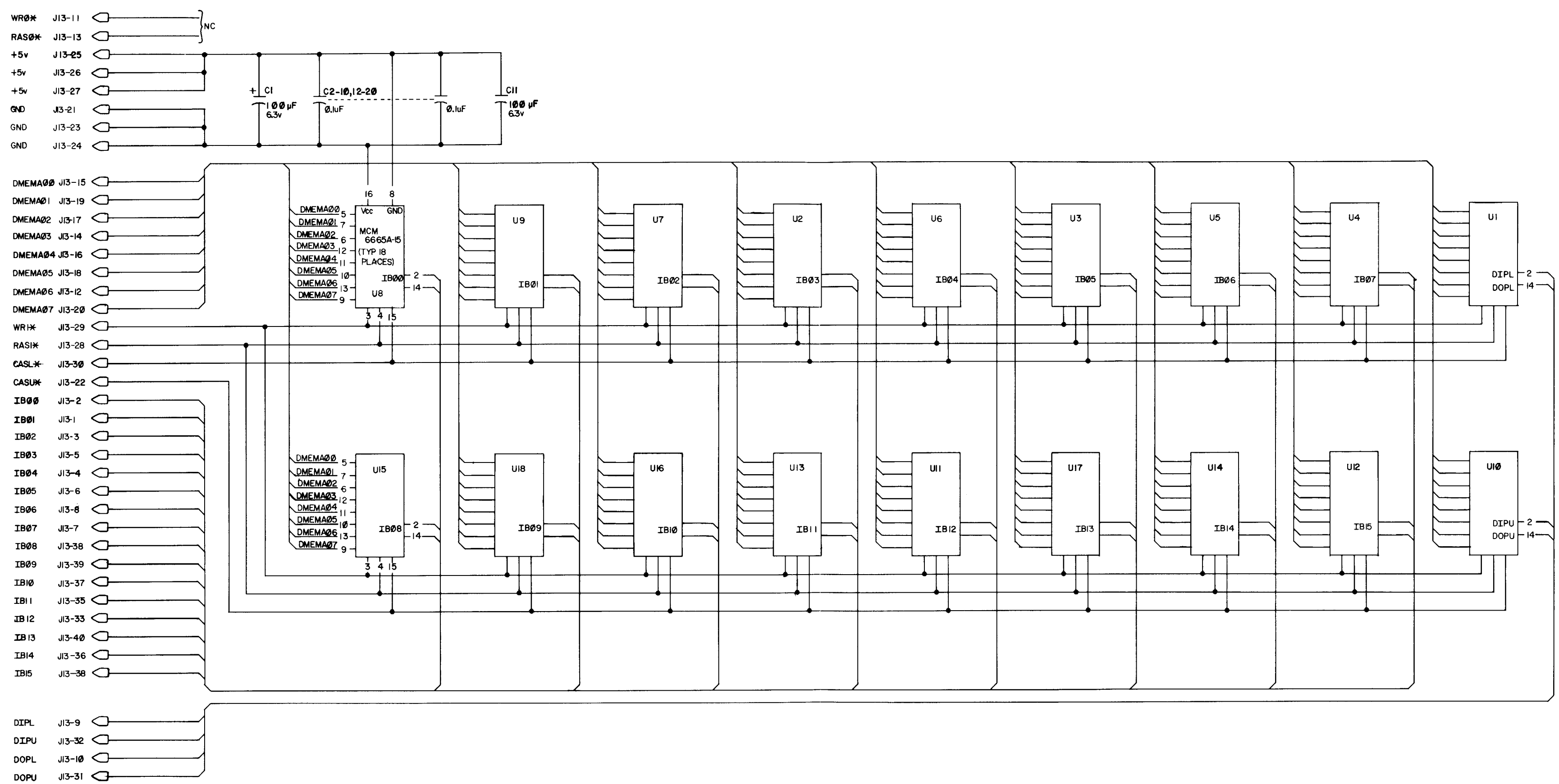
The data test writes a known data pattern to all memory locations. The data is then read back and compared to the known data pattern for errors. Errors generated by this test would indicate a problem either on the data/address bus interface to memory or with the decoders associated with the memory array.

The modified address test has two versions: the long test will test the RAM 65,536 times per pass (0000H-FFFFH) and the short test will test the RAM 256 times per pass (0000-00FF). The number of tests per pass is determined by a 16-bit mask register which is incremented by one for each write/read cycle through the entire memory array (i.e., 00000H-7FFFFH for 512K). The data pattern that is written is the result of the exclusive-OR of the high address segment register (16-bit) with the result of the exclusive-OR of the lower address segment or offset (16-bit) and the mask register. This data pattern is written through the memory array and then read and compared to check for accuracy. Errors that occur will be listed individually in the error table that specifies the data written, the data read, the exclusive-OR of the data written and the data read, and the address where the error occurred. In most cases, this will indicate which RAM chip in a particular bank has failed.

It is recommended that all three RAM tests should be used to verify correct operation of the RAM installed in the unit. Although these tests do not exercise every combination of bits that can be written throughout the full RAM capacity, they exercise enough write/read operations to achieve a fairly reliable test of memory I/0 and data recovery to isolate most common memory failures. A complete test that exercises every bit in an array is impractical because of the extreme number of bit combinations, especially in larger memory arrays. For a 16-bit system, there are $16(2^n)$ combinations, where n equals the memory size (e.g., 128K,256K,512K), that must be written, read and compared to complete the full test. In comparison, the modified address method reduces the amount of time it takes to complete a pass but even the long modified address test on a 512K memory array will take approximately 30 hours to complete.

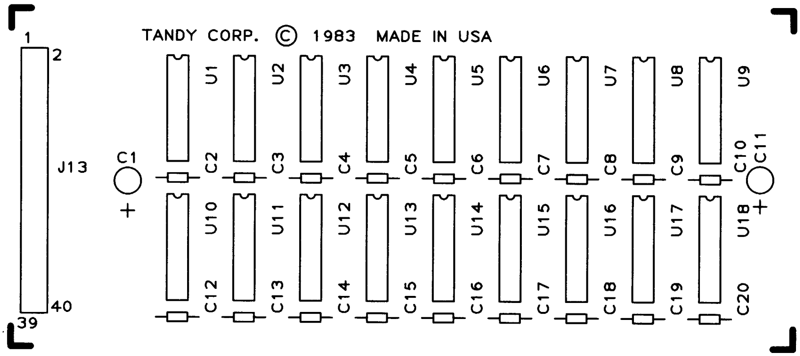
PIN #	SIGNAL	PIN #	SIGNAL
01	IB01	02	IB00
03	IB02	04	IB04
05	IB03	06	IB05
07	IB07	08	IB06
09	DIPL	10	DOPL
11	NO CONNECTION	12	DMEMA06
13	NO CONNECTION	14	DMEMA03
15	DMEMA00	16	DMEMA04
17	DMEMA02	18	DMEMA05
19	DMEMA01	20	DMEMA07
21	GROUND	22	CASU*
23	GROUND	24	GROUND
25	+5 VOLTS	26	+5 VOLTS
27	+5 VOLTS	28	RAS1*
29	WR1*	30	CASL*
31	DOPU	32	DIPU
33	IB12	34	IB15
35	IB11	36	IB14
37	IB10	38	IB08
39	IB09	40	IB13

TABLE 1. J13 PIN ASSIGNMENTS
INTERNAL EXPANSION RAM TO SYSTEM RAM INTERFACE

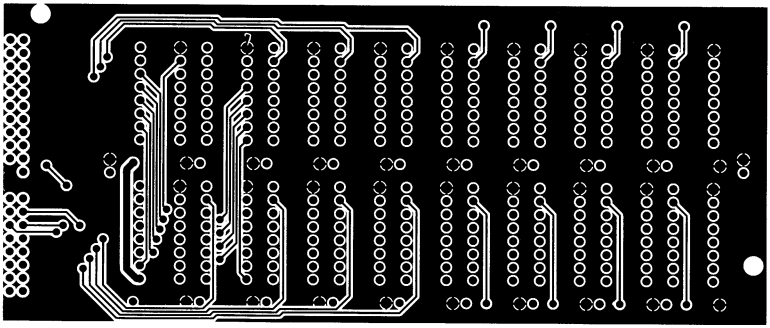


Schematic 8000205, 128K Internal RAM Expansion PCB

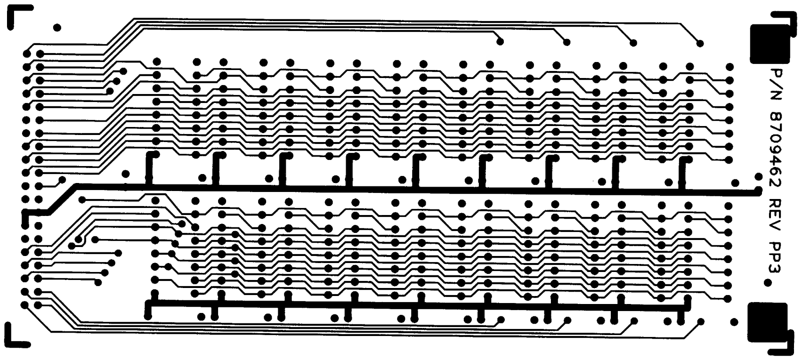
Schematic 8000205, 128K Internal RAM Expansion PCB



Component Layout 1700252, Internal RAM Expansion PCB



Circuit Trace 1700252, 128K Int RAM PCB
Component Side



Circuit Trace 1700252, 128K Int RAM PCB
Circuit Side

9.2 External Memory Board

The Model 2000 Expansion Memory Board (EXP MEM BD) is an optional plug-in board. Each board provides either 128K or 256K bytes of memory. The Model 2000 will accommodate up to three of these boards: two with a maximum of 256K bytes and the third with 128K bytes. This will bring the total Model 2000 RAM capacity to 896K bytes. Some features of the Exp Memory Board are independent on-board refresh control, delay line timing control, and byte-wide single-bit error detection. The block diagram of the EXP MEM BD is shown in Figure 9-1.

9.2.1 Memory Array

The memory array is made up of 64K x 1 Dynamic RAM ICs with 150 nanosecond access time. These RAM ICs are arranged into four groups of 9 ICs each; low word - high and low byte, and high word - low and high byte (see Figure 9-1). In each of the four groups, eight of the RAMs are for the stored data and one is for the error detection or parity bit. The data bus groups together the two high bytes D8 - D15 and the two low bytes D0 - D7. Each byte group has its own Model 2000 / Ext Memory Board interface. This conforms to the Model 2000 Bus / 80186 architectural feature of byte accesses. Physically, the internal data bus is accomplished by connecting the corresponding bits of each byte together. Additionally, the input and output data pins of each individual RAM IC are connected together. (This is allowed because single operation accesses only are allowed). The interface circuity consists of input buffers and output latches. Latching the output data prevents the stretching of the internal READ cycle until the CPU is complete and therefore allows the read and write cycles to be of equal length. And, most importantly, it allows refresh cycles to be added to any CPU access by inserting wait states.

9.2.2 Address Logic

The EXP MEM BD uses all twenty address bits of the Model 2000 bus, A0 thru A19. A19 and A18 are used for board selection, A17 is used for word selection, A16 thru A1 are the RAM address inputs, and A0, in conjuction with BHE (80186 signal), is used for byte selection.

A19,A18

These two address bits are used by the Model 2000 to decode which group of four 256K bytes (128K words) is being accessed. On the EXP MEM BD, they generate the signal SELECT. The circuit consists of U64 (a 74F138 3-to-8 decoder) used as a 2-to-4 decoder. A18 and A19 are the decoded inputs and MC0, MC1 (80186 memory chip selects) are the enables. Three of the four possible decoded outputs are provided as jumper selectable outputs - B1, B2, and B3. One of the jumper options has to be made before the board will operate. For the first board in the system, the jumper must be between B1 and S; for the second board between B2 and S, and for the third board between B3 and S. See Figure 9-2 for more details.

A17

This address bit is combined with the RAM row address strobe RASP to select either the array high word (A17 true) or the array low word (A17 false). This takes place at U15.

A16 thru A1

These address bits are used by the RAM ICs to decode one of 64K internal memory locations. The RAM ICs, due to the number of pins, require the address bits to be divided into two groups and the groups loaded sequentially. These two groups are ROW address (loaded first) and COLUMN address (loaded second). The circuit that accomplishes this is composed of line receivers U68, U70 (74LS244s), and 2-to-1 multilpexers U67 and U69 (74F258s). The line receivers are always enabled. The multiplexers are enabled when ENRCAD* is true (low). The address group applied to the RAMs is determined by the logic level of MUX* - low (normal state) for row address, high (active state) for column address. The outputs of the decoders are routed to the RAM array through damping resistors (RP4). These resistors are shared by refersh address buffer U66.

9.2.3 Refresh Address

The 256 refresh address combinations are generated by an eight-bit counter U72. The clock for this counter is RFCNT* which occurs at the end of each refresh cycle. The counter works in the continuous mode, i.e. the counter counts 0, 1, ..254, 255, 0,..etc. The refresh address buffer U66 applies the current count to the array via the damping resistors RP4 when it is enabled by ENRFAD* being true (low) (ENRCAD will be false).

9.2.4 Memory Control

The Memory Control logic generates all the timing clocks/control strobes to access the memory, refresh the memory, and generate/check parity. A general description of the operational characteristics of the EXT MEM BD will set the stage for the more detailed individual circuit analysis that follows.

First, the EXT MEMORY BOARD has three modes of operation:

9.2.4.1 Memory access without refresh.

This mode has two variants. If it is a video access, refresh is inhibited. If it is a CPU access and CNT = 0, no refresh is required. RDY is set immediately.

9.2.4.2 Memory access with refresh

In this mode, the memory access is performed first and then followed by 1 to 16 refresh cycles. This is accomplished by holding the RDY cleared until the last refresh cycle and extending the CPU access. If it is a READ access, the output data is latched for the CPU at the end of the first cycle. (This is because the CPU will not READ the data until RDY is set).

9.4.2.3 Refresh only

In this mode, a memory access is taking place at an off-board memory location but a refresh cycle(s) is required. Therefore, a single refresh cycle is performed in parallel to the other access. Only a single refresh cycle is allowed because the RDY line cannot be controlled. The timing cycle for a read, write or refresh is the same. Only the decoded timing strobes are different. For instance, the difference between a read and a write is the presence of the write strobe to the array and the direction of the data flow. A refresh cycle inhibits CAS and selects the refresh address instead of the CPU addresses. A RAS only cycle is a refresh cycle to the RAM and no data is affected. A block diagram of the memory controller is shown in Figure 9-3.

GLOSSARY OF TERMS

The following will be helpful in understanding the remaining discusion.

RAS0* = Row Address Strobe for lower word. A17=0.
= RASP * A17/ + RFRAS
RAS1* = Row Address Strobe for upper word. A17=1.
= RASP * A17 + RFRAS
RASP = Row Address Strobe Prime. Basic strobe for RAS,RAS1.
RFRAS* = ReFresh RAS. RAS is row address strobe.
CASH* = Column Address Strobe, High byte.
= CASP * BHE
CASL* = Column Address Strobe,Low byte.
= CASP * A0
CASP = Column Address Strobe Prime. Basic strobe for CASH,CASL.
MUX* = Row column adderss select.
WRITEH* = WRITE strobe,High byte.
WRITEL* = WRITE strobe,Low byte.
WRITEP* = Write Prime.
LRFSH = Latched Refresh. Indicates the current timing cycle is for refresh.
ENRCAD* = ENable Row Column ADdress. Goes to U67, U69.

ENRFAD* = ENable ReFresh ADdress. Goes to U66.
RASCLR* = RAS CLeaR. Terminates RASP.
RFSRT* = ReFresh StaRT. Restarts a timing cycle.
RFCNT* = ReFresh cycle CouNT. Counts down CNT.
CNT = Refresh cycles due CouNT.
SCNT = Synchronized CNT.
STROBE* = parity interrupt timing strobe.
SELECT = board SELECTed by address. Access starts when MREAD or MWRITE occur.
PARH = PARity High. Parity has occured on high byte.
PARL = PARity Low. Parity has occured on low byte.

9.2.5 Timing Sequence Generator

The timing sequence generator consists of delay lines U32, U49, half the J-K flip-flop U48, and the AND-OR gate U47. The timing sequence is started by triggering the flip-flop by the leading edge of the signal MEMCYC. This sets Q low. This low appears 80 nanoseconds later from the delay line at the clear of the flip-flop and sets Q high. Thus, an 80 nanosecond negative pulse is initiated down the delay line, creating a series of timing pulses - once. If the conditions are right, a short pulse RFSRT is created at the 300 nanosecond tap to begin the cycle over.

The signal MEMCYC/ is created under two conditions. The first is a memory access - that is, SELECT, MREAD and MWRITE are true.

The second condition is the need for a refresh cycle. If SCNT is true but SELECT is false, the next MREAD or MWRITE creates a MEMCYC. The signal RFSRT will add cycles to the original cycle if and only if SELECT is true and as long as SCNT is true. These added cycles are refresh cycles and can be added only if the signal BUSARDY (CPU "wait") can be controlled.

9.2.6 Refresh Counter

The refresh method is basically a single cycle every 16 microseconds. The exception is that the refresh cycles are allowed to stack up until a convenient time when a refresh burst occurs that is equal in number to the deficit amount. The refresh counter circuitry consists of the refresh period counter U45, U61, and the deficit counter U27, U11, and 1/6 of U46. The refresh counters U45 and U61 provide a constant time tick (125 nanosecond negative pulse) every 16.0 microseconds to U27. This causes U27 to count up. Every time a refresh cycle is performed, a signal RFCNT is applied which causes U27 to count down. The CNT logic U11 samples the output of U27 and, if the count is greater than zero, CNT is true.

9.2.7 Refresh Count Synchronizer

The output signal from the refresh counter CNT needs to be synchronized with MREAD or MWRITE to prevent CNT from affecting the access status after the cycle has started (RDY already set). This is accomplished by the two flip-flops

U28(1/2), U12(1/2), 3/4 U13, 1/4 U29, and 1/6 U65. Working backward, the output SCNT is the logical AND of the synchronized CNT (U29.11) and the enable RFINH/ (refresh inhibit- refresh not allowed during video accesses). The synchronized CNT signal is the logical OR of two versions of synchronized CNT - one that is latched and one that reflects the real time status of CNT. The latched version of CNT is required so that SCNT becomes true only between memory cycles. Once a refresh cycle is started, denoted by the presence of LRFSH (latched refresh), the latched version of CNT is cleared and replaced by the real-time version which will allow SCNT to go false when CNT = 0. (The latched version will not update until next ALE which will not occur until CNT = 0 which allows the memory access cycle to finish and proceed to the next ALE). There are two latches instead of one because of the special sequence where a non-SELECTed refresh cycle preceeds a normal access. In this case, the delayed strobe D300 is active when the new access is started. This causes the decoder to latch a refresh cycle and hang-up the sequence by failing to set RDY. By making the sync chain two flip-flops, only alternate bus accesses can cause a refresh cycle.

9.2.8 Decoder

The decoder accepts the input timing signals from the timing generator and the status signals and creates the timing strobes for the MEMORY TIMING LOGIC. The decoders U30, U31, U42, and part of U71 are programmable logic arrays and contain proprietary information. Timing diagrams are shown in Figure 9-4.

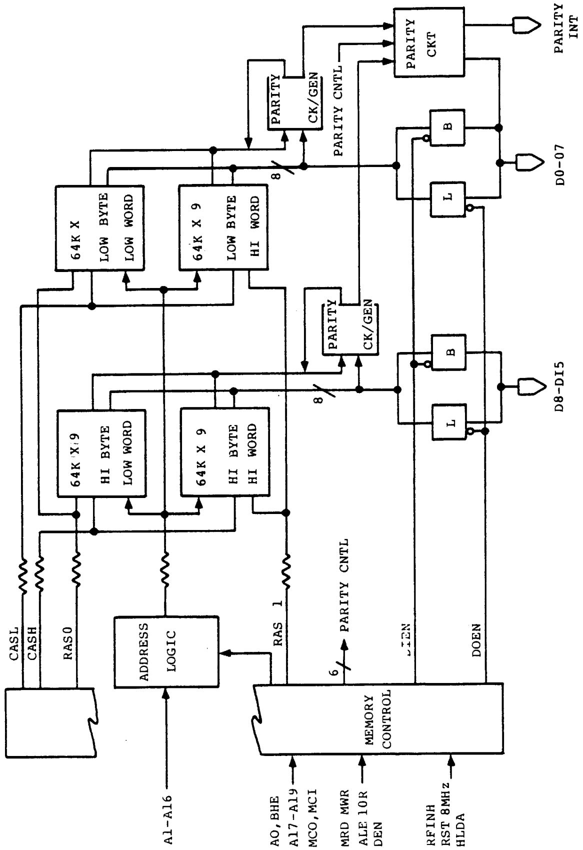


Figure 9-1. Block Diagram, External Memory Board

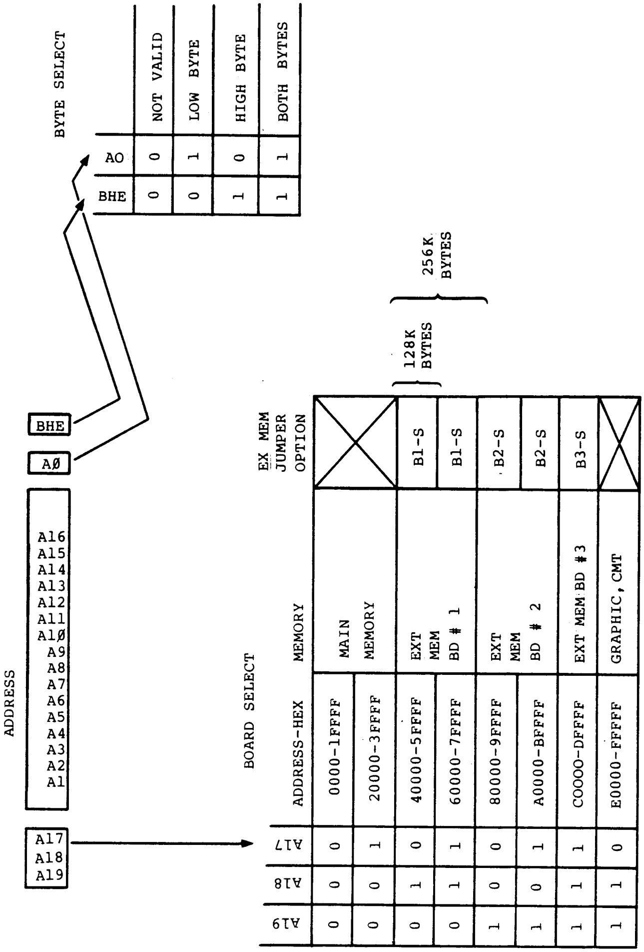


Figure 9-2. Board Select

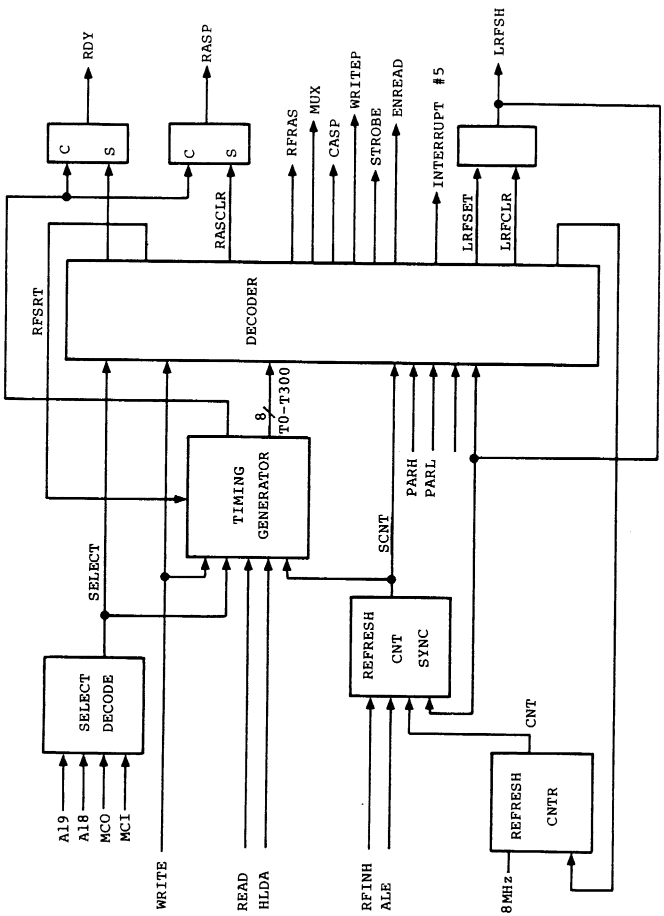


Figure 9-3. Memory Control Block Diagram

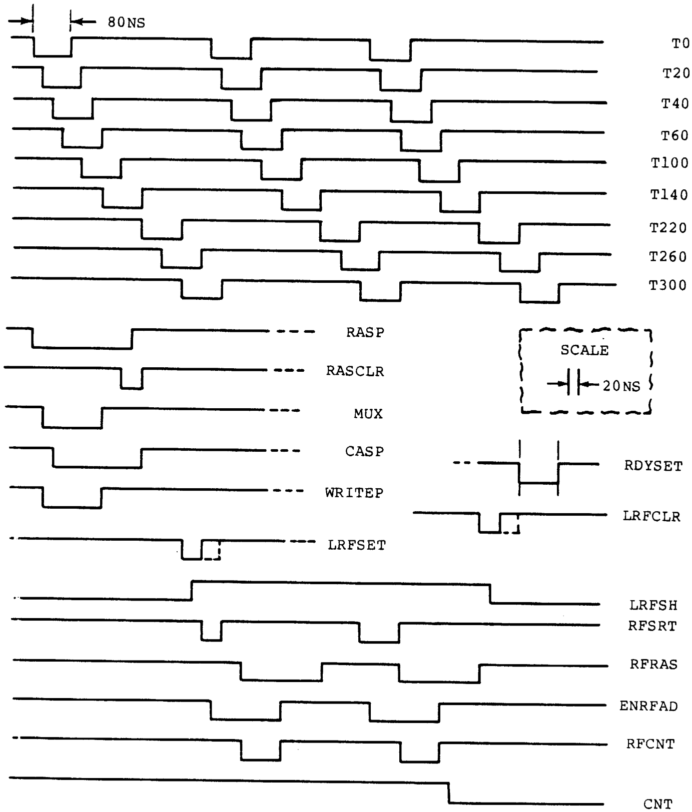


Figure 9-4. Normal Cycle Plus Refresh Cycle

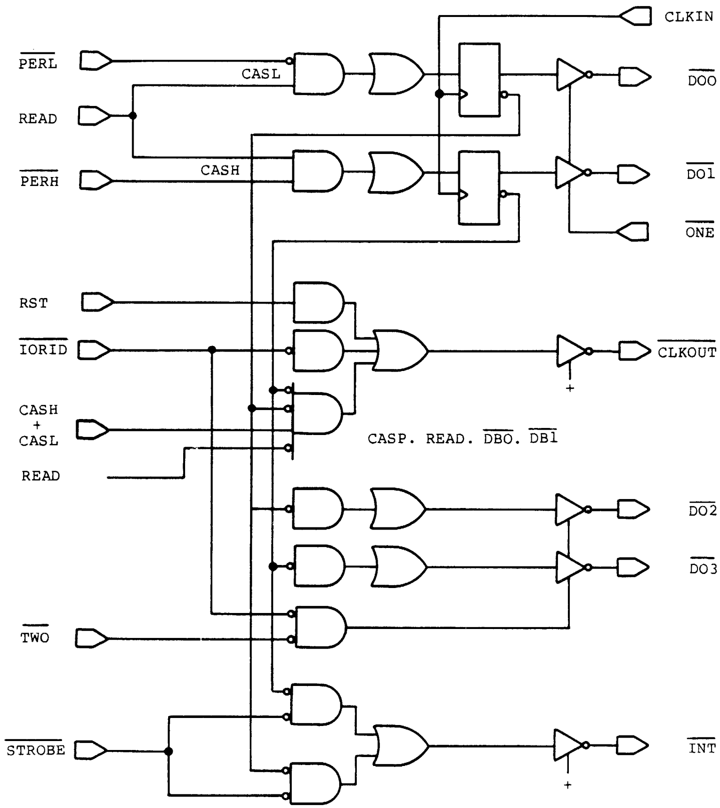
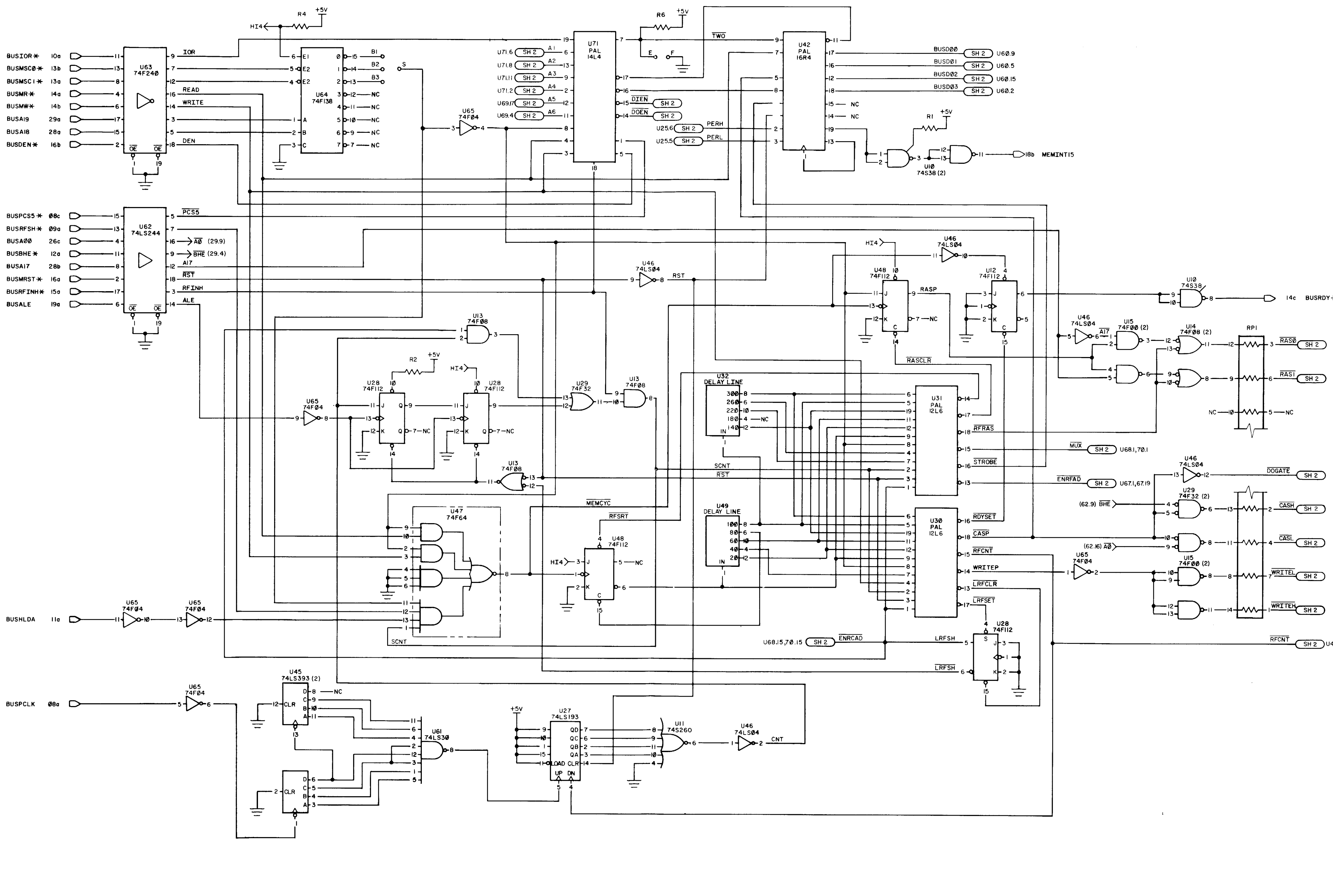
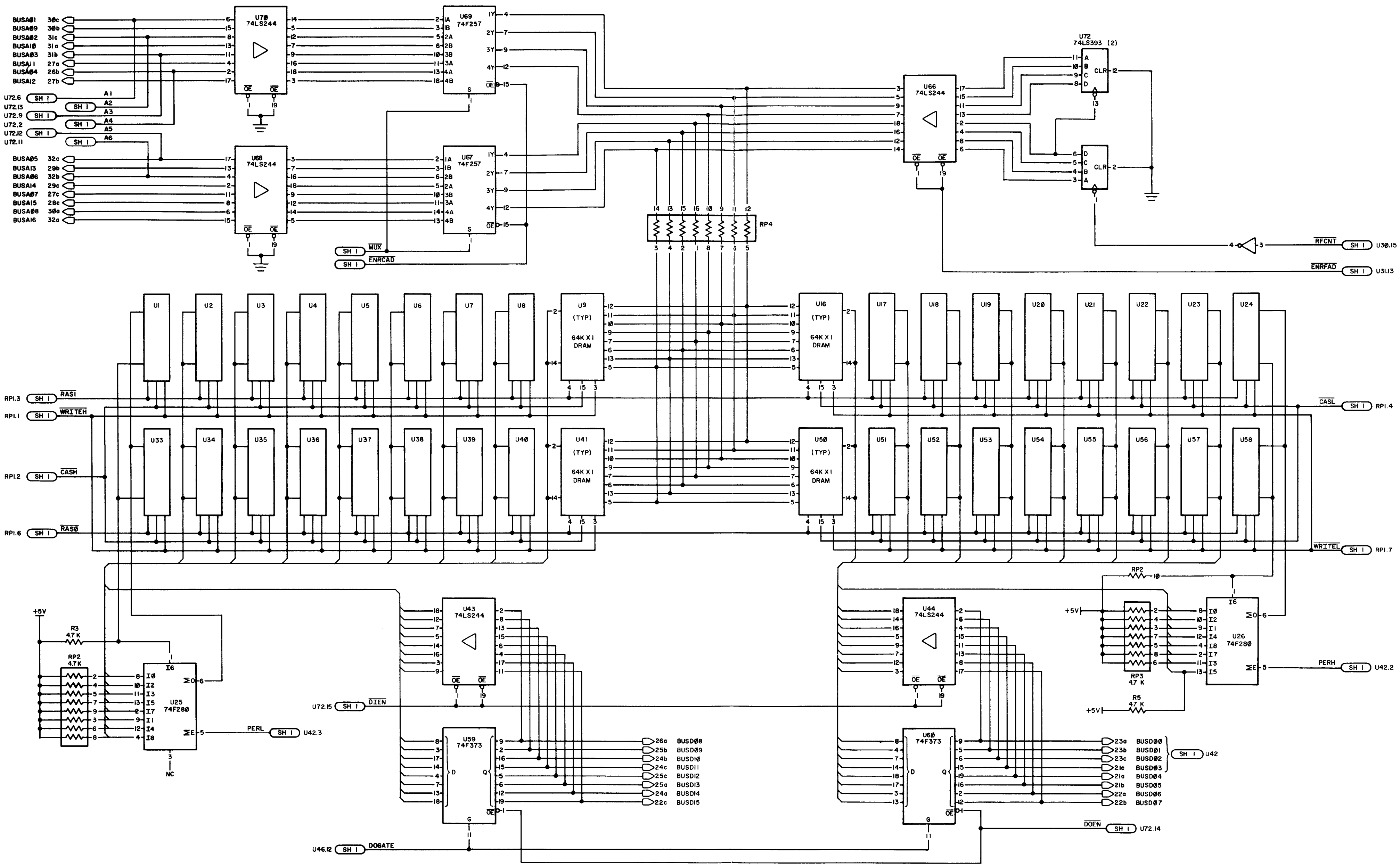


Figure 9-5. U42 Diagram



Schematic 8000218, 128/256K External RAM PCB Block Diagram
Page 1 of 2

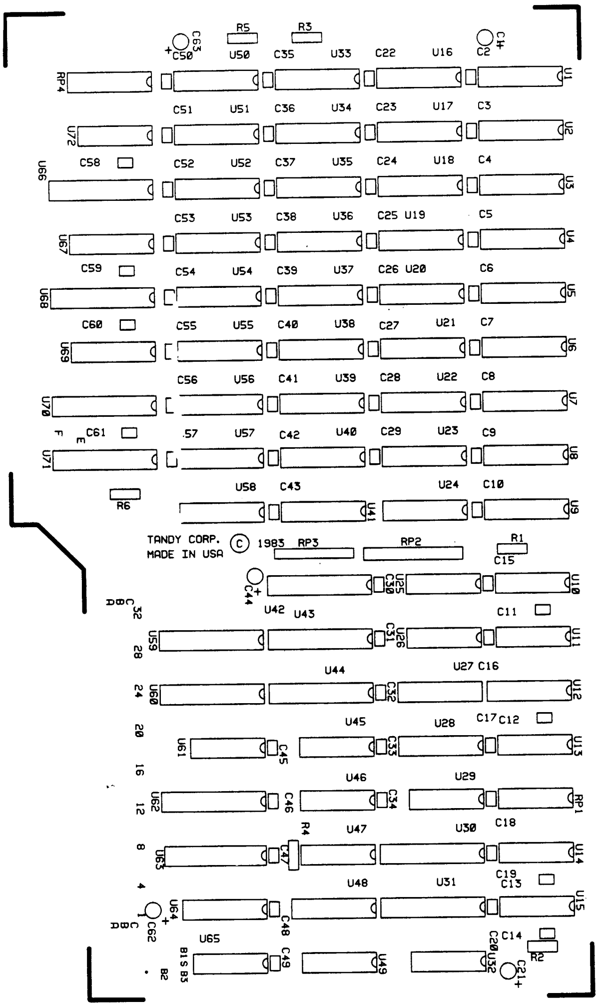
Schematic 8000218, 128/256K External RAM PCB Block Diagram
Page 1 of 2



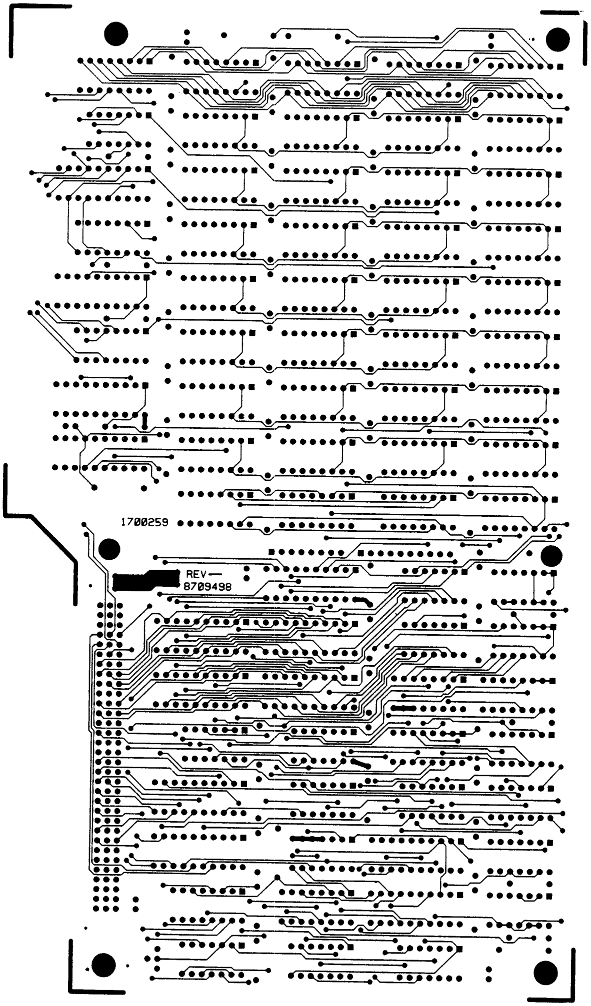
Schematic 8000218, 128/256K External RAM PCB Block Diagram

Page 2 of 2

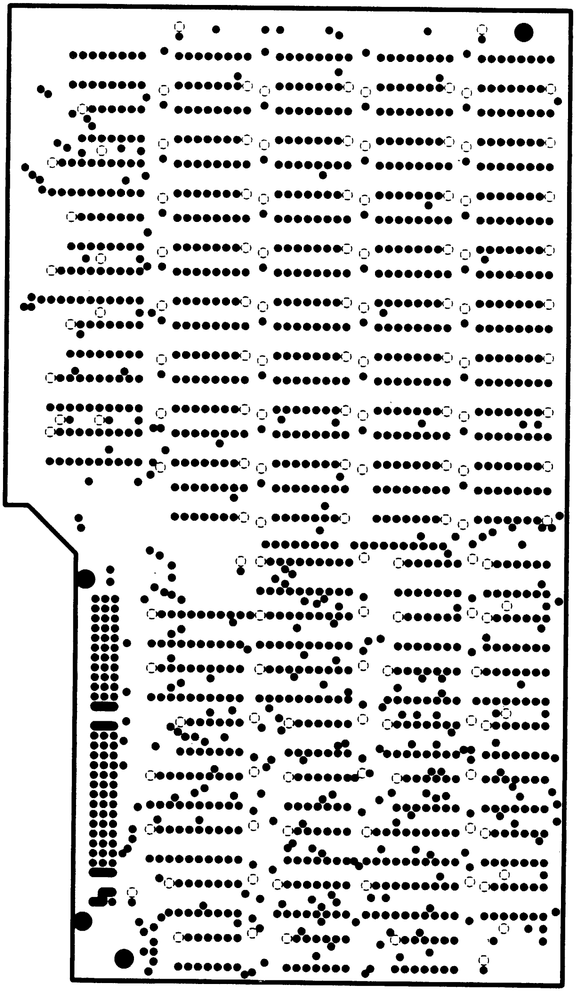
Schematic 8000218, 128/256K External RAM PCB Block Diagram
Page 2 of 2



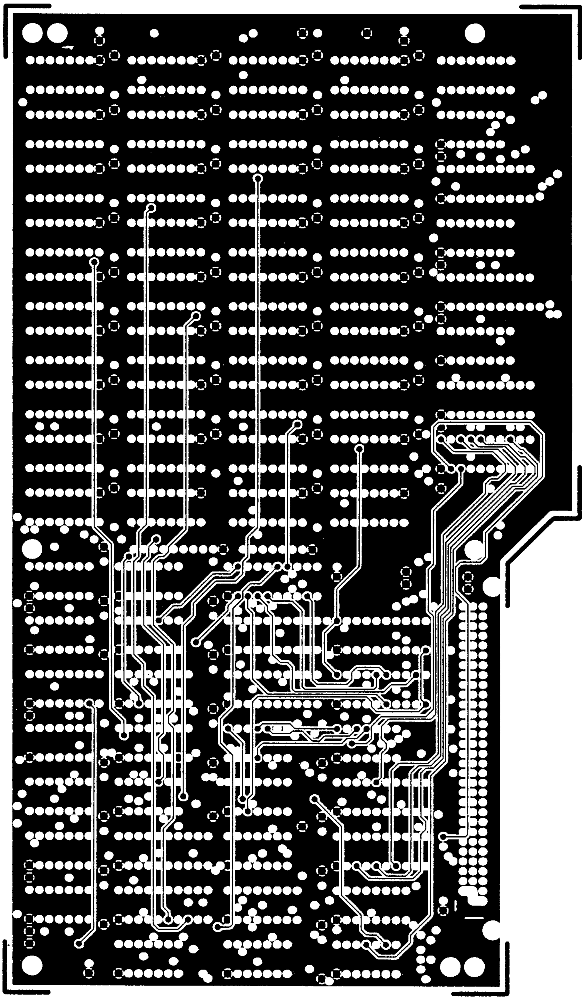
Component Layout, External 256K RAM Memory Expansion 889B011



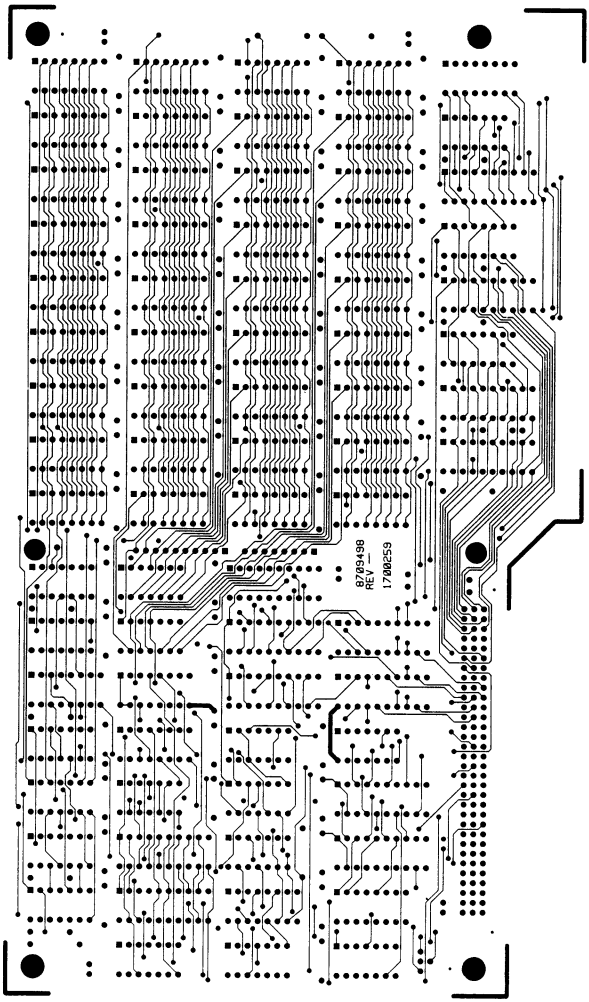
Circuit Trace, External 256K RAM PCB Assembly 889B011
Component Side



Circuit Trace, External 256K RAM PCB 899B011
Ground Plane



Circuit Trace, External 256K RAM PCB Assembly 889B011
Power Plane



Circuit Trace, External 256K RAM PCB Assembly 889B011
Component Side

Parts List - 26-5161 External RAM Board (11-14-83)

PCB 889B011 256K Board Populated with 128K

Item	Sym	Description	Part Number
1	1	External 256K Logic PCB	8709498
2	6	Staking Pins, A thru F	8529014
3	36	Socket, 16-Pin DIP (U1-9,16-24, 33-41,50-58)	8509003
4	4	Socket, 20-Pin DIP (U30,31,42,71)	8509009
5	1	Connector, 96 Pin Euro Female (J1)	8519181
6	2	Screw, #2-56 x 3/8" PPH (J1)	8569201
7	2	Nut, #2-56 (J1)	8579042
8	1	Chassis, 128/256K Memory	8729278
9	2	Nylatch Plunger	8590149
10	2	Nylatch Grommet	8590148
11	6	Screw, #4-40 x 3/16" PPH MS	8569220
12	1	Label, Serial	87891041
	C1	Capacitor, 100 mfd, 6.3V Tant. Rad.	8337100
	C2	Capacitor, .1 mfd, 50V Mono	8374101
	C3	Capacitor, .1 mfd, 50V Mono	8374101
	C4	Capacitor, .1 mfd, 50V Mono	8374101
	C5	Capacitor, .1 mfd, 50V Mono	8374101
	C6	Capacitor, .1 mfd, 50V Mono	8374101
	C7	Capacitor, .1 mfd, 50V Mono	8374101
	C8	Capacitor, .1 mfd, 50V Mono	8374101
	C9	Capacitor, .1 mfd, 50V Mono	8374101
	C10	Capacitor, .1 mfd, 50V Mono	8374101
	C11	Capacitor, .1 mfd, 50V Mono	8374101
	C12	Capacitor, .1 mfd, 50V Mono	8374101
	C13	Capacitor, .1 mfd, 50V Mono	8374101
	C14	Capacitor, .1 mfd, 50V Mono	8374101
	C15	Capacitor, .1 mfd, 50V Mono	8374101
	C16	Capacitor, .1 mfd, 50V Mono	8374101
	C17	Capacitor, .1 mfd, 50V Mono	8374101
	C18	Capacitor, .1 mfd, 50V Mono	8374101
	C19	Capacitor, .1 mfd, 50V Mono	8374101
	C20	Capacitor, .1 mfd, 50V Mono	8374101
	C21	Capacitor, 100 mfd, 6.3V Tant. Rad.	8337100
	C22	Capacitor, .1 mfd, 50V Mono	8374101
	C23	Capacitor, .1 mfd, 50V Mono	8374101
	C24	Capacitor, .1 mfd, 50V Mono	8374101
	C25	Capacitor, .1 mfd, 50V Mono	8374101
	C26	Capacitor, .1 mfd, 50V Mono	8374101
	C27	Capacitor, .1 mfd, 50V Mono	8374101
	C28	Capacitor, .1 mfd, 50V Mono	8374101

Parts List - 26-5161 External RAM Board

PCB 889B011 256K Board Populated with 128K

Item	Sym	Description	Part Number
	C29	Capacitor, .1 mfd, 50V Mono	8374101
	C30	Capacitor, .1 mfd, 50V Mono	8374101
	C31	Capacitor, .1 mfd, 50V Mono	8374101
	C32	Capacitor, .1 mfd, 50V Mono	8374101
	C33	Capacitor, .1 mfd, 50V Mono	8374101
	C34	Capacitor, .1 mfd, 50V Mono	8374101
	C35	Capacitor, .1 mfd, 50V Mono	8374101
	C36	Capacitor, .1 mfd, 50V Mono	8374101
	C37	Capacitor, .1 mfd, 50V Mono	8374101
	C38	Capacitor, .1 mfd, 50V Mono	8374101
	C39	Capacitor, .1 mfd, 50V Mono	8374101
	C40	Capacitor, .1 mfd, 50V Mono	8374101
	C41	Capacitor, .1 mfd, 50V Mono	8374101
	C42	Capacitor, .1 mfd, 50V Mono	8374101
	C43	Capacitor, .1 mfd, 50V Mono	8374101
	C44	Capacitor, 100 mfd, 6.3V Tant. Rad.	8337100
	C45	Capacitor, .1 mfd, 50V Mono	8374101
	C46	Capacitor, .1 mfd, 50V Mono	8374101
	C47	Capacitor, .1 mfd, 50V Mono	8374101
	C48	Capacitor, .1 mfd, 50V Mono	8374101
	C49	Capacitor, .1 mfd, 50V Mono	8374101
	C50	Capacitor, 100 mfd, 6.3V Tant. Rad.	8337100
	C51	Capacitor, .1 mfd, 50V Mono	8374101
	C52	Capacitor, .1 mfd, 50V Mono	8374101
	C53	Capacitor, .1 mfd, 50V Mono	8374101
	C54	Capacitor, .1 mfd, 50V Mono	8374101
	C55	Capacitor, .1 mfd, 50V Mono	8374101
	C56	Capacitor, .1 mfd, 50V Mono	8374101
	C57	Capacitor, .1 mfd, 50V Mono	8374101
	C58	Capacitor, .1 mfd, 50V Mono	8374101
	C59	Capacitor, .1 mfd, 50V Mono	8374101
	C60	Capacitor, .1 mfd, 50V Mono	8374101
	C61	Capacitor, .1 mfd, 50V Mono	8374101
	C62	Capacitor, .1 mfd, 50V Mono	8374101
	C63	Capacitor, 100 mfd, 6.3V Tant. Rad.	8337100
	R1	Resistor, 1 kohm, 1/4W 5%	8207210
	R2	Resistor, 1 kohm, 1/4W 5%	8207210
	R3	Resistor, 4.7 kohm, 1/4W 5%	8207247
	R4	Resistor, 1 kohm, 1/4W 5%	8207210
	R5	Resistor, 4.7 kohm, 1/4W 5%	8207247
	R6	Resistor, 1 kohm, 1/4W 5%	8207210

Parts List - 26-5161 External RAM Board

PCB 889B011 256K Board Populated with 128K

Item	Sym	Description	Part Number
	RP1	Resistor Pak, 56 ohm, 14-Pin DIP	8
	RP2	Resistor Pak, 4.7 kohm, 10-Pin SIP	8294247
	RP3	Resistor Pak, 4.7 kohm, 8-Pin SIP	8292246
	RP3	Resistor Pak, 27 ohm, 16-Pin DIP	8290027
	U10	IC, 74S38, Quad 2-Input NAND	8010038
	U11	IC, 74S260, Dual 5-Input NOR	8010260
	U12	IC, 74F112, Flip-Flop	8015112
	U13	IC, 74F08, Quad 2-Input AND	8015008
	U14	IC, 74F08, Quad 2-Input AND	8015008
	U15	IC, 74F00, Quad 2-Input NAND	8015000
	U25	IC, 74S280, Parity Generator	8010280
	U26	IC, 74S280, Parity Generator	8010280
	U27	IC, 74ALS193, Counter	8025193
	U28	IC, 74F112, Flip-Flop	8015112
	U29	IC, 74F32, Quad 2-Input OR	8015032
	U30	IC, PAL12L6	8040126
	U31	IC, PAL12L6	8040126
	U32	IC, Delay Line, 200 nsec	8429010
	U33	IC, 6665-150, DRAM	8041665
	U34	IC, 6665-150, DRAM	8041665
	U35	IC, 6665-150, DRAM	8041665
	U36	IC, 6665-150, DRAM	8041665
	U37	IC, 6665-150, DRAM	8041665
	U38	IC, 6665-150, DRAM	8041665
	U39	IC, 6665-150, DRAM	8041665
	U40	IC, 6665-150, DRAM	8041665
	U41	IC, 6665-150, DRAM	8041665
	U42	IC, PAL16R4	8040164
	U43	IC, 74ALS244, Octal Buffer	8025244
	U44	IC, 74ALS244, Octal Buffer	8025244
	U45	IC, 74LS393, Counter	8020393
	U46	IC, 74LS04, Hex Inverter	8020004
	U47	IC, 74F64, AND-OR Inverter	8015064
	U48	IC, 74F112, Flip-Flop	8015112
	U49	IC, Delay Line 100 nsec	8429024
	U50	IC, 6665-150, DRAM	8041665
	U51	IC, 6665-150, DRAM	8041665
	U52	IC, 6665-150, DRAM	8041665
	U53	IC, 6665-150, DRAM	8041665
	U54	IC, 6665-150, DRAM	8041665
	U55	IC, 6665-150, DRAM	8041665

Parts List - 26-5161 External RAM Board

PCB 889B011 256K Board Populated with 128K

Item	Sym	Description	Part Number
	U56	IC, 6665-150, DRAM	8041665
	U57	IC, 6665-150, DRAM	8041665
	U58	IC, 6665-150, DRAM	8041665
	U59	IC, 74F373, Octal Latch	8015373
	U60	IC, 74F373, Octal Latch	8015373
	U61	IC, 74LS30, 8-Input NAND	8020030
	U62	IC, 74LS244, Octal Buffer	8025244
	U63	IC, 74F240, Octal Buffer	8015240
	U64	IC, 74F138, Decoder	8015138
	U65	IC, 74F04, Hex Inverter	8015004
	U66	IC, 74LS244, Octal Buffer	8025244
	U67	IC, 74LS257, Multiplexer	8015257
	U68	IC, 74LS244, Octal Buffer	8025244
	U69	IC, 74F257, Multiplexer	8015257
	U70	IC, 74LS244, Octal Buffer	8025244
	U71	IC, PAL14L4	8040104
	U72	IC, 74LS393, Counter	8020393

9.3 Hi-Resolution Graphics Option 640 X 400 X 8

The High Resolution (Hi-Res) Graphics option for the Model J provides 640 X 400 pixels on the VM-1 or CM-1 video monitors. The board contains 96K bytes of high speed RAM for storage of graphics data, and a user programmable color palette for color assignment. The board resides in the lower slot of the Model 2000 card cage.

9.3.1 Memory Organization

The graphics memory is organized in a planer fashion. Up to three 16K by 16 memory planes may be installed. If two-color video is required, then PLANE 0 is installed. Installing PLANE 1 and PLANE 2 provides 8-color video.

There is a 6-bit STATUS PORT on the graphics board to inform the programmer how many planes are installed. See STATUS PORT DESCRIPTION for more information.

All three memory planes occupy the same physical address space. To determine which of the three planes the CPU is reading from or writing to, a PLANE SELECT REGISTER must be set up prior to accessing graphics RAM. See the section entitled PLANE SELECT REGISTER (9.3.4).

The memory starts at address E0000H in the IAPX186 Processor address space. This address corresponds to the UPPER LEFT of the video screen. The next address is to the right. The lower right corner is the last address. The full screen requires 32,000 bytes or 16,000 words to fully describe a single plane. The board responds to both byte and word accesses. Word accesses must be on even addresses only. Either the high byte or the low byte may be transferred during byte accesses.

The graphics memory may be accessed at any time. The Hi-Res circuitry uses WAIT states to synchronize the data transfer between CPU and graphics memory. The average speed at which data may be transferred is 16 bits per microsecond.

9.3.2 Pixel Mapping

Each bit in the graphics memory represents a dot (pixel) on the video screen. The MSB of a byte or word is the LEFTMOST pixel. The LSB is the last pixel to the right.

9.3.3 Color Palette - Changing a Pixel Color

The Hi-Res board contains a high speed static RAM which serves as the color palette. The palette "looks up" a color by forming an address using the data from each installed plane. PLANE 0 is pallette address bit A0, PLANE 1 is palette address bit A1, and PLANE 2 is palette address bit A2. Palette address bit A3 is always tied high, a 1. If a plane is NOT installed, the palette address bit is a 1. Therefore, if PLANE 0 contained a 1, PLANE 1 a 0, and PLANE 2 a 0, the palette would "look-up" the color at address 1001 in the palette memory.

Since there are three memory planes (maximum), there can be up to eight colors displayed at one time on the screen. The CM-1 color monitor can display 15 colors. Therefore, any of the available 15 colors, up to 8 at a time, can be displayed.

The CPU can write the palette to change the color lookup table. The palette is located in the Processor I/0 space, and is on word (even address) boundries. The Processor uses PCS3 as the I/0 port decode for graphics boards.

The palette appears to the programmer as 16 word addresses, starting at I/0 address 0180H. The palette is a WRITE-ONLY device. I/0 address 0180H is the first palette address, 0182H the second, etc. Data is stored in the palette on data bits D3-D0. The upper data bits are ignored. Remember that these addresses are not the same as the address formed to "look-up" a color for a particular pixel.

Although a program may access the palette anytime, it is possible to generate an undesirable "tear" or horizontal bar on the screen during a palette write from the CPU. To prevent the video monitor from doing this, the palette must be written to only during vertical blanking time. The SMC9007 Video Controller, used in the Model 2000, has a status register which reflects the status of vertical sync. Also, the 9007 can provide interrupts to the Processor each vertical sync. It is up to the individual programmer as to which is preferred.

The data in the palette is tied to the video guns of the CM-1 color monitor as shown in the table below. As can be seen, D0 controls the blue gun, D1 the green gun, D2 the red gun, and D3 the half intensity. A 1 in D3 is full intensity, a 0 half intensity. The following table shows possible colors versus data bits.

D3	D2	D1	D0	COLOR on CM-1
0	0	0	0	black
0	0	0	1	dark blue
0	0	1	0	dark green
0	0	1	1	dark yellow
0	1	0	0	dark red
0	1	0	1	dark magenta
0	1	1	0	dark cyan
0	1	1	1	gray
1	0	0	0	black
1	0	0	1	blue
1	0	1	0	green
1	0	1	1	yellow
1	1	0	0	red
1	1	0	1	magenta
1	1	1	0	cyan
1	1	1	1	white

9.3.4 Plane Select Register

Since the three memory planes the the Hi-Res board occupy the same address space, there must be some way to determine which one the CPU is trying to read from or write to. This is done by writing the proper data into the plane select register.

The plane select register is I/O mapped as address 01A0H. It is WRITE-ONLY. It is 6 bits wide on D0-D5. The register has 3 functions.

First, it selects which plane of memory the CPU has access to. Only one plane at a time may be selected. If more than one plane is selected, the register DESELECTS ALL PLANES.

Second, it determines if the graphics planes are displayed or "turned off". If they are turned off, the address into the palette will be 08H (the plane data forced to 0). This does NOT erase the data in the planes, but simply forces the palette address to see 08H.

Third, it determines if addresses into the palette are from the internal memory planes, or from the 9007 video memory. See DISPLAYING ALPHA-NUMERIC TEXT USING THE HI-RES BOARD for further information.

Below is a chart for the bits contained in the plane select register.

BIT	FUNCTION
0	Select plane 0
1	Select plane 1
2	Select plane 2
3	No connection
4	Graphics on/off
5	Graphics/Alpha switch
6 and 7	No connection

To select a particular plane, a 1 must be in the corresponding bit while the remaining two plane selects are a 0. If plane 1 is to be selected, then D0 and D2 would contain a 0, while D1 would contain a 1.

The graphics on/off bit, D4, contains a 1 to turn on (display) the graphics data in the installed planes. A 0 forces the palette to ignore the memory plane data and display the color contained at palette address 08H (Processor I/O address 0190H).

The graphics/alpha bit, D5, determines which data is used as palette addresses. If this bit is a 1, the Hi-Res memory planes are used. If this bit is a 0, the 9007 video data is used (this displays text on the CM-1 color monitor).

9.3.5 Displaying Alpha-Numeric Text

The Hi-Res board contains circuitry to switch between the internal memory planes or external data for use as palette addresses. In the Model 2000, the external data is hard-wired on the bus as the 9007 video and the video attribute bit INTENSITY. If the external mode is selected (referred to as the ALPHA MODE), the video data is palette address bit A0 and the attribute bit for intensity is palette address bit A1. Palette address bits A2 and A3 are tied high (a 1). This allows 4-color text to be displayed on the CM-1 color monitor.

For this to work properly, the 9007 must be in 640 X 400 display mode, NOT in 800 X 400 mode. Text from the 9007 and graphics data from the Hi-Res board CANNOT be displayed at the same time on the CM-1 monitor.

9.3.6 Displaying Monochrome Graphics on VM-1 B/W Monitor

You have the option of using either a monochrome monitor (the VM-1), a Hi-Res board and a color monitor (the CM-1) or both. This implies four possible combinations for having text (generated by the main unit's 9007) and graphics (generated by the Hi-Res option) displayed at the same time. These are summarized below:

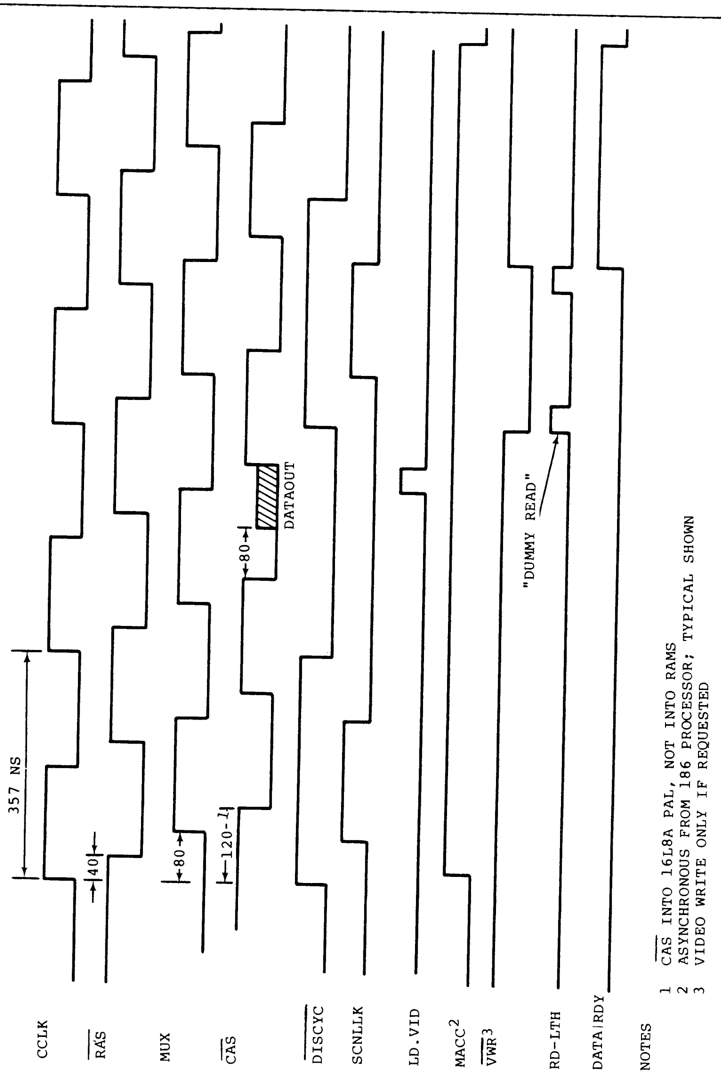
VM-1	CM-1
TEXT	TEXT
TEXT	GRAPHICS
(X) GRAPHICS	TEXT
GRAPHICS	GRAPHICS

Of the four possible modes, ONLY THREE ARE ALLOWED. Graphics on the VM-1 and Text on the CM-1 is NOT allowed. The way that a particular mode is selected is by two I/0 ports, one on the Hi-Res board and one in the Model 2000 main unit. The plane select register on the Hi-Res board selects between text and graphics displayed on the CM-1. This bit is sent to the main pc board and used with the VIDEO SELECT BIT located at I/0 address 0081H in Rev 1 pc boards and port 0101H in later releases. If D15 of this port is a 1, the 9007 video goes to the VM-1 monitor. If the bit is a 0, then the graphics data from PLANE 0 goes to the VM-1. In this manner, monochrome graphics can be displayed on the VM-1 from the Hi-Res board. If other planes are installed, the VM-1 ignores them and uses PLANE 0 ONLY.

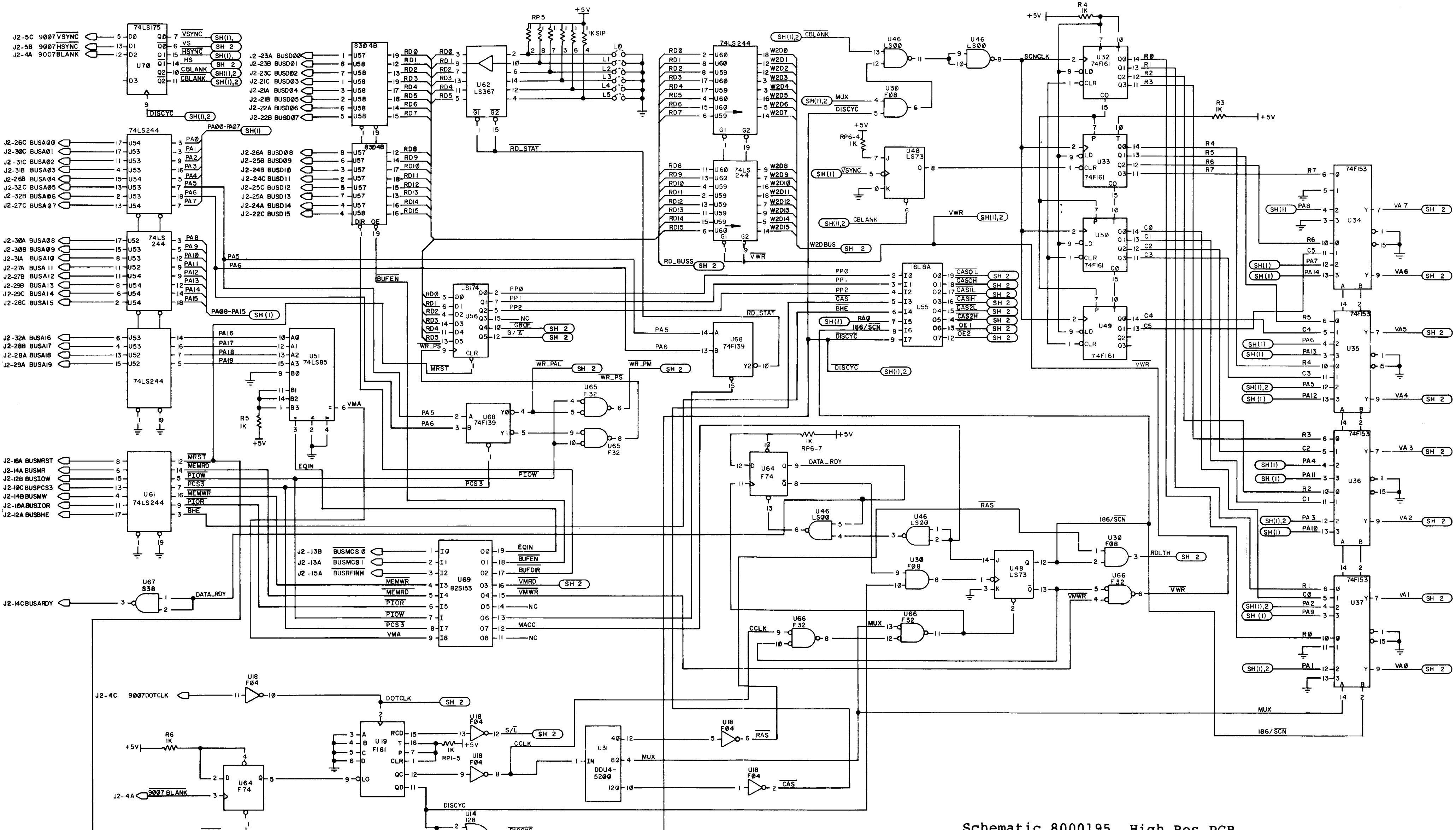
9.3.7 Status Port Description

The Hi-Res board contains a 6 bit status port, which is READ-ONLY. This port is used to determine the number of installed planes, pcb revision level, etc. It is located in the I/O map at address 0180H. The following description relates the bits in the port to their meaning.

BIT	MEANING
0	0 = Hi-Res board 1 = TV Board
1	0 = Plane 0 only 1 = 3 planes installed
2,3,4	pcb revision
5	future use

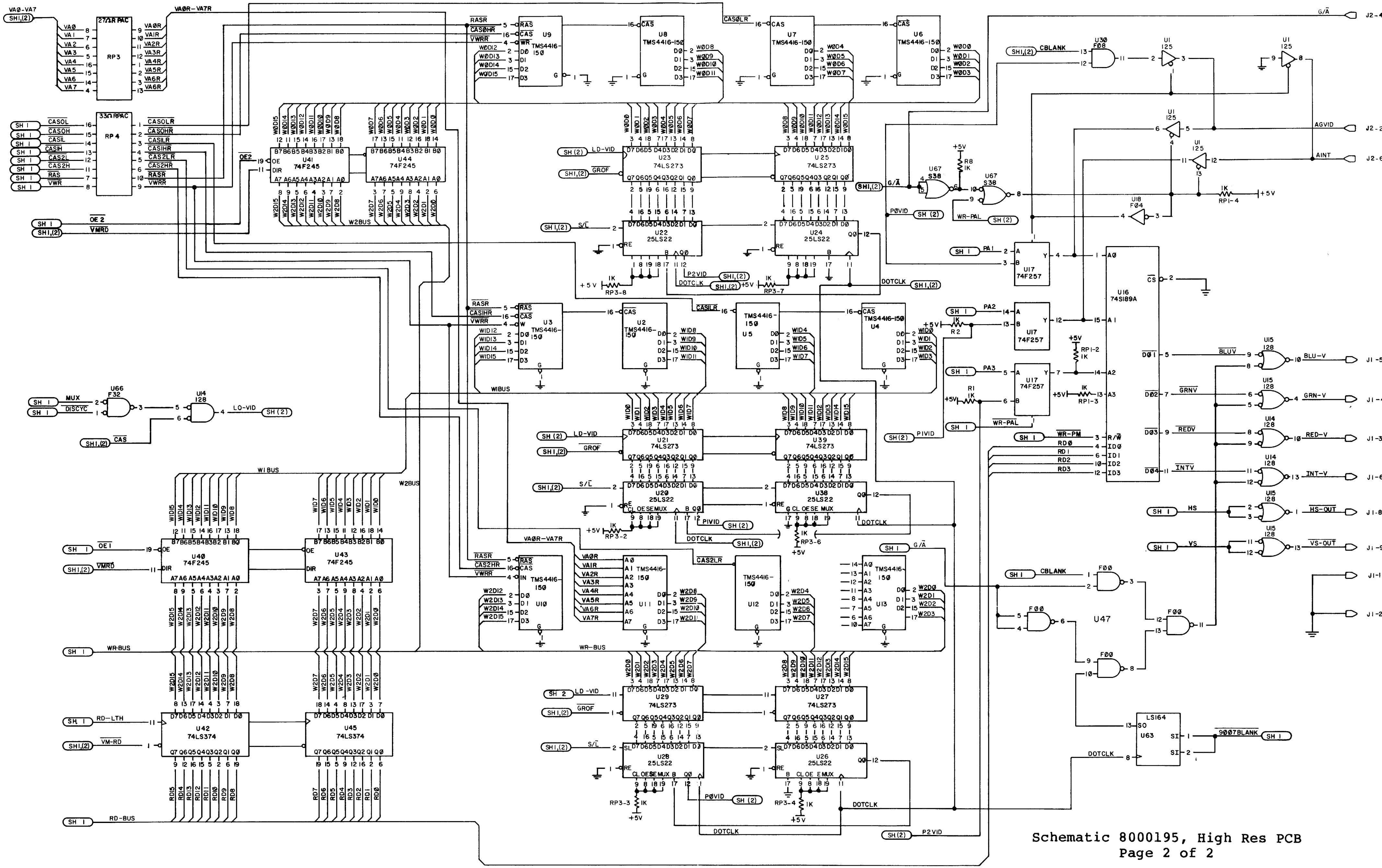


Timing Diagram, Hi Res PCB



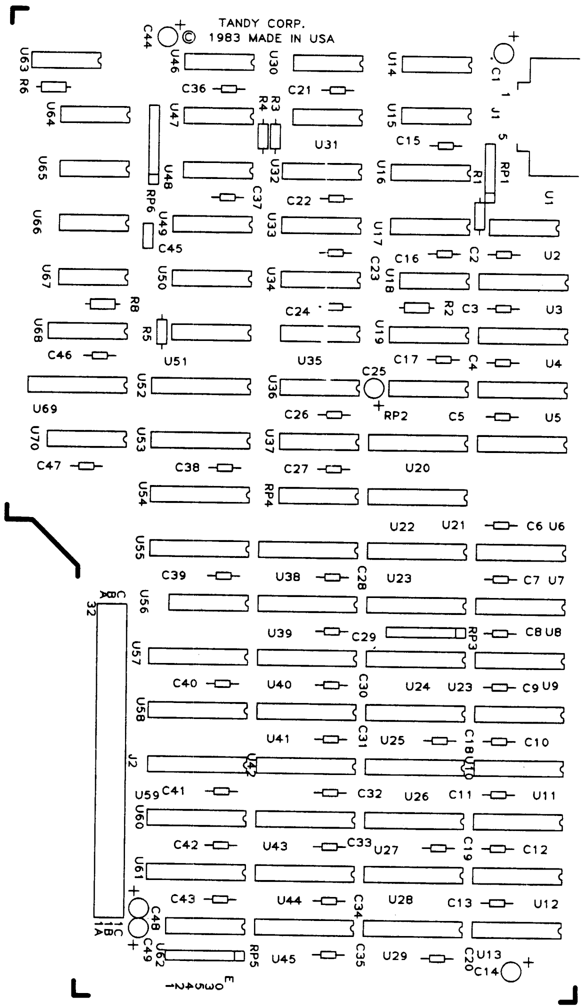
Schematic 8000195, High Res PCB
Page 1 of 2

Schematic 8000195, High Res PCB
Page 1 of 2

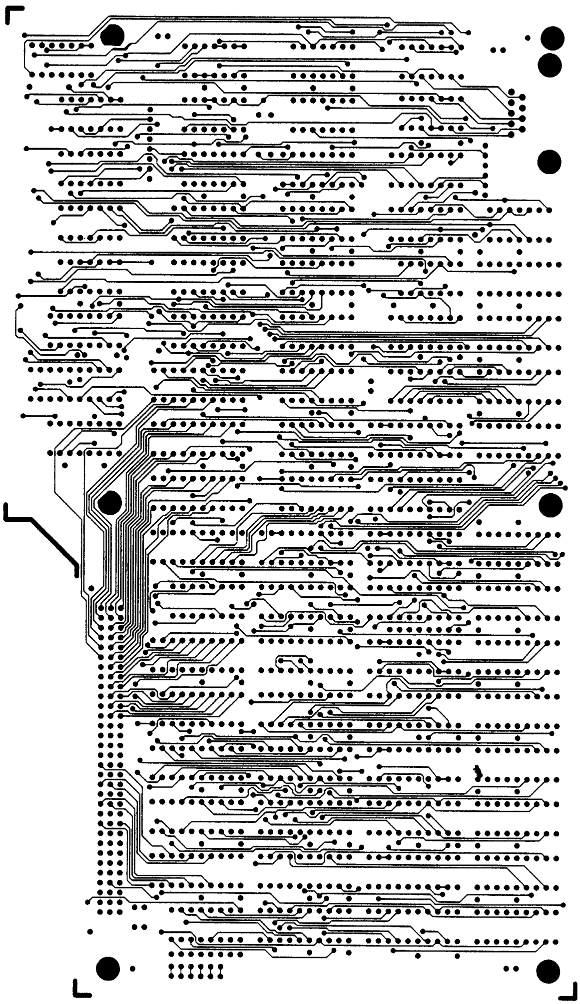


Schematic 8000195, High Res PCB
Page 2 of 2

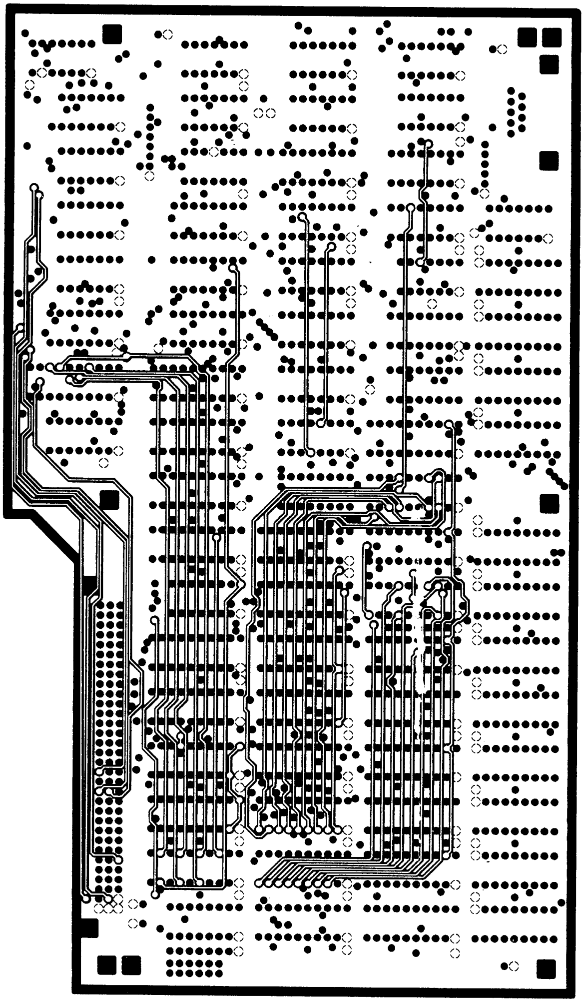
Schematic 8000195, High Res PCB
Page 2 of 2



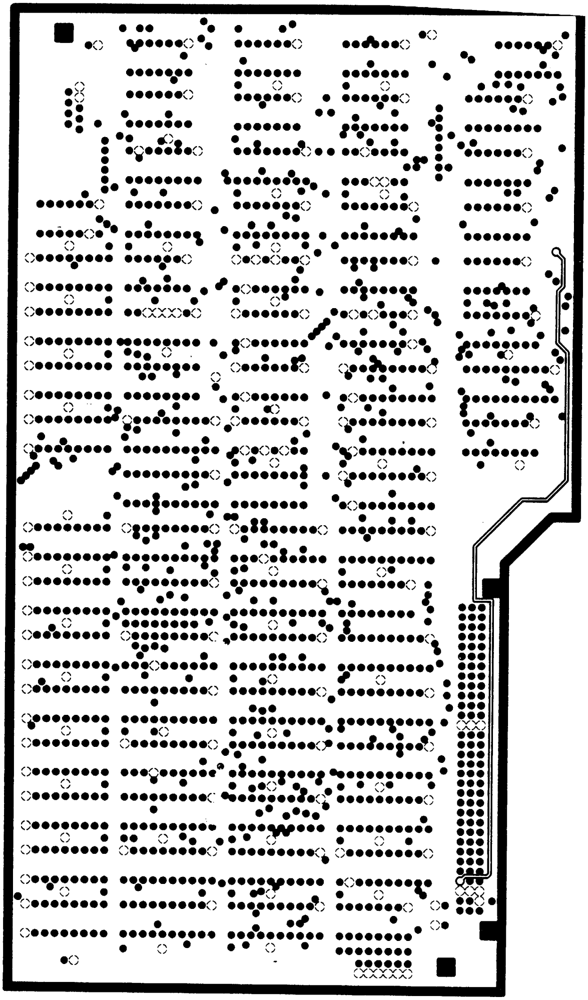
Component Location 1700261, Hi/Lo Res Graphics PCB



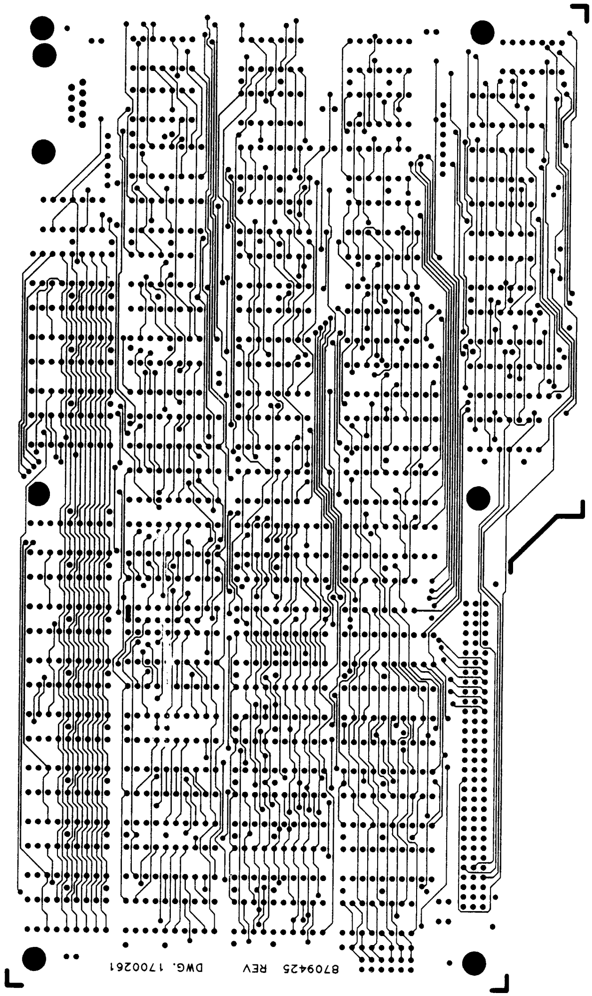
Circuit Trace 1700261, Hi/Lo Res Graphics PCB
Circuit Side



Circuit Trace 1700261, Hi/Lo Res Graphics PCB
+5 Volt Plane



Circuit Trace 1700261, Hi/Lo Res Graphics PCB
Ground Plane



Circuit Trace 1700261, Hi/Lo Res Graphics PCB
Solder Side

Parts List - PCB Assembly 889B010
26-5140 B & W Graphics Option

Item	Sym	Description	Part Number
1	1	Chassis, Graphics Board	8729258
2	2	Plunger, Nylatch	8590149
3	2	Grommet, Nylatch	8590148
4	1	PCB, Graphics Board	8709425
5	1	Connector, DB9 (J1)	8519183
6	1	Connector, 96 Pin (J2)	8519181
7	12	Socket, 18-Pin DIP (U2-U13)	8509006
8	11	Socket, 20-Pin DIP (U20,22,24, 38,40,41,43,44,55,69)	8509009
9	2	Screw, #2-56 x 3/8" PPH (J2)	8569201
10	2	Nut, #2 (J2)	8579042
11	6	Screw, #4-40 x 3/16" PPH MS	8569272
12	1	Label, PCB Serial	8789140
	C1	Capacitor, 22 mfd, 6.3V Elec Radial	8326221
	C2	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C3	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C4	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C5	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C6	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C7	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C8	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C9	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C10	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C11	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C12	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C13	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C14	Capacitor, 22 mfd, 6.3V Elec Radial	8326221
	C15	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C16	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C17	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C18	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C19	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C20	Capacitor, .1 mfd, 50V Mono Axial	8326221
	C21	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C22	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C23	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C24	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C25	Capacitor, 22 mfd, 6.3V Elec Radial	8326221
	C26	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C27	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C28	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C29	Capacitor, .1 mfd, 50V Mono Axial	8374104

Parts List - PCB Assembly 8898801
26-5140 B & W Graphics Option

Item	Sym	Description	Part Number
	C30	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C31	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C32	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C33	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C34	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C35	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C36	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C37	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C38	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C39	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C40	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C41	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C42	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C43	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C44	Capacitor, 22 mfd, 6.3V Elec Radial	8326221
	C45	Not Used	
	C46	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C47	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C48	Capacitor, 22 mfd, 6.3V Elec Radial	6326221
	C49	Capacitor, 22 mfd, 6.3V Elec Radial	6326221
	R1	Resistor, 4.7 kohm, 1/4W 5%	8207247
	R2	Resistor, 330 ohm, 1/4W 5%	8207133
	RP1	Resistor Pak, 1 kohm, SIP 6 Pin	8290210
	RP2	Resistor Pak, 27 ohm, DIP 16 Pin	8290027
	RP3	Resistor Pak, 1 kohm, SIP 10 Pin	
	RP4	Resistor Pak, 33 ohm, DIP 16 Pin	8290044
	RP5	Resistor Pak, 1 kohm, SIP 10 Pin	
	RP6	Resistor Pak, 1 kohm, SIP 10 Pin	
	U1	IC, 74LS125, Bus Buffer	8020125
	U2	Not Used	
	U3	Not Used	
	U4	Not Used	
	U5	Not Used	
	U6	IC, TMS4416-15 RAM	8040416
	U7	IC, TMS4416-15 RAM	8040416
	U8	IC, TMS4416-15 RAM	8040416
	U9	IC, TMS4416-15 RAM	8040416
	U10	Not Used	
	U11	Not Used	
	U12	Not Used	
	U13	Not Used	

Parts List - PCB Assembly 8898801
26-5140 B & W Graphics Option

Item	Sym	Description	Part Number
	U14	IC, 74128, 50 ohm Line Driver	8000128
	U15	IC, 74128, 50 ohm Line Driver	8000128
	U16	IC, 74S189, RAM	8010189
	U17	IC, 74F257, Multiplexer	8015257
	U18	IC, 74F04, Hex Inverter	8015004
	U19	IC, 74F161, Counter	8015161
	U20	Not Used	
	U21	IC, 74LS273, Octal Flip Flop	8020273
	U22	Not Used	
	U23	IC, 74LS273, Octal Flip Flop	8020273
	U24	Not Used	
	U25	IC, 74LS273, Octal Flip Flop	8020273
	U26	IC, 25LS22, 8-bit Shift Register	8020022
	U27	IC, 74LS273, Octal Flip Flop	8020273
	U28	IC, 25LS22, 8-Bit Shift Register	8020022
	U29	IC, 74LS273, Octal Flip Flop	8020273
	U30	IC, 74F08, Quad 2-Input NAND	8015008
	U31	IC, DDU4-5200 Delay Line, 200nsec	8429010
	U32	IC, 74F161, Counter	8015161
	U33	IC, 74F161, Counter	8015161
	U34	IC, 74F153, Multiplexer	8015153
	U35	IC, 74F153, Multiplexer	8015153
	U36	IC, 74F153, Multiplexer	8015153
	U37	IC, 74F153, Multiplexer	8015153
	U38	Not Used	
	U39	IC, 74LS273, Octal Flip Flop	8020273
	U40	Not Used	
	U41	Not Used	
	U42	IC, 74LS374, Flip Flop	8020374
	U43	Not Used	
	U44	Not Used	
	U45	IC, 74LS374, Flip Flop	8020374
	U46	IC, 74LS00, Quad 2-Input NAND	8020000
	U47	IC, 74F00, Quad 2-Input NAND	8015000
	U48	IC, 74LS73, Flip Flop	8020073
	U49	IC, 74F161, Counter	8015161
	U50	IC, 74F161, Counter	8015161
	U51	IC, 74LS85, Comparator	8020085
	U52	IC, 74LS244, Octal Buffer	8020244
	U53	IC, 74LS244, Octal Buffer	8020244
	U54	IC, 74LS244, Octal Buffer	8020244
	U55	IC, PAL16L8A, Mono	
	U56	IC, 74LS174, Hex Flip Flop	8020174

Parts List - PCB Assembly 8898801
26-5140 B & W Graphics Option

Item	Sym	Description	Part Number
	U57	IC, 8304B, Bus Transceiver	8060304
	U58	IC, 8304B, Bus Transceiver	8060304
	U59	IC, 74LS244, Octal Buffer	8020244
	U60	IC, 74LS244, Octal Buffer	8020244
	U61	IC, 74LS244, Octal Buffer	8020244
	U62	IC, 74LS367, Hex Driver	8020367
	U63	IC, 74LS164, Shift Register	8020164
	U64	IC, 74F74, Flip Flop	8015074
	U65	IC, 74F32, Quad 2-Input OR	8015032
	U66	IC, 74F32, Quad 2-Input OR	8015032
	U67	IC, 74S38, Quad 2-Input NAND	8010038
	U68	IC, 74F139, Decoder	8015139
	U69	IC, 82S153, IFL Decode	
	U70	IC, 74LS175, Flip Flop	8020175

Parts List

26-5141 Color Video Upgrade

Item	Sym	Description	Part Number
Note: This kit requires the 26-5140 B & W Graphics option (see Paragraph 9.4) in addition to the parts noted below.			
	U2	IC, RAM TMS4416-15	8040416
	U3	IC, RAM TMS4416-15	8040416
	U4	IC, RAM TMS4416-15	8040416
	U5	IC, RAM TMS4416-15	8040416
	U10	IC, RAM TMS4416-15	8040416
	U11	IC, RAM TMS4416-15	8040416
	U12	IC, RAM TMS4416-15	8040416
	U13	IC, RAM TMS4416-15	8040416
	U20	IC, 25LS22, 8-bit Shift Register	8020022
	U22	IC, 25LS22, 8-bit Shift Register	8020022
	U24	IC, 25LS22, 8-bit Shift Register	8020022
	U38	IC, 25LS22, 8-bit Shift Register	8020022
	U40	IC, 74F245, Octal Buffer	8015245
	U41	IC, 74F245, Octal Buffer	8015245
	U43	IC, 74F245, Octal Buffer	8015245
	U44	IC, 74F245, Octal Buffer	8015245
	U55	IC, PAL16L8A Color	

APPENDICES

The following sections contain reprints of manufacturer's documentation of components used in the Model 2000 Computer.

Tandy Corporation gratefully acknowledges permission by the following to reprint their copyrighted material in this manual.

Mitsubishi Electric Corporation
2-3 Marunouchi 2-Chome
Chiyoda-Ku, Tokyo 100, Japan

Tandon Corporation
20320 Prarie Street
Chatsworth, California 91311

Intel Corporation
3065 Bowers Avenue
Santa Clara, California 95051

Standard Microsystems Corporation
35 Marcus Blvd.
Hauppauge, New York 11787

MODEL 2ØØØ PORT SPECIFICATIONS

DEVICE	ADDRESS	ACCESS	BIT(S)	FUNCTION
LS273	ØØØØ	WR	DØ	KEYBOARD POWER (1=ON)
			D1	EXTERNAL CLOCK ENABLE
			D2	SPEAKER GATE
			D3	SPEAKER DATA
			D4	REFRESH CLOCK GATE (1=ON)
			D5	FDC RESET (Ø=RESET)
			D6	186 TIMER Ø ENABLE (1=ON)
			D7	186 TIMER 1 ENABLE (1=ON)
LS273	ØØØØ	RD	DØ	RS-232 RING INDICATE (Ø=TRUE)
			D1	RS-232 CARRIER DETECT (Ø=TRUE)
			D2-D6	UNDEFINED
			D7	ACLOW (Ø = LOW AC LINE)
LS139	ØØØ2	WR		DMA CONTROL PORT
			DØ	REQUEST Ø ENABLE (1 = ENABLE)
			D1	REQUEST 1 ENABLE (1 = ENABLE)
			D2	REQUEST 2 ENABLE (1 = ENABLE)
			D3	REQUEST 3 ENABLE (1 = ENABLE)
			CHANNEL SELECTS ROUTE DMA REQUESTS TO EITHER CHANNEL Ø OR CHANNEL 1 DRQ'S, A Ø SELECTS DRQØ, A 1 SELECTS DRQ1.	
			D4	REQUEST Ø SELECT
			D5	REQUEST 1 SELECT
			D6	REQUEST 2 SELECT
			D7	REQUEST 3 SELECT
8251	ØØ1Ø	RD/WR	DØ-D7	BIDIRECTIONAL DATA BUS TO/FROM 8251 DATA REGISTER
8251	ØØ12	RD/WR	DØ-D7	WRITE CONTROL WORD READ 8251 STATUS
LS138	ØØ2F	RD/WR	XX**	FDC TERMINATE TRANSFER STROBE
8272	ØØ3Ø	RD/WR	DØ-D7	READ - READ MAIN STATUS FDC WRITE - ILLEGAL
8272	ØØ32	RD/WR	DØ-D7	READ - READ DATA REGISTER WRITE - WRITE DATA REGISTER
8253	ØØ4Ø	RD/WR	DØ-D7	WRITE - LOAD COUNTER Ø READ - READ COUNTER Ø
8253	ØØ42	RD/WR	DØ-D7	WRITE - LOAD COUNTER 1 READ - READ COUNTER 1
8253	ØØ44	RD/WR	DØ-D7	WRITE - LOAD COUNTER 2 READ - READ COUNTER 2
8253	ØØ46	RD/WR	DØ-D7	WRITE - LOAD MODE WORD

MODEL 2ØØØ PORT SPECIFICATIONS

DEVICE	ADDRESS	ACCESS	BIT(S)	FUNCTION
				READ - ILLEGAL OPERATION
8255A-5	ØØ5Ø	RD/WR	DØ-D7	BIDIRECTIONAL DATA BUS
8255A-5	ØØ52*	RD	DØ-D7	INPUT KEYBOARD DATA
8255A-5	ØØ52*	RD	DØ-D2	UNDEFINED BITS
			D3	PRINTER ACK*
			D4	PRINTER FAULT*
			D5	SELECT
			D6	PAPER EMPTY
			D7	BUSY
LS244	ØØ52*	RD	DØ-D7	AUX.STATUS BITS
8255A-5	ØØ54	WR	DØ	DIRECTION FOR PORT ØØ5Ø
		WR	D1-D2	SELECTS DEVICE INPUT FOR PORT ØØ52 D1 D2 SOURCE Ø Ø PRINTER STATUS Ø 1 READ KBOARD DATA 1 Ø AUX.STATUS PORT 1 1 UNDEFINED
			D3	INTRQ FOR LPRINT13
			D4	STROBE INPUT (AUX INPUT)
			D5	INPUT BUFFER FULL (AUX)
			D6	PRINTER ACKNOWLEDGE
			D7	STROBE TO PRINTER
8259A-2	ØØ6Ø	WR	DØ-D7	WRITE COMMAND WORDS
	ØØ62	RD	DØ-D7	READ STATUS
8259A-2	ØØ7Ø	WR	DØ-D7	WRITE COMMAND WORDS
	ØØ72	RD	DØ-D7	READ STATUS
LS139	ØØ8Ø	RD/WR	DØ-D7	GENERATE DMACKØ
LS139	ØØAØ	RD/WR	DØ-D7	GENERATE DMACK1
LS139	ØØCØ	RD/WR	DØ-D7	GENERATE DMACK2
LS139	ØØEØ	RD/WR	DØ-D7	GENERATE DMACK3

* FOR DETERMINATION OF DEVICE ENABLED AT PORT ØØ52 REFER TO SETTING OF BITS D1 AND D2 OF PORT ØØ54.
** XX = DON'T CARE

DEVICE	ADDRESS	ACCESS	BIT(S)	FUNCTION
9ØØ7	Ø1ØØ	RD	DØ-D7	9ØØ7 RØØ
LS374	Ø1Ø1	WR		ADDRESS CONTROL REGISTER
			D8	A15 OF VIDEO ACCESS
			D9	A16 OF VIDEO ACCESS
			D1Ø	A17 OF VIDEO ACCESS
			D11	A18 OF VIDEO ACCESS
			D12	A19 OF VIDEO ACCESS
			D13	CLOCK SPEED Ø = 22.4 MHZ 1 = 28 MHZ
			D14	DOTS/CHAR Ø = 1Ø (8ØØX4ØØ) 1 = 8 (64ØX4ØØ)
			D15	VIDOUT-SEL, SELECTS THE VIDEO SOURCE FOR DISPLAY ON MONOCHROME MONITOR.

MODEL 2ØØØ PORT SPECIFICATIONS

DEVICE	ADDRESS	ACCESS	BIT(S)	FUNCTION
				1 = 9ØØ7, Ø = BUS
9ØØ7	Ø1ØØ	WR	DØ-D7	9ØØ7 RØØ
LS374	Ø1Ø1	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø1Ø2	WR	DØ-D7	9ØØ7 RØ1
LS374	Ø1Ø3	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø1Ø4	WR	DØ-D7	9ØØ7 RØ2
LS374	Ø1Ø5	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø1Ø6	WR	DØ-D7	9ØØ7 RØ3
LS374	Ø1Ø7	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø1Ø8	WR	DØ-D7	9ØØ7 RØ4
LS374	Ø1Ø9	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø1ØA	WR	DØ-D7	9ØØ7 RØ5
LS374	Ø1ØB	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø1ØC	WR	DØ-D7	9ØØ7 RØ6
LS374	Ø1ØD	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø1ØE	WR	DØ-D7	9ØØ7 RØ7
LS374	Ø1ØF	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø11Ø	WR	DØ-D7	9ØØ7 RØ8
LS374	Ø111	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø112	WR	DØ-D7	9ØØ7 RØ9
LS374	Ø113	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø114	WR	DØ-D7	9ØØ7 RØA
LS374	Ø115	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø116	WR	DØ-D7	9ØØ7 RØB
LS374	Ø117	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø118	WR	DØ-D7	9ØØ7 RØC
LS374	Ø119	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø11A	WR	DØ-D7	9ØØ7 RØD
LS374	Ø11B	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø11C	WR	DØ-D7	9ØØ7 RØE
LS374	Ø11D	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø11E	WR	DØ-D7	9ØØ7 RØF
LS374	Ø11F	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø12Ø	WR	DØ-D7	9ØØ7 R1Ø
LS374	Ø121	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø122	WR	DØ-D7	9ØØ7 R11
LS374	Ø123	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø124	WR	DØ-D7	9ØØ7 R12
LS374	Ø125	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø126	WR	DØ-D7	9ØØ7 R13
LS374	Ø127	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø128	WR	DØ-D7	9ØØ7 R14
LS374	Ø129	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø12A	RD/WR	DØ-D7	9ØØ7 R15
LS374	Ø12B	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø12C	RD/WR	DØ-D7	9ØØ7 R16
LS374	Ø12D	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø12E	WR	DØ-D7	9ØØ7 R17
LS374	Ø12F	WR	D8-D15	ADDRESS CONTROL REGISTER

MODEL 2ØØØ PORT SPECIFICATIONS

DEVICE	ADDRESS	ACCESS	BIT(S)	FUNCTION
9ØØ7	Ø13Ø	WR	DØ-D7	9ØØ7 R18
9ØØ7	Ø17Ø	RD	DØ-D7	9ØØ7 R38
LS374	Ø131	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø132	WR	DØ-D7	9ØØ7 R19
9ØØ7	Ø172	RD	DØ-D7	9ØØ7 R39
LS374	Ø133	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø134	WR	DØ-D7	9ØØ7 R1A
LS374	Ø135	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø174	RD	DØ-D7	9ØØ7 R3A
LS374	Ø175	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø176	RD	DØ-D7	9ØØ7 R3B
LS374	Ø177	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø178	RD	DØ-D7	9ØØ7 R3C
LS374	Ø179	WR	D8-D15	ADDRESS CONTROL REGISTER