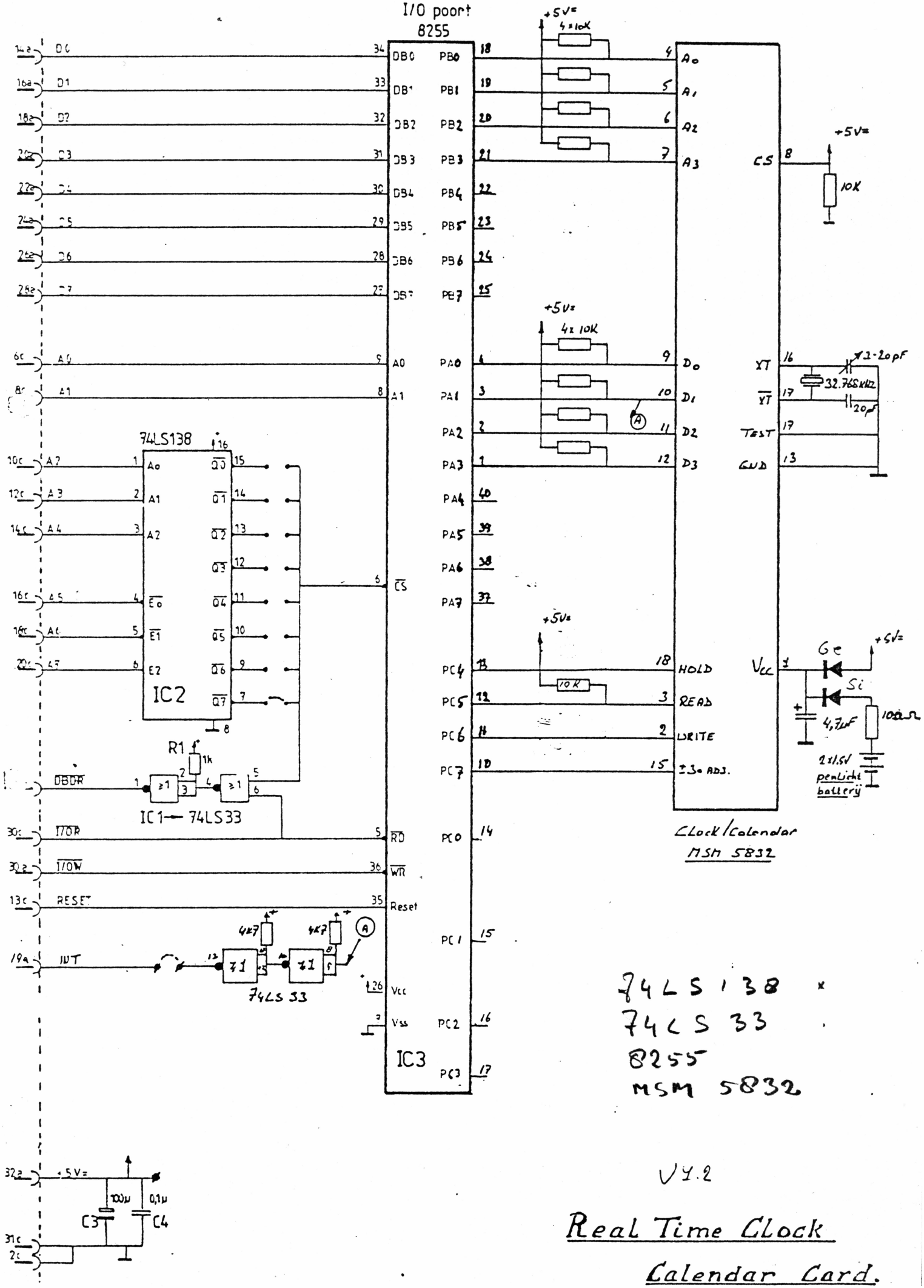


74LS138 x
74LS33
8255
MSM 5832

V4.2

Real Time Clock
Calendar Card.

Onderdelen lijst Real time Clock/Calendar

IC's

1 x 8255 I/O poort
1 x 74LS138
1 x 74LS 33
1 x MSM5832 clock

Kristal 32,768 KHz

2 x Diode Germanium
1 x " Silisium

Weerstanden 10 x 10 KΩ
2 x 4K7
1 x 1K

Condensator 1 x 10 µF
1 x 4,7 µF
2 x 0,1 µF
1 x 20 pF
2 x 3-20 pF

Batterij 2 x 1,5V = (penlight) + houder.

Pinstrook

Connector 64 polig a-c.

153

FUNCTION TABLE

FIGURE 1

ADDRESS INPUTS				INTERNAL COUNTER	DATA I/O				DATA LIMITS	NOTES
A_0	A_1	A_2	A_3		D_0	D_1	D_2	D_3		
0	0	0	0	S 1	*	*	*	*	0∿9	S1 or S10 are reset to zero irrrespective of input data D0∿D3 when write instruction is executed with address selection.
1	0	0	0	S 10	*	*	*		0∿5	
0	1	0	0	MI 1	*	*	*	*	0∿9	
1	1	0	0	MI 10	*	*	*		0∿5	
0	0	1	0	H 1	*	*	*	*	0∿9	
1	0	1	0	H 10	*	*	†	†	0∿1 / 0∿2	D2 = "1" for PM D3 = "1" for 24 hour format D2 = "0" for AM D3 = "0" for 12 hour format
0	1	1	0	W	*	*	*		0∿6	
1	1	1	0	D 1	*	*	*	*	0∿9	
0	0	0	1	D 10	*	*	†		0∿3	D2 = "1" for 29 days in month 2 D2 = "0" for 28 days in month 2 (2)
1	0	0	1	MO 1	*	*	*	*	0∿9	
0	1	0	1	MO 10	*				0∿1	
1	1	0	1	Y 1	*	*	*	*	0∿9	
0	0	1	1	Y 10	*	*	*	*	0∿9	

(1) * data valid as "0" or "1".

Blank does not exist (unrecognized during a write and held at "0" during a read)

† data bits used for AM/PM, 12/24 HOUR and leap year.

(2) If D2 previously set to "1", upon completion of month 2 day 29, D2 will be internally reset to "0".

FUNCTIONAL DESCRIPTION

A block diagram of the MSM5832 microprocessor real-time clock/calendar and a package connection diagram are shown on the first page. Figure 9 illustrates a method of interfacing between the clock/calendar circuit and a micro processor. Figures 9, 10 and 11 illustrate alternative standby power supply circuits. A function table listing relationships between address inputs, data input/output and internal counter selection is shown in Figure 1. Unless otherwise indicated, the following descriptions are based on the block diagram.

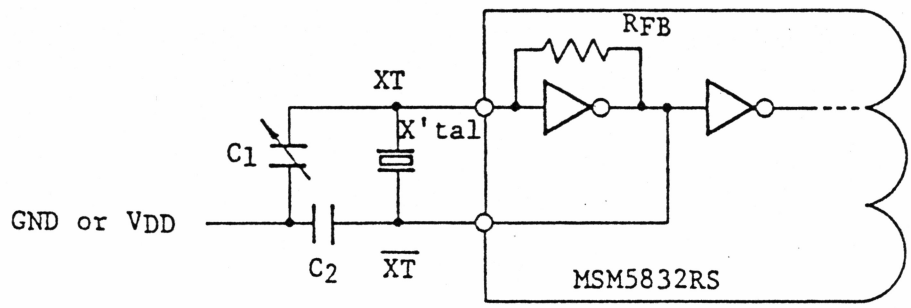
32.768kHz OSCILLATOR (pins 16 and 17): An internal inverting amplifier with feedback resistor, R_{FB}, is connected with a crystal and two capacitors as shown in Figure 6 to form a stable, accurate oscillator -- which serves as the precision time base of the circuit. Capacitors C1 and C2 in series provide the parallel load capacitance required for precise tuning of the quartz crystal. Typical oscillator performance as a function of ambient temperature and supply voltage is shown in Figures 2 and 3 respectively.

$A_0 \sim A_3$ (pins 4 ~ 7): Address inputs, used to select internal counters for read/write operations (see function table -- Figure 1). A "1" is defined as V_{CC}; a "0" is GND. Pull-down to GND is provided by internal resistors.

$D_0 \sim D_3$ (pins 9 ~ 12): Data Inputs/Outputs, two-way bus lines controlled by READ and WRITE inputs. As shown in Figure 7 external pull-up resistors of 4.7K or higher are required by the open-drain N-channel MOS outputs. D3 is the MSB; D_0 is the LSB.

TEST (pin 14): Normally this input is unconnected -- pull-down to GND is provided by an internal resistor -- or connected to GND. With CS at V_{CC}, pulses to V_{CC} on the TEST input will directly clock the S_1, MI_{10}, W, D_1 and Y_1 counters, depending on which counter is addressed (W and D_1 are select-d by D_1 address in this mode only). Roll-over to next counter is enabled in this mode.

OSCILLATOR CIRCUIT FIGURE 6



$C_1 \sim C_2 = 15 \sim 30pF$

CHIP SELECT (pin 8): Connecting CS input to V_{CC} enables all inputs and outputs. Unconnected -- pull-down to GND is provided by an internal resistor -- or connecting CS to GND will disable HOLD, WRITE, READ, ±30 ADJ, $D_0 \sim D_3$, $A_0 \sim D_3$ and TEST.

As shown in Figure 9 CS can be used to detect system power failure by connecting system power (+5V) to CS, so that when system power is on, all inputs and outputs will be enabled, and when system power is off, all inputs and outputs will be disabled. The threshold voltage of CS is higher than all other inputs to insure correct operation of this function.

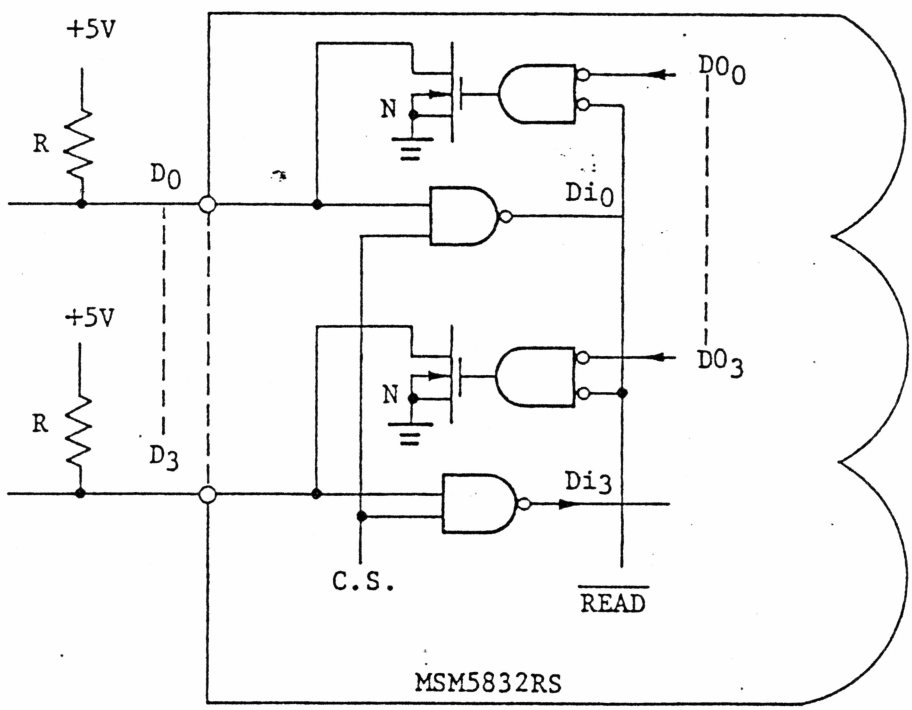
HOLD (pin 18): Switching this input to V_{CC} inhibits the internal 1Hz clock to the S1 counter. After the specified HOLD set-up time (150 µS), all counters will be in a static state, thus allowing error-free read or write operations. So long as the HOLD pulse width is less than 1 second, accuracy of the real time will be undisturbed. Pull-down to GND is provided by an internal resistor.

READ (pin 3): Read function as shown in Figure 4 is enabled when READ is switched to VCC. Pull-down to GND is provided by an internal resistor.

WRITE (pin 2): Write function as shown in Figure 5 is enabled when WRITE is switched to V_{CC}. Pull-down to GND is provided by an internal resistor.

±30 ADJ (pin 15): Momentarily connecting this input to V_{CC} (>31.25 ms) will reset seconds (S1, S10 counters and $2^{11} \sim 2^{15}$ frequency dividers) to 00; if seconds were 30 or more, one minute is added to the minutes (MI 1 counter) and if seconds were less than 30, the minutes are unchanged. Pull-down to GND is provided by an internal resistor.

DATA I/O CIRCUIT FIGURE 7



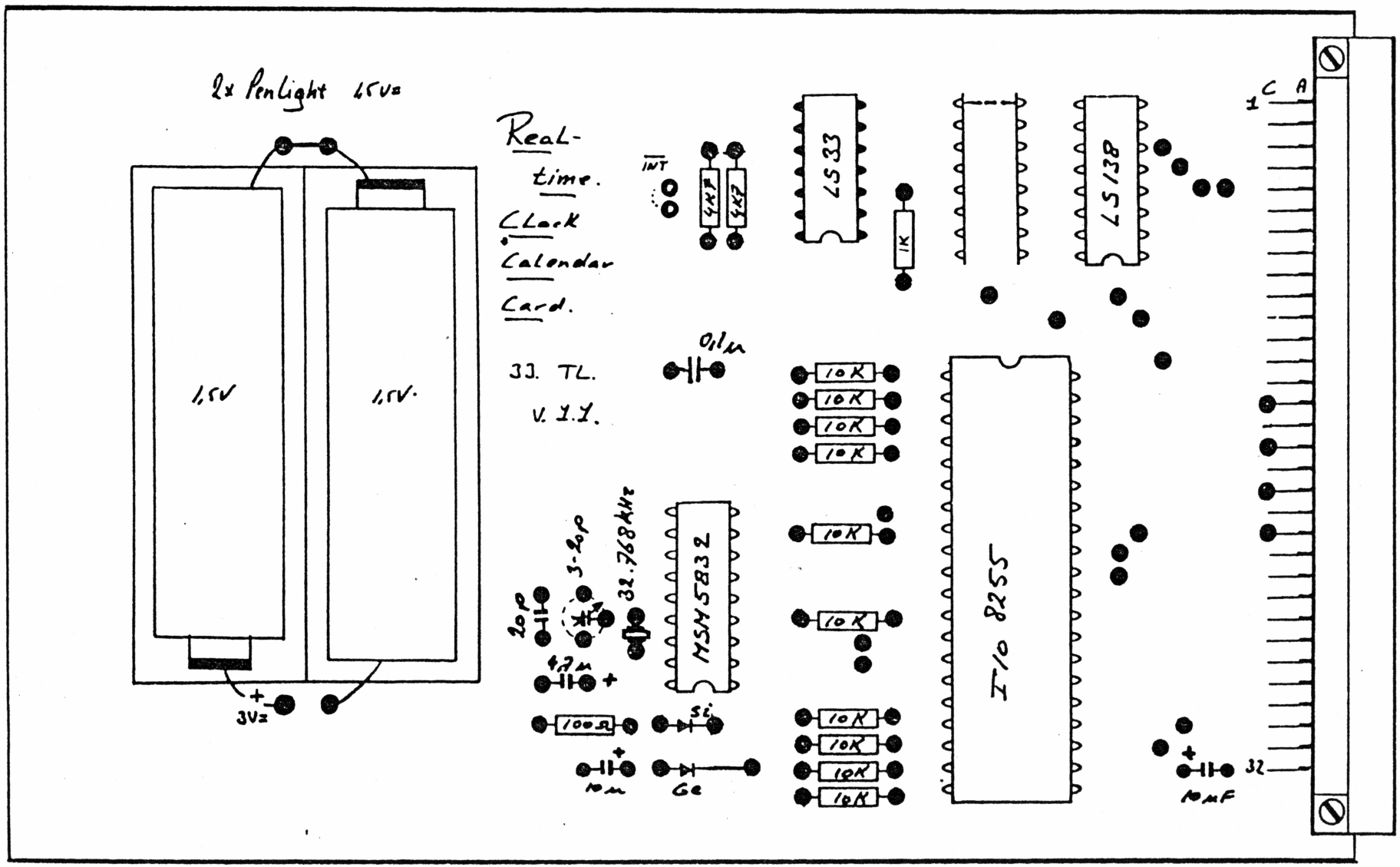
REFERENCE SIGNAL OUTPUT

Reference signals are available as outputs on $D_0 \sim D_3$ if CS, READ and $A_0 \sim A_3$ are at V_{CC}. Refer to Figure 8 for specifics. As shown in Figure 9 these signals may be used to generate interrupts for the microprocessor.

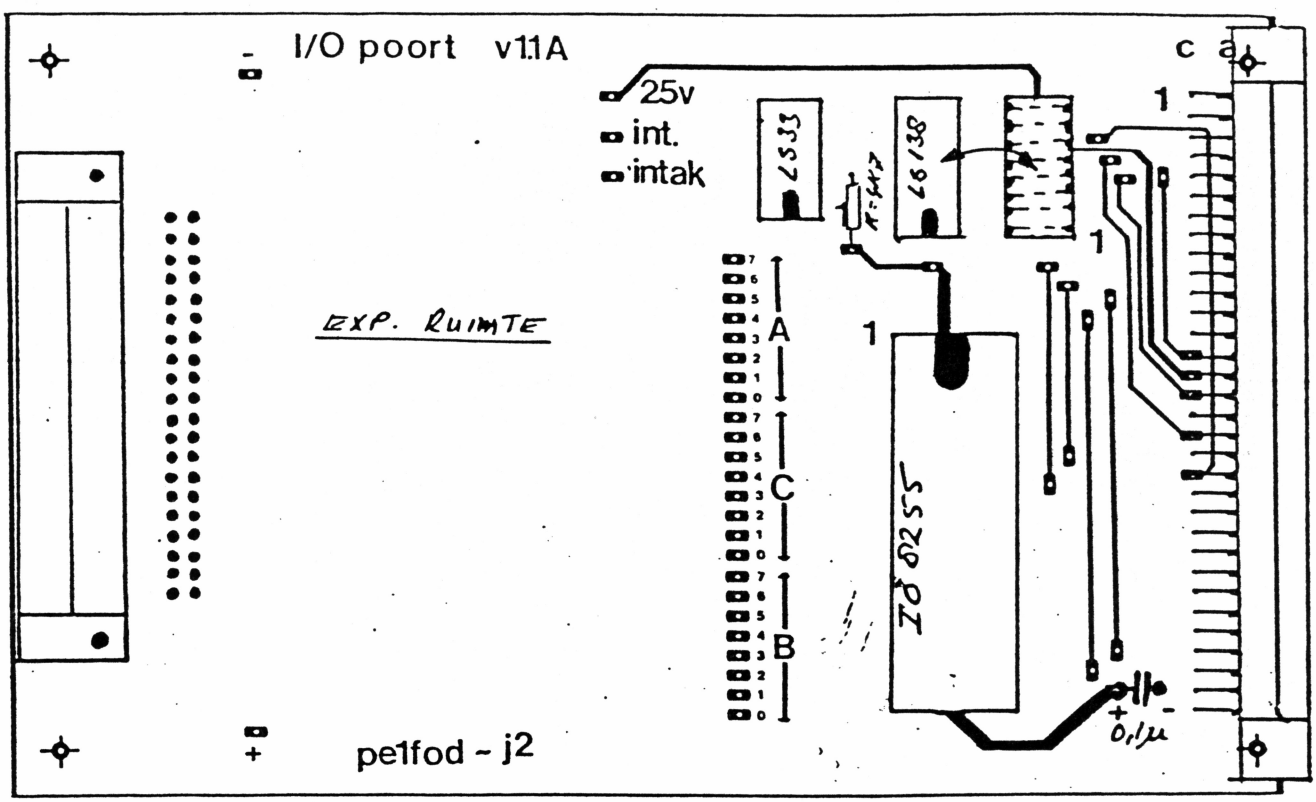
REFERENCE SIGNAL OUTPUTS FIGURE 8

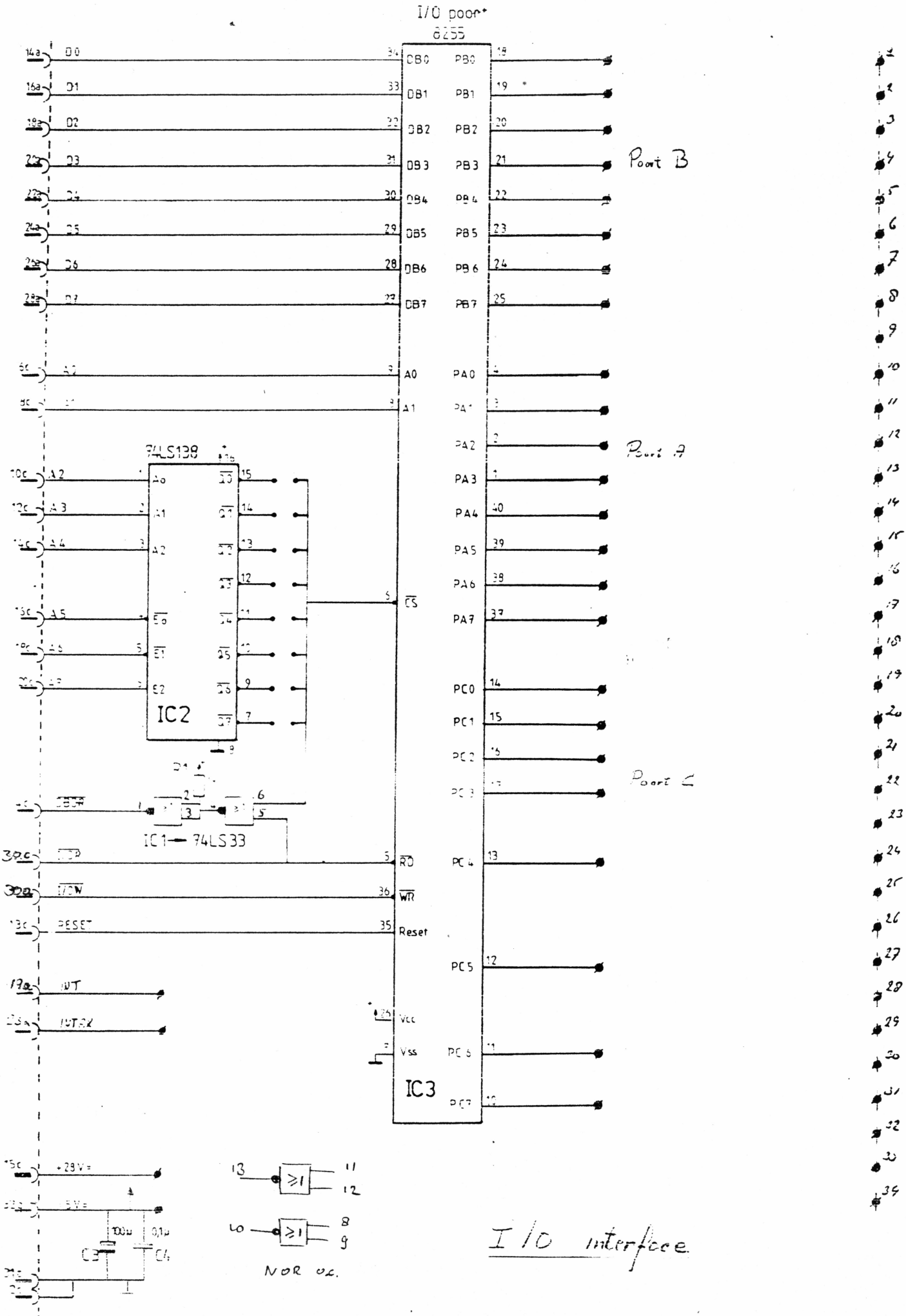
CONDITIONS	OUTPUT	REFERENCE FREQUENCY	PULSE WIDTH
HOLD = L	D_0(1)	1024 Hz	duty 50%
READ = H	D_1	1 Hz	122.1 µS
C.S. = H	D2	1/60 Hz	122.1 µS
$A_0 \sim A_3$ = H	D_3	1/3600 Hz	122.1 µS

(1) 1024 Hz signal at D_0 not dependent on HOLD input level


2x Penlight 1,5V=
1,5V
1,5V.
3V=
Real-
time.
Clock
Calendar
Card.
33. TL.
V. Y. Y.
INT
4K7
4K7
LS33
1K
LS138
0,1µ
10K
10K
10K
10K
10K
10K
10K
10K
10K
I/O 8255
MSM5832
10p
3-40p
32.768kHz
4,7µ
100Ω
Si
Ge
10µ
10µF
1
C
A
32

Opstelling.


I/O poort v1.1A
25v
int.
intak
EXP. RUIMTE
A
C
B
pe1fod - j2


I/O poort
8255
D0
D1
D2
D3
D4
D5
D6
D7
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
Poort B
A0
A1
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
Poort A
74LS138
A2
A3
A4
A5
A6
A7
IC2
CS
PC0
PC1
PC2
PC3
Poort C
IC1 — 74LS33
RD
WR
Reset
PC4
PC5
PC6
PC7
Vcc
Vss
IC3
INT
INTRX
+28V=
5V=
100µ
0,1µ
C3
C4
NOR o.c.
I/O interface