APPLICATION NOTE

HOW TO CONVERT A TMS7742 BASED APPLICATION TO TAKE ADVANTAGE OF THE NEW TMS77C82 CMOS MICROCONTROLLER WITH ON-CHIP EPROM

I - INTRODUCTION

The TEXAS INSTRUMENTS TMS7000 microcontroller family contains numerous members designed to support a wide range of applications that require more and more performance for a lower and lower cost. The TMS77C82 is hardware & software compatible with the TMS7742 but provides the required additional performance whilst reducing "glue logic" and consuming much less power that the TMS7742.

This report brings the first support to the designers for advantageously converting a TMS7742 NMOS EPROM on-chip microcontroller design into a TMS77C82 CMOS EPROM on-chip MCU one.
It gives a detailled comparison between the two microcontrollers focusing on key features, peripheral memory map, pinning, reset, programmation and emulation. It is earnestly recommended that designers refer to the TMS77C82 data sheet and the TMS7000 data manual edited by TEXAS INSTRUMENTS technical library group.

For any further information related to the TMS77C82 call the nearest TEXAS INSTRUMENTS sales office or regional technology center.

II - KEY FEATURES

The major differences between both circuits are as follows :

	TMS77C82	TMS7742
TECHNOLOGY	CMOS	NMOS
MEMORY	8K-BYTE EPROM	4K-BYTE EPROM
EQUIVALENT EPROM	TMS27C64	TMS2732A
MEMORY EXPANSION	64K BYTES	64K BYTES
I/O	CMOS COMPATIBLE 24 BIDIRECTIONAL PINS	TTL COMPATIBLE I/O PINS 22 BIDIRECTIONAL PINS +2 INPUT PINS
SERIAL CLOCK	SCLK ON PIN A4 (10)	SCLK ON PIN A6(15)
TIMERS ON CHIP	TWO 16 BITS WITH 5 BITS PRESCALE ONE 8 BITS WITH 2 BITS PRESCALE CAPTURE LATCH, CASCADABLE	TWO 8 BITS WITH 5 BITS PRESCALE ONE 8 BITS WITH 2 BITS PRESCALE CAPTURE LATCH
INTERRUPTS	EXTERNAL INTERRUPT PRGM FOR EDGE OR EDGE/LEVEL TRIGGERING . FOR RISING AND FALLING EDGE DETECTION BY SOFTWARE.	PRIORITIZED BY SOFTWARE. EDGE OR EDGE/LEVEL TRIGGERING AT MASKING .
VCC	3V TO 6V	4.5V TO 5.5V
FREQUENCY OSC.	0.5 MHz TO 8 MHz	1 TO 5 MHz
CLOCK OPTION	XTAL	XTAL
PACKAGE	40 PIN	40 PIN (same mechanical data)

Because the TMS77C82 includes twice the EPROM capacity of the TMS7742 and it is a CMOS processed chip, the TMS77C82 drastically reduces cost of design

III - PERIPHERAL MEMORY MAP

	77C82 (70CX2)	7742 (70X2)	70CX0
IOCNT0	P0	P0 >0100	P0
IOCNT2	P1> 0101	-	-
T1(LS) DAT	P13> 010D	P2 >0102	P2
T1CTL(0)	P15> 010F	P3 >0103	P3
APORT	P4	P4 >0104	P4
ADDR	P5	P5 >0105	-
BPORT	P6	P6 >0106	P6
RESERVED	P7	P7 >0107	P7
CPORT	P8	P8 >0108	P8
CDDR	P9	P9 >0109	P9
DPORT	P10	P10 >010A	P10
DDDR	P11	P11 >010B	P11
T1MSDATA	P12> 010C	-	-
IOCNT1	P2> 0102	P16 >0110	-
RESERVED	P3> 0103	P1 >0101	P1
T1CTL1	P14> 010E	-	-
T2MSDATA	P16> 0110	-	-
T2LSDATA	P17> 0111	P18 >0112	-
T2CTL0	P19	P19 >0113	-
SMODE	P20> 0114	P17 >0111	-
SCTL0	P21> 0115	P17	-
SSTAT	P22> 0116	P17	-
T3DATA	P23> 0117	P20 >0114	-
SCTL1	P24> 0118	P21 >0115	-
RXBUF	P25> 0119	P22 >0116	-
TXBUF	P26> 011A	P23 >0117	-
RESERVED	P27- P35	-	-
NOT AVAILA (in single or PERIPH.	P36 - P255	P12 - P15 P24 - P255	P12-P255

IV - PINNING EQUIVALENCE

When using the serial clock pin (SCLK), a modification of the application hardware is mandatory.

SCLK is on pin #10 (A4) when using the TMS77C82.
#15 (A6) TMS7742

Otherwise the two microcontrollers have exactly the same pin-out configuration.

V - INPUT/OUTPUT LEVELS

77C82 input/output's are CMOS compatible, whereas on 7742 they are TTL compatible.
Output current capabilities are shown in the following table :
(For VCC=5V)

	TMS77C82	TMS7742
VOH min/IOH	3.9 V/-0.7 mA	2.4 V/-400 uA
VOL max/IOL	1.1 V/2.5 mA	0.4 V/3.2 mA

VI - INITIALIZATION (reset functions)

4.1) SERIAL PORT

Should be programmed in the same manner than 7742 's, with the differences in the port register addresses.

SMODE	is	P20	(P17 for the TMS7742)
SCTL0	is	P21	(P17)
TIMER 3	at	P23	(P20)
SCTL1	is	P24	(P21)

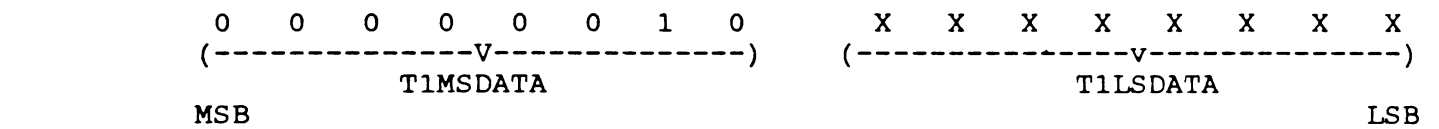
The serial port can be reset in three ways : hardware reset (via the RESET pin) or software reset (via the UR bit in SCTL0), or by writing to the SMODE register.

4.2) TIMERS

Only differences between the two devices are shown here.
Register for which there is no difference is T2CTL0 (P19).

Two 16 bit timers w/ 5 bit prescale	Two 8 bit timers w/5 bit prescale
internal clock source : Fosc /4	internal clock source : Fosc/16
T1LSDATA register is P13> 010D	T1DATA register is P2> 0102
T1CTL0 register is P15> 010F	T1CTL register is P3> 0103
T2LSDATA register is P17	T2DATA register is P18

Therefore each 16 bit timer data should be programmed as :

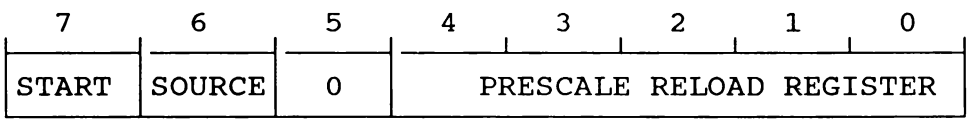


to obtain same internal clock and 8 bit timer as in 7742, if using internal clock source.

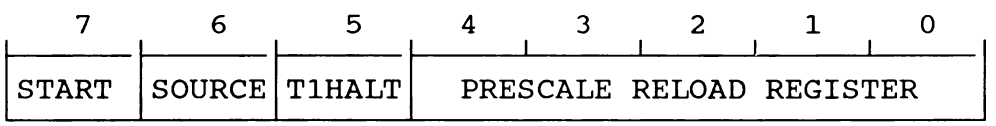
If external clock source is used then the 8 MSbits should be set at "0".

During write mode :

T1CTL / 7742

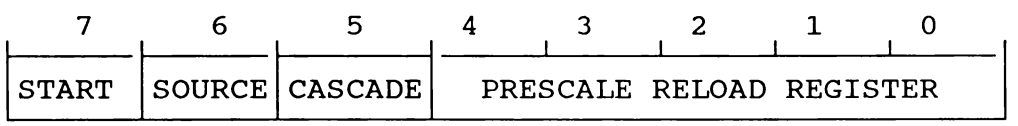


T1CTL0 / 77C82



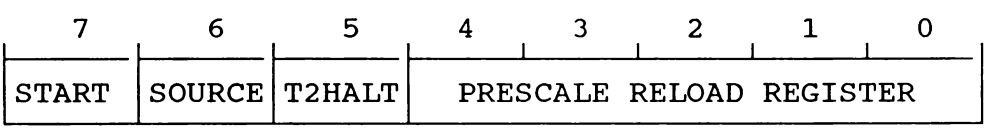
0-TIMER 1 REMAINS ACTIVE DURING IDLE
1-TIMER 1 WILL HALT DURING IDLE

T2CTL / 7742



0- SOURCE BIT DETERMINE CLOCK SOURCE
1- CLOCK SOURCE IS TIMER 1
RELOAD SIGNAL; OVERRIDES SOURCE BIT

T2CTL0 / 77C82



0-TIMER 2 REMAINS ACTIVE DURING IDLE
1-TIMER 2 WILL HALT DURING IDLE

T2CTL1 / 77C82

7							
CASCADE	T2OUT	X	X	X	X	X	X

0-DATA REGISTER BIT B1
1-TIMER2-OUT TOGGLES B1 WHEN T1 DECREMENTS THROUGH 0

0-SOURCE BIT DETERMINES CLOCK SOURCE
1-CLOCK SOURCE IS TIMER1 RELOAD SIGNAL;OVERRIDES SOURCE BIT

If the cascade bit in timer 2 of the 7742 is set to 1, then the cascadet bit of T2CTL1 should also be set to 1.

T1HALT bit of T1CTL0 in the 77C82 should always be set to 0.
T2HALT bit of T2CTL0 in the 77C82 should always be set to 0.
T2OUT bit of T2CTL1 in the 77C82 should always be set to 0.

4.3) INTERRUPT CONFIGURATION

Some 77C82 interrupts are programmable by software, and thus need to be positionned initially :

T2CTL0 / 77C82

7	6	5	4	3	2	1	0
0	0	INT3 EDGE	INT3 POL.	0	0	INT1 EDGE	INT1 POL.

0- ACTIVE LOW/FALLING EDGE
1- ACTIVE HIGH/RISING EDGE

0- EDGE & LEVEL SENSITIVE
1- EDGE SENSITIVE ONLY

0- ACTIVE LOW/FALLING EDGE
1- ACTIVE HIGH/RISING EDGE

0- EDGE & LEVEL SENSITIVE
1- EDGE SENSITIVE ONLY

Therefore, depending on customer application : edge (7742), or edge/level (EPP002), bits 5 and 1 shall be initialized at 1 or 0. Bits 0 and 4 shall be initialized at 0.

VII - HOW TO PROGRAM A 77C82

On data I/O EPROM programmer (EPROM MODE)

need : SOCKET 40-28 adaptor

with RESET (pin 14),
INT1 (pin 13),
INT3 (pin 12),
XTAL2 (pin 17) grounded

On EVM (EVM-7000N or EVM-700C)

need : SOCKET 40-28 adaptor
same as the one used for data I/O .
RESET (14) and XTAL2 (17) must be grounded during program and read operations.

VPP : VPP for 77C82 is 12V

On EVM, this option is programmed as follows :

```
? 12                (enter 12V calibrate command)
ARE YOU SURE ? Y    (enter Y, adjust R32 for VPP)
<ANY KEY>           (any key return to monitor)
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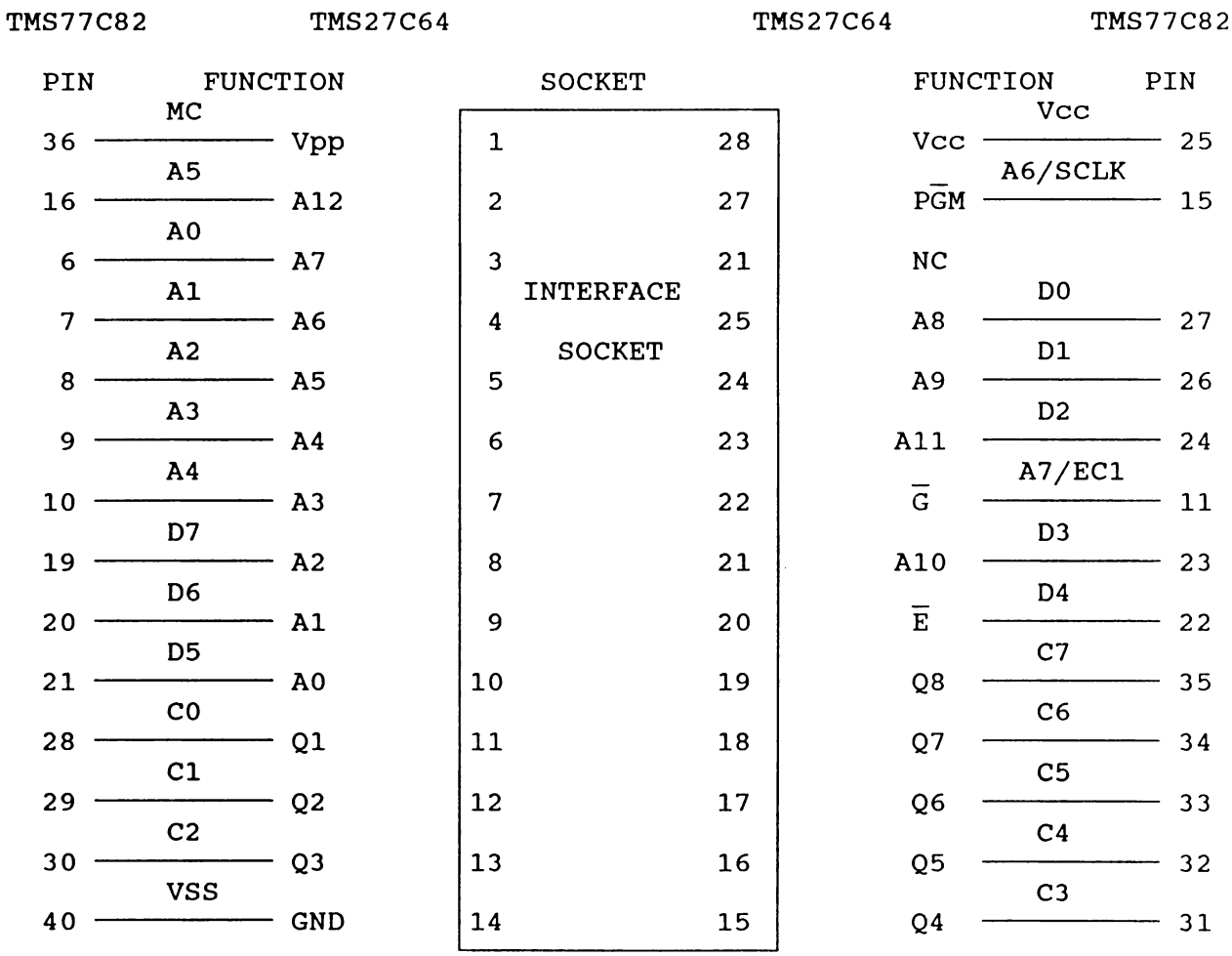

VIII - SIMULATION

The set of instructions and cycle times of the TMS77C82 are identical to that of all TMS7000 microcontrollers.

For TMS77C82 emulation in microcontroller mode, the evaluation module, EVM 7000C-1 equipped with a TMS70C02 CPU together with the programmer socket part # RTC/PGM C82-06, provides a low-cost but complete development tool. Included in the firmware on the EVM are editer, monitor, assembler and debug functions such as single step etc.....

For development & emulation on XDS (TI extended development system) the version to be used is TMDX 70622A1.

The cross-assembler/linker software for TMS77C82 are available for both TI & IBM compatible PC'S (with part # TMDS 7040810-02) and for DEC vax computers (with part # TMDS 7040210-08). In addition a C-compiler exists for IBM compatible PC'S.

All these development tools (and technical literature) are available from TEXAS INSTRUMENTS & authorised distributors.

NOTE

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