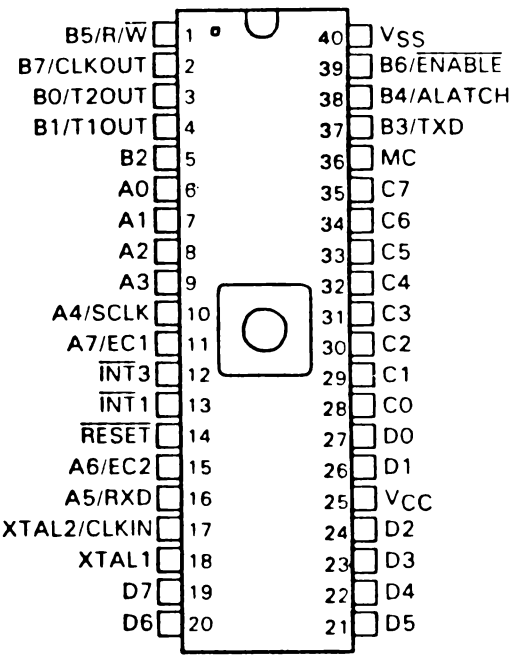
TMS77C82
8 BIT CMOS EPROM MICROCOMPUTER

FEBRUARY 88

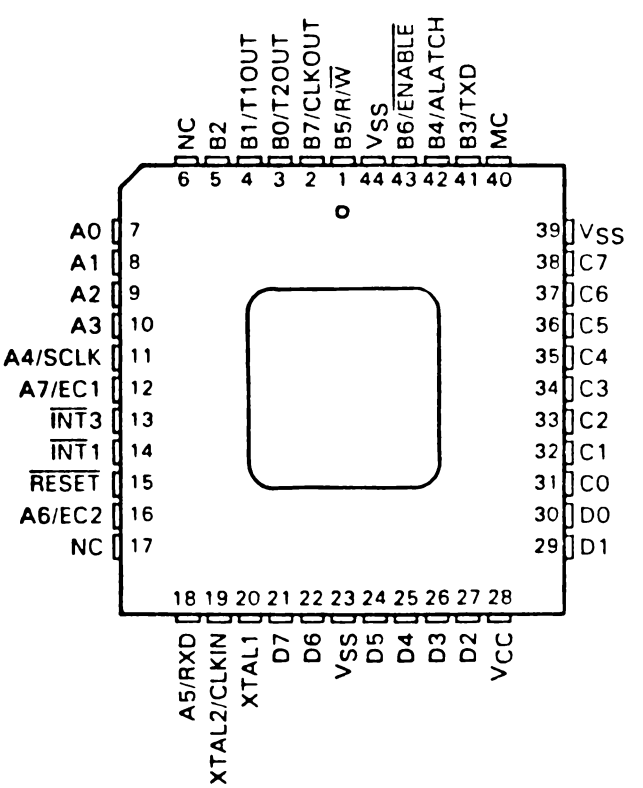
ADVANCE INFORMATION

- Additional Member of TMS7000 Family
  - TMS70C42 Prototyping Device
  - Low-Volume Production Support Option
  - Register-to Register Architecture
  - TMS7000 Instruction Set Compatible
  - Eight Powerful Addressing Formats
- CMOS Technology
  - Low Power Modes
- 8K-Byte On-Chip EPROM with Programming Procedure Compatible with TMS27C64
- Operating Range
  - Voltage (V_{CC}) 3V - 6V
  - Frequency 0.5 MHz to 6.0 MHz
  - Temperature −40°C to 85°C
- Flexible Memory Configurations
  - 256-Byte On-Chip RAM Register File
  - Memory-Mapped Ports
  - Memory Expansion to 64K Bytes
- 32 CMOS Compatible I/O Pins
  - 24 Bidirectional Pins
  - 8 Output Pins
- Three On-Chip Timers:
  - Two Cascadable 16-Bit Timers with 5-Bit Prescale and 16-Bit Capture Latch
  - One 8-Bit Timer with 2-Bit Prescale
  - Internal Interrupt with Timer Reload
- On-Chip Serial Port
  - Flexible Data Protocols
  - Internal or External Baud Rate Generator
  - Asynchronous, Isoynchronous, and Serial I/O Modes
  - Two Multiprocessor Communication Formats
- Flexible Interrupt Handling
  - External Interrupts Programmable for Edge or Edge/Level Triggering and Rising or Falling Edge Detection
  - Priority Servicing of Simultaneous Interrupts
  - Global and Individual Interrupt Masking
- Development Support
  - Low Cost Evaluation Module
  - Full Feature Development System
  - Assembler/Linker Cross Support for Popular Hosts

JD PACKAGE
(TOP VIEW)



FJ PACKAGE
(TOP VIEW)



TEXAS INSTRUMENTS

description

The TMS77C82 is an EPROM version of the 8-bit TMS70C42 microcomputer. The TMS77C82 contains 8K bytes of on-chip EPROM and is completely software and pin compatible with the TMS70C42. Other features include 256 bytes of on-chip RAM, a flexible serial port (UART), three timers, programmable sense interrupts, eight addressing formats, and the same advanced register-to-register architecture that allows direct register arithmetic and logical operations without requiring the use of an accumulator (e.g., ADD R37, R228; add register 37 to register 228 and store the result in register 228).

The TMS77C82 is ideal for low-power applications, and for designs where program constraints are likely to change periodically. The CMOS fabrication, coupled with high-performance CPU and internal peripherals, allows flexible system designs in industrial, automotive, computer, and telecommunications applications. Other uses of this device include prototyping capabilities for the TMS70C42 and a low-volume alternative to masked ROM parts.

The 16-bit timers, with their associated 5-bit prescale, 16-bit capture latch, and timer outputs, simplify A/D conversions, pulse width measurements and other time-critical application designs. For real-time applications where accuracy over long periods is essential, the Timer 1 output may be cascaded into the Timer 2 input to effectively form one 42-bit timer.

The unique serial port can operate in any one of three modes: Asynchronous, Isosynchronous, or Serial I/O. Additional features of the serial port include a selectable protocol (data bits, parity, and stop bits), internal or external baud rate generation, and error detection flags. Direct networking for processor-to-processor communications is also supported through two multiprocessor protocols.

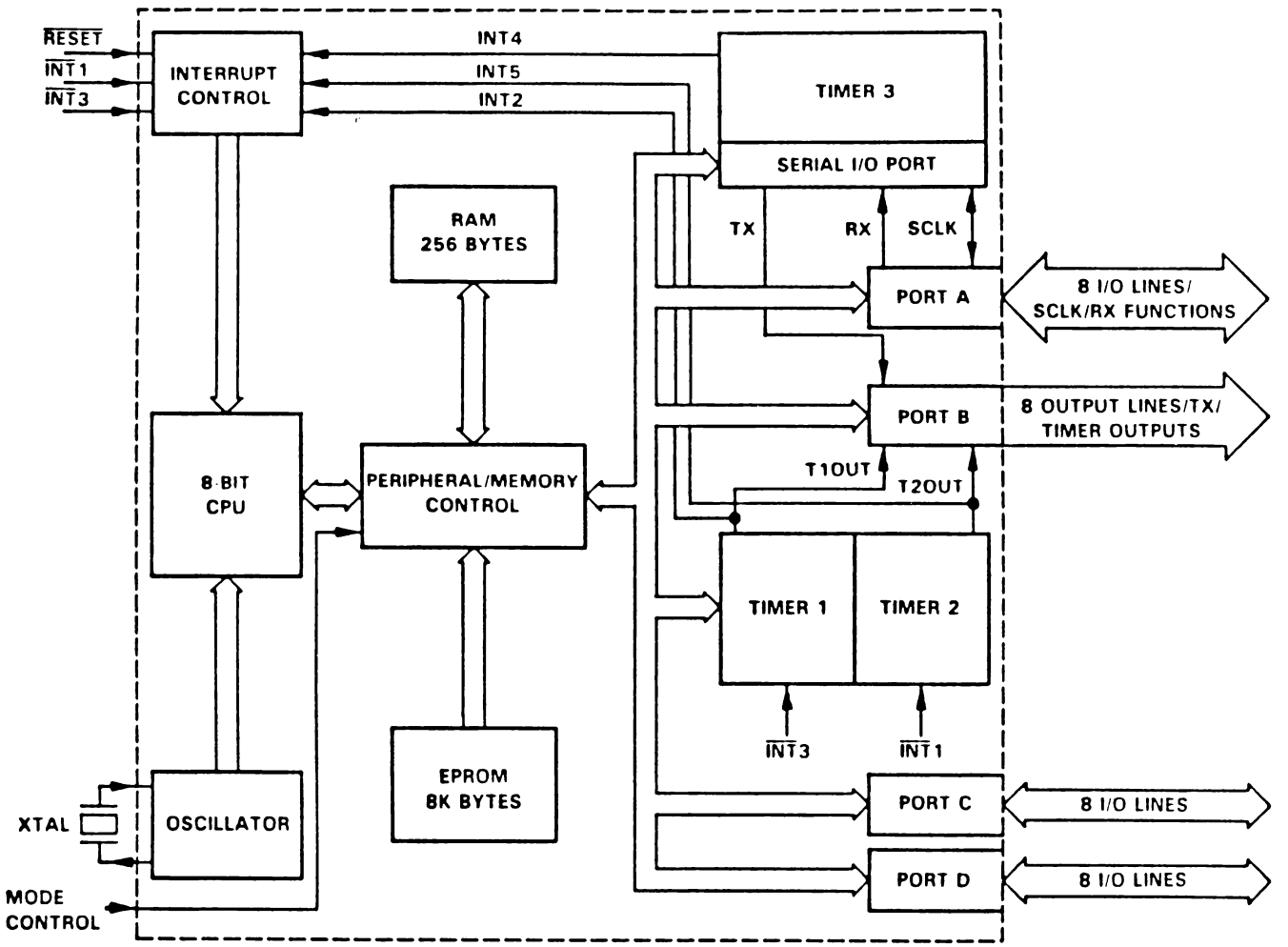
There are six prioritized interrupt levels on the TMS77C82. Level 0 is the non-maskable reset, level 2 is associated with Timer 1, level 4 is associated with the serial port (receive, transmit, and Timer 3), and level 5 is generated by Timer 2. Levels 1 and 3 are external interrupts with programmable edge/edge and level triggering, and rising/falling sense detection. All interrupts are routed through a user-defined vector to the appropriate service routine; therefore, each service routine can be located anywhere in the TMS77C82 address space. There is a global interrupt enable bit in the status register, as well as individual interrupt enable bits for interrupts 1 through 5.

The TMS77C82 can be programmed like any Texas Instruments TMS27C64 on a wide variety of PROM progammers with the aid of an adapter socket (see pages 40 and 41 for schematics). Contact your PROM programmer manufacturer or local TI field sales office for programming support. The TMS77C82 also contains an EPROM integrity feature called the R bit, which may be used to disable external access to the EPROM. Once the R bit has been programmed, the contents of the EPROM cannot be modified and only 1s can be read externally from the EPROM. The only way to modify the R bit protection is to completely erase the contents of the EPROM.

When power consumption is critical, the TMS77C82 can idle selectable sections of the microcomputer (e.g., Timer 1, Timer 2, or UART) and use power only where needed. Also, the entire processor can be halted while retaining the 256 bytes of internal RAM.

The TMS77C82 instruction set is identical to that of all TMS7000 family members, allowing easy transition between members.

functional block diagram



pin descriptions

OPERATION MODES					EPROM MODE		
SIGNAL	PIN NO. LCC	PIN NO. DIP	I/O	DESCRIPTION	SIGNAL	I/O	DESCRIPTION
A0 (LSb)	7	6	I/O	A0-A7 are general-purpose bidirectional pins.	A7	I	A3-A7, A12 are address
A1	8	7	I/O		A6	I	lines.
A2	9	8	I/O		A5	I	
A3	10	9	I/O		A4	I	
A4/SCLK	11	10	I/O	Data I/O/Serial port clock	A3	I	
A5/RXD	18	16	I/O	Data I/O/Serial port receiver	A12	I	
A6/EC2	16	15	I/O	Data I/O/Timer 2 event counter	$\overline{PGM}$	I	Program
A7/EC1	12	11	I/O	Data I/O/Timer 1 event counter	$\overline{G}$	I	Output enable
B0/T2OUT	3	3	O	B0-B3 are outputs. B4-B7 are outputs in Single-Chip mode and memory interface pins in			
B1/T1OUT	4	4	O	all other modes. B0 and B1 are outputs for Timer 2 and Timer 1.			
B2	5	5	O				
B3/TXD	41	37	O	Data output/Serial port transmitter			
B4/ALATCH	42	38	O	Data output/Memory interface address latch strobe			
B5/R/$\overline{W}$	1	1	O	Data output/Memory read/write signal			
B6/$\overline{ENABLE}$	43	39	O	Data output/Memory interface enable strobe			
B7/CLKOUT	2	2	O	Data output/Internal clockout			
C0	31	28	I/O	Port C is a bidirectional data port. In	Q1	I/O	Q1-Q8 are bidirectional
C1	32	29	I/O	Microprocessor, Peripheral-Expansion, and	Q2	I/O	data lines.
C2	33	30	I/O	Full-Expansion modes, Port C is a multiplexed	Q3	I/O	
C3	34	31	I/O	low address and data bus.	Q4	I/O	
C4	35	32	I/O		Q5	I/O	
C5	36	33	I/O		Q6	I/O	
C6	37	34	I/O		Q7	I/O	
C7	38	35	I/O		Q8	I/O	
D0	30	27	I/O	Port D is a bidirectional data port. In	A8	I	A0-A2 and
D1	29	26	I/O	Microprocessor and Full-Expansion modes,	A9	I	A8-A11 are
D2	27	24	I/O	it is the high address bus.	A11	I	address lines.
D3	26	23	I/O		A10	I	
D4	25	22	I/O		$\overline{E}$	I	Chip enable
D5	24	21	I/O		A0	I	
D6	22	20	I/O		A1	I	
D7	21	19	I/O		A2	I	
$\overline{INT1}$	14	13	I	Highest priority maskable external interrupt			
$\overline{INT3}$	13	12	I	Lowest priority maskable external interrupt			
$\overline{RESET}$	15	14	I	Reset	GND		V_{SS} for EPROM mode
MC	40	36	I	Mode control pin, V_{CC} for Microprocessor mode	V_{PP}		Program enable 12.5 V to program (0 V to verify)
XTAL2/CLKIN	19	17	I	Crystal input for control of internal oscillator	GND		V_{SS} for EPROM mode
XTAL1	20	18	O	Crystal output for control of internal oscillator			
V_{CC}	28	25		Supply voltage (positive)	V_{CC}		Supply voltage (6 V)
V_{SS}	23 39 44	40		Ground reference	GND		Ground reference

architecture

memory modes

The TMS77C82 has four different operating modes, allowing the optimization of the on-chip versus off-chip memory for each application. These modes are Single-Chip, Peripheral Expansion, Full Expansion, and Microprocessor. The tables below show the pin conditions that must be met for each mode, the number of I/O pins, and the amount of external address space available in each of the different modes. To enter the EPROM mode, the $\overline{\text{RESET}}$ and XTAL2 pins must be held low.

MODE SELECT		OPERATION MODES				EPROM PROGRAMMING MODE	EPROM VERIFY MODE
		SINGLE-CHIP	PERIPHERAL EXPANSION	FULL EXPANSION	MICROPROCESSOR		
I/O CONTROL REGISTER	BIT 7	0	0	1	X	X	X
	BIT 6	0	1	0	X	X	X
MODE CONTROL PIN		V_{SS}	V_{SS}	V_{SS}	V_{CC}	V_{PP}	V_{SS}
$\overline{\text{RESET}}$ PIN		V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{SS}	V_{SS}
XTAL2 PIN		N/A	N/A	N/A	N/A	V_{SS}	V_{SS}

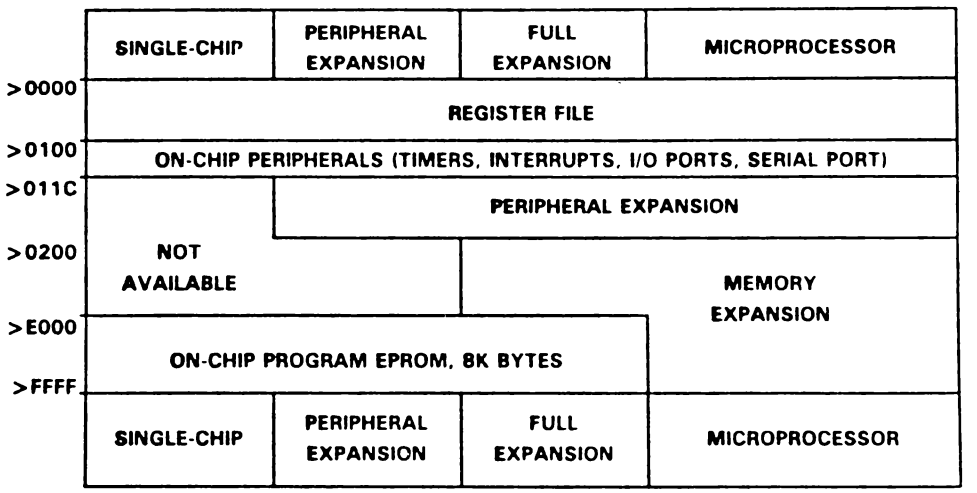
X — Don't care

N/A — Not applicable

	SINGLE-CHIP	PERIPHERAL EXPANSION	FULL EXPANSION	MICROPROCESSOR
I/O Pins:				
Bidirectional	24	16	8	8
Output only	8	4	4	4
Expansion Bus:				
Address only lines	0	0	8	8
Multiplexed Address/Data lines	0	8	8	8
Control lines	0	4	4	4
Memory Space:				
RAM	256	256	256	256
EPROM†	8192	8192	8192	0
Internal Peripheral File	28	25	23	23
External Peripheral File	0	231	233	233
External Memory	0	0	56832	65024

†The first six bytes of masked ROM are reserved for TI internal use.

memory map


SINGLE-CHIP
PERIPHERAL EXPANSION
FULL EXPANSION
MICROPROCESSOR
>0000
REGISTER FILE
>0100
ON-CHIP PERIPHERALS (TIMERS, INTERRUPTS, I/O PORTS, SERIAL PORT)
>011C
PERIPHERAL EXPANSION
>0200
NOT AVAILABLE
MEMORY EXPANSION
>E000
ON-CHIP PROGRAM EPROM, 8K BYTES
>FFFF
SINGLE-CHIP
PERIPHERAL EXPANSION
FULL EXPANSION
MICROPROCESSOR

peripheral memory map

REGISTER	ADDRESS	NAME	NOTE	FUNCTION
P0	>0100	IOCNT0	3	Interrupts 1, 2, and 3, expansion mode control
P1	>0101	IOCNT2		Polarity and edge/level control for $\overline{INT}1$ and $\overline{INT}3$
P2	>0102	IOCNT1	3	Interrupts 4 and 5
P3	>0103	–		Reserved
P4	>0104	APORT		A port data value
P5	>0105	ADDR		A port direction register
P6	>0106	BPORT	1	B port data value
P7	>0107	–		Reserved
P8	>0108	CPORT	1	C port data value
P9	>0109	CDDR	1	C port direction register
P10	>010A	DPORT	2	D port data value
P11	>010B	DDDR	2	D port direction register
P12	>010C	T1MSDATA	3	Timer 1 MSB reload register/MSB readout latch
P13	>010D	T1LSDATA	3	Timer 1 LSB reload register/LSB decrementer value
P14	>010E	T1CTL1	3	Timer 1 control register 1/MSB readout latch
P15	>010F	T1CTL0	3	Timer 1 control register 0/LSB capture latch value
P16	>0110	T2MSDATA	3	Timer 2 MSB reload register/MSB readout latch
P17	>0111	T2LSDATA	3	Timer 2 LSB reload register/LSB decrementer value
P18	>0112	T2CTL1	3	Timer 2 control register 1/MSB readout latch
P19	>0113	T2CTL0	3	Timer 2 control register 0/LSB capture latch value
P20	>0114	SMODE		Serial port mode control register
P21	>0115	SCTL0		Serial port control register 0
P22	>0116	SSTAT		Serial port status register
P23	>0117	T3DATA	3	Timer 3 reload register/decrementer value
P24	>0118	SCTL1		Serial port control register 1
P25	>0119	RXBUF		Receiver buffer
P26	>011A	TXBUF		Transmitter buffer
P27	>011B	–		Reserved
P28-P255	>011C->01FF	–		Peripheral expansion

NOTES: 1. P8, P9, and the most significant nibble of P6 become off-chip in Peripheral Expansion, Full Expansion, and Microprocessor modes.
2. P10 and P11 become off-chip in Full Expansion and Microprocessor modes. All other addresses between P0 and P27 inclusive remain on-chip in all expansion modes.
3. Exercise caution when using logical instructions (e.g., ANDP, ORP, XORP) on these registers because of the different read/write functions.

interrupt priorities

The TMS77C82 has five interrupt levels plus $\overline{RESET}$. These levels are defined as follows:

Level 0: $\overline{RESET}$ (highest priority)
Level 1 ($\overline{INT}1$): External, user-defined, software programmable control over edge/level triggering and polarity
Level 2 (INT2): Timer 1
Level 3 ($\overline{INT}3$): External, user-defined, software programmable contol over edge/triggering and polarity
Level 4 (INT4): Serial port TX ready, RX full, or Timer 3
Level 5 (INT5): Timer 2

device initialization

Interrupt level 0 ($\overline{\text{RESET}}$) cannot be masked and will be recognized immediately, even in the middle of an instruction. To execute the level 0 interrupt, the $\overline{\text{RESET}}$ pin must be held low for a minimum of 1.25 internal clock cycles ($t_{c(C)}$) to guarantee recognition by the device. During assertion of the $\overline{\text{RESET}}$ pin, the following conditions for the indicated locations occur.

PF LOCATIONS	LOCATION	RESET RESULT
P5, P9, P11	Data Direction Registers	Set to all 0s (ports are inputs)
P4, P8, P10	Port A, C, D Output Data Flip Flops	Not affected
P6	Port B Output Data Flip Flops	Set to all 1s
P0, P1	IOCNT0, IOCNT2	Set to all 0s (Bits 7, 6, 3, 2, 0, and IOCNT2 are indeterminate) NOTE: INT1FLG-INT3FLG are cleared
P2	IOCNT1	Bits 3, 2, 0 set to 0 Bits 7, 6, 5, 4, 1 not affected NOTE: INT4FLG is not cleared NOTE: INT5FLG is cleared
P21	SCTLO	Bits 7, 2, 1, 0 set to 0 Bit 6 set to 1 Bits 5, 4, 3 not affected
P22	SSTAT	Bits 6, 1 set to 0 Bits 2, 0 set to 1 Bits 7, 5, 4, 3 not affected
P24	SCTL1	Bits 6, 5, 4, 3, 2 set to 0 Bits 7, 1, 0 not affected
P14	T1CTL1	Bit 6 set to 0 All others not affected
P18	T2CTL1	Bits 7, 6 set to 0 All others not affected

CPU REGISTERS	RESET RESULT
Status Register	Cleared
Stack Pointer	Loaded with >01
Program Counter	Old MSB, LSB loaded into Register A and B PC loaded with reset vector

I/O control registers

The I/O control registers are located in the Peripheral File and are responsible for memory mode definition and interrupt control. In the following figures, each bit in the I/O control registers is defined.

The INTn FLAG values are independent of the INTn ENABLE values. Writing a 1 to the INTn ENABLE will not clear the INTn FLAG. Writing a 1 to the INTn CLEAR bit will clear the corresponding INTn FLAG, but writing a 0 to the INTn CLEAR bit has no effect on the bit.

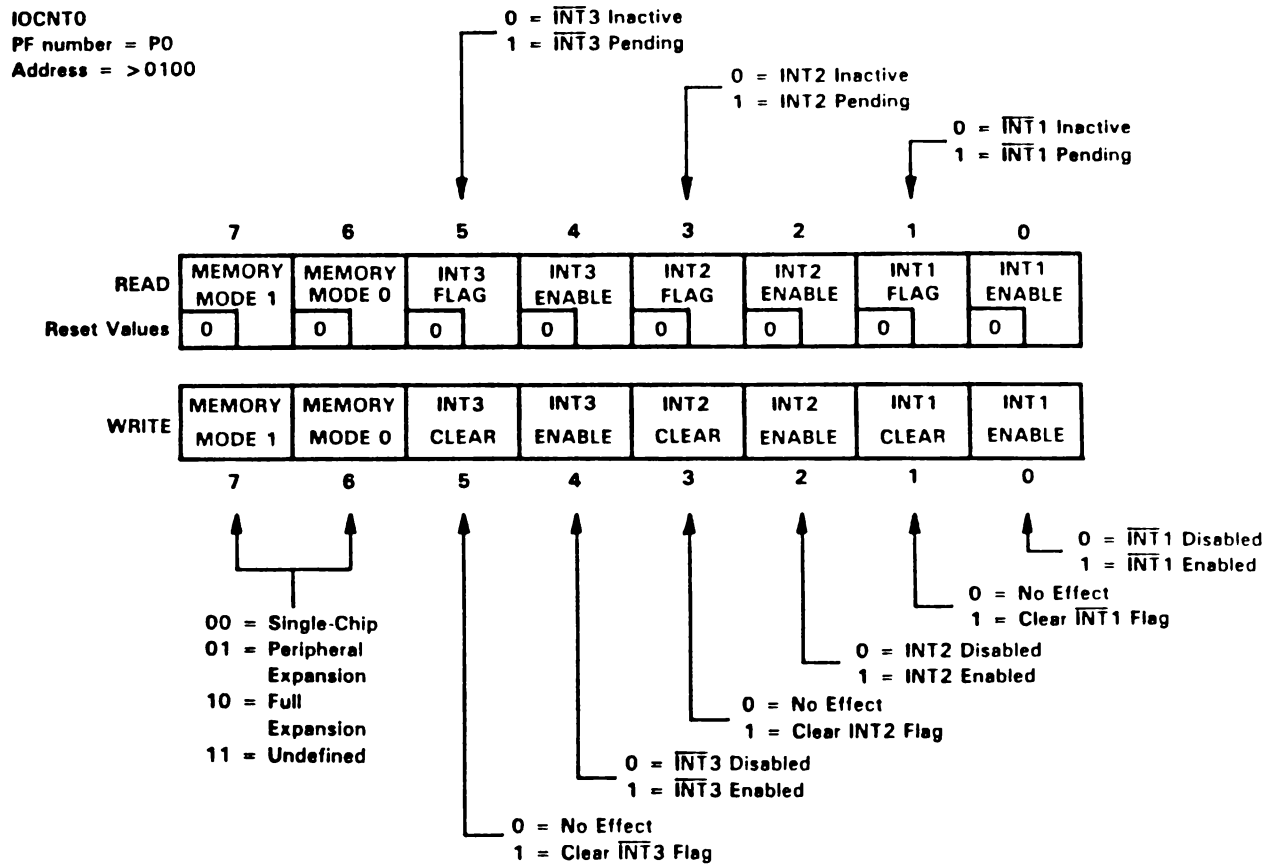


FIGURE 1. I/O CONTROL REGISTER 0 (IOCNTO)

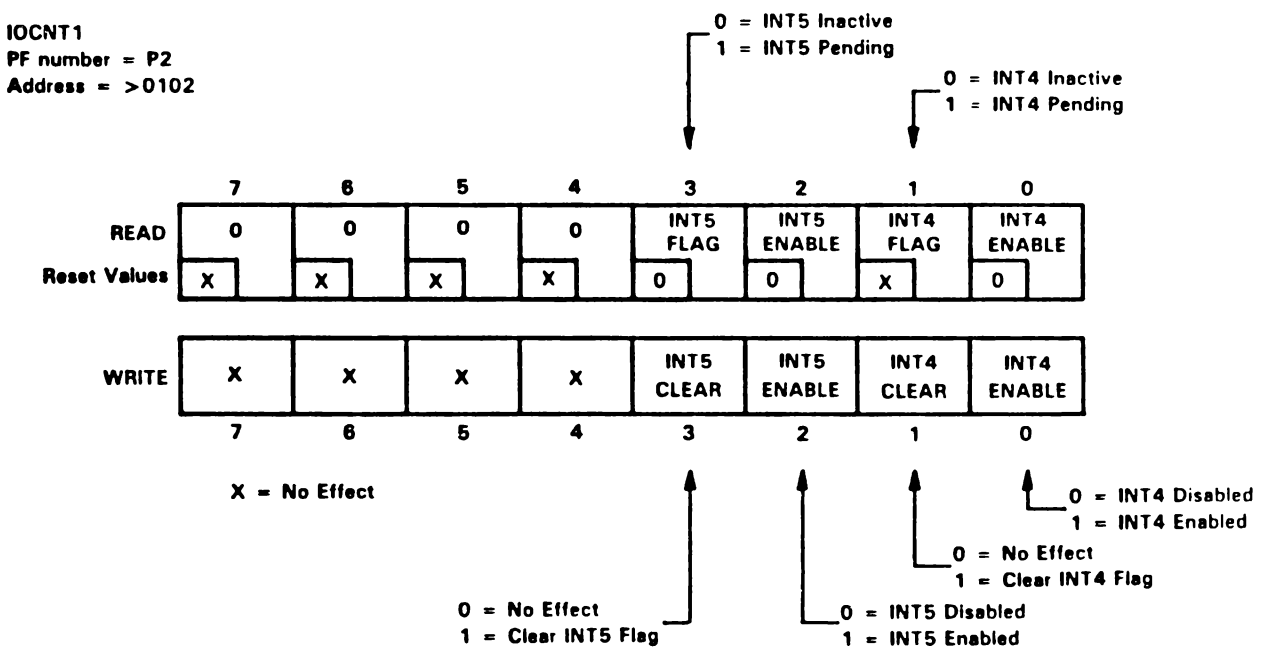
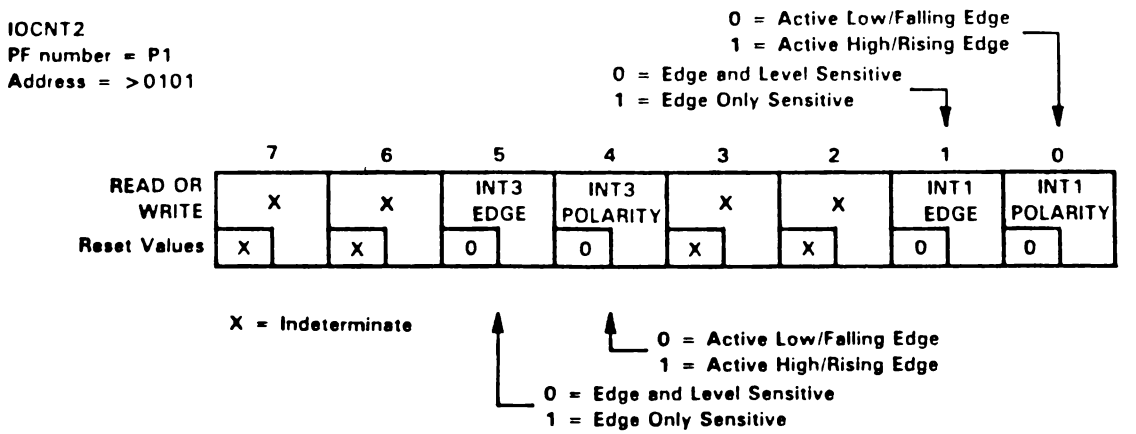


FIGURE 2. I/O CONTROL REGISTER 1 (IOCNT1)



NOTE 4: When changing the sense of $\overline{INT1}$ or $\overline{INT3}$, the interrupt will become active (set the FLAG bit and interrupt the CPU if enabled) if the level present at the interrupt pin corresponds with the new sense selected. Also, the corresponding capture latch will be loaded.

FIGURE 3. I/O CONTROL REGISTER 2 (IOCNT2)

programmable timer/event counter

The TMS77C82 features three on-chip timers with individual start/stop control bits. Timer 1 (shown in Figure 4) and Timer 2 (shown in Figure 7) consist of a 16-bit readable decrementer with a 16-bit reload register, a 16-bit capture latch, and a 5-bit prescaler with a 5-bit reload register. Timer 3 consists of an 8-bit readable decrementer with an 8-bit reload register and a 2-bit prescaler with a 2-bit reload register. Timer 3 can be used as a general-purpose timer or as a baud rate generator for the serial port.

most significant byte readout latch

This latch is shared between the most significant byte (MSB) of the decrementer and the MSB of the capture latch. it allows the complete 16-bit value of the decrementer or the capture latch to be sampled at one moment. The least significant byte (LSB) must be read first, which causes the MSB to be simultaneously loaded into the readout latch.

There is only one readout latch for each timer, but the same latch can be read from two addresses for easier programming (see the diagrams for Timer 1 and Timer 2).

Timer 1 MSB readout latch can be read from both P12 (>010C) and P14 (>010E). Similarly, Timer 2 MSB readout latch can be read from both P16 (>0110) and P18 (>0112).

Reading the LSB of the decrementer or capture latch will always update the contents of the readout latch. In order to correctly read the entire 16-bit value of the decrementer or capture latch, the LSB must be read first, which will load the MSB readout latch. The MSB readout latch must be read and stored before reading the LSB of either the decrementer or capture latch.

The order of 16-bit read operations should be:

Timer 1:
Decrementer: P13 then P12, or P13 then P14
Capture latch: P15 then P12, or P15 then P14

Timer 2:
Decrementer: P17 then P16, or P17 then P18
Capture latch: P19 then P16, or P19 then P18

timer 1 schematic diagram

A schematic diagram of Timer 1 is shown below. For clarity the details of the clock source selection and the power reduction mechanism are covered in Figure 6, Timer 1 Control Registers.

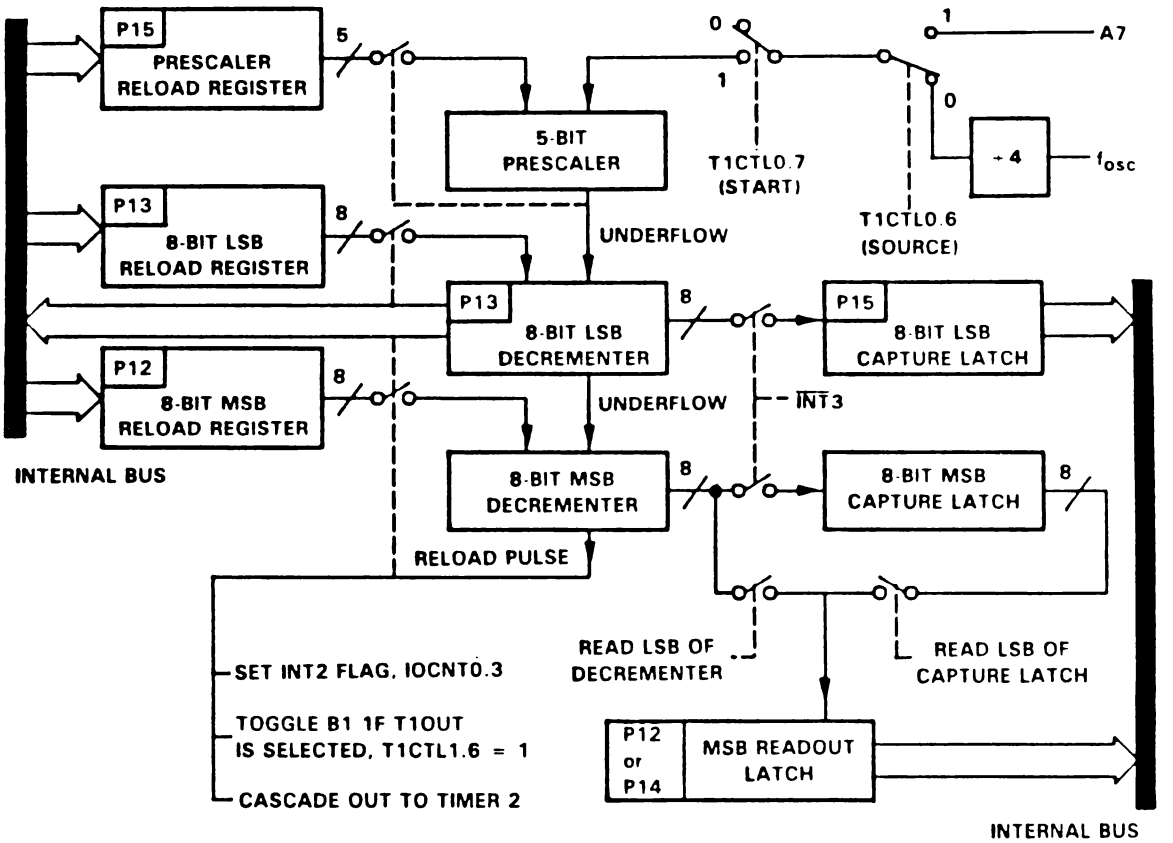


FIGURE 4. TIMER 1 SCHEMATIC DIAGRAM

timer 1 control registers

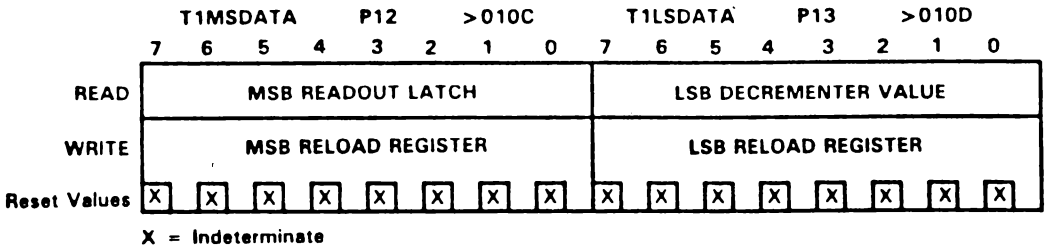


FIGURE 5. TIMER 1 DATA REGISTERS

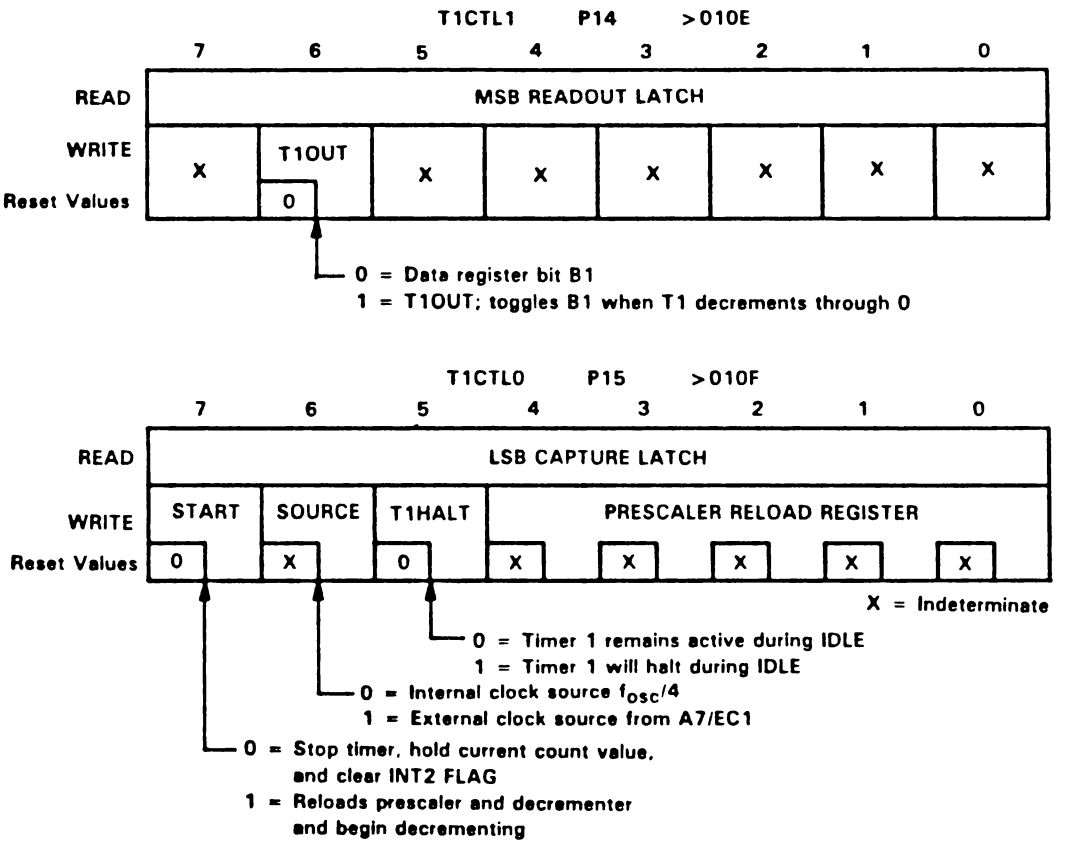


FIGURE 6. TIMER 1 CONTROL REGISTERS

timer 2 schematic diagram

A schematic diagram of Timer 2 is shown below. For clarity the details of the clock source selection and the power reduction mechanism are covered in Figure 9, Timer 2 Control Registers.

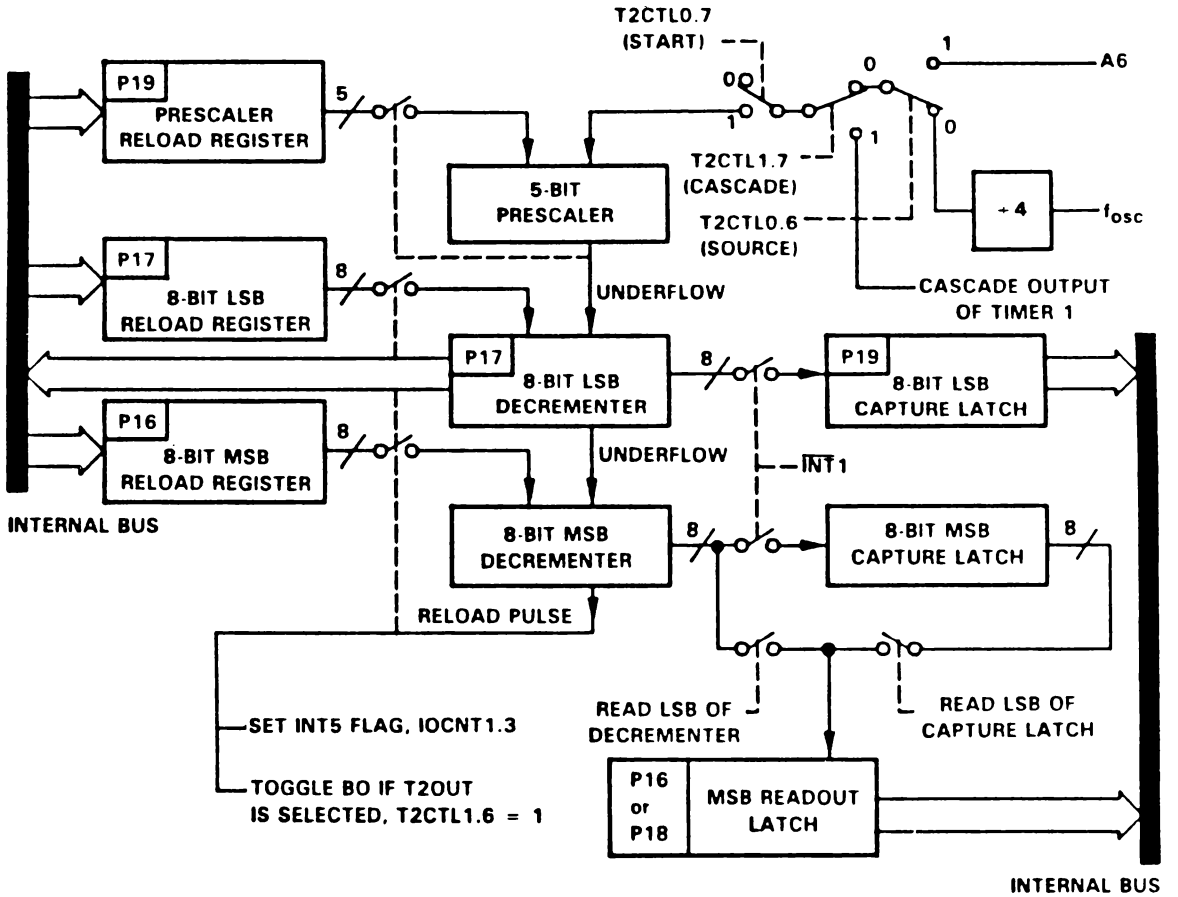


FIGURE 7. TIMER 2 SCHEMATIC DIAGRAM

timer 2 control registers

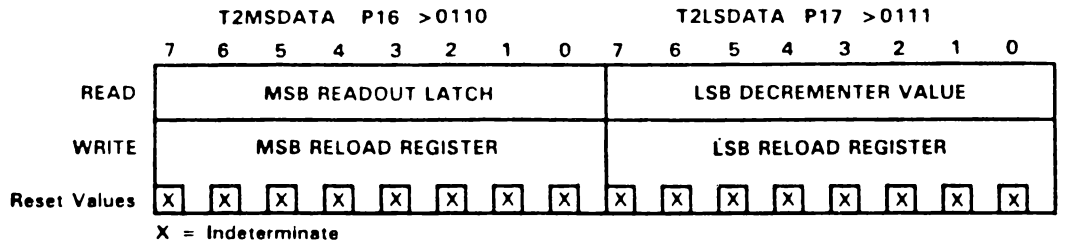
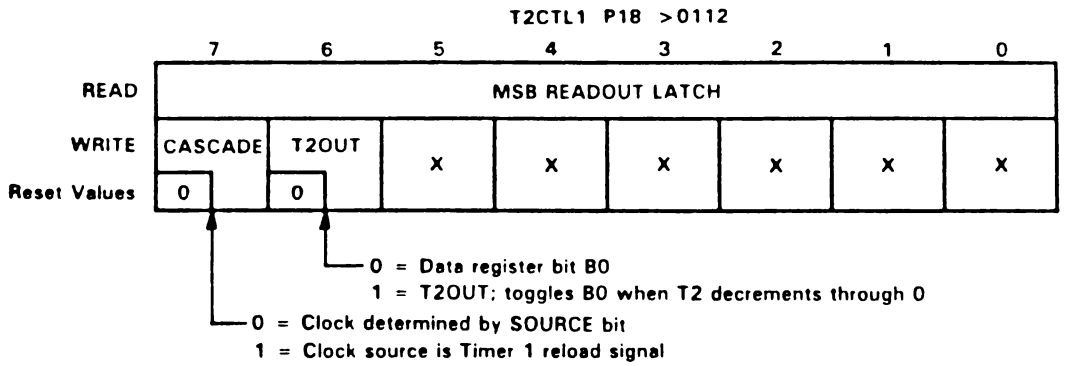


FIGURE 8. TIMER 2 DATA REGISTERS



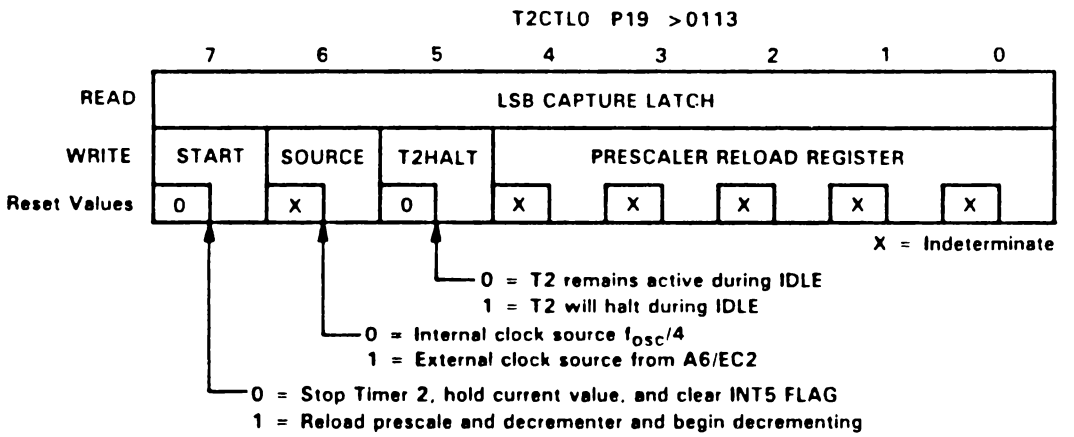


FIGURE 9. TIMER 2 CONTROL REGISTERS

timer 1 and timer 2 clock source

TIMER 1 CLOCK SOURCES

T1CTL0 BIT 6 (SOURCE)	CLOCK SOURCE	MODE
0	$f_{osc}/4$	RTC (Real Time Clock)
1	A7, External	EC (Event Counter)

TIMER 2 CLOCK SOURCES

T2CTL0 BIT 6 (SOURCE)	T2CTL1 BIT 7 (CASCADE)	CLOCK SOURCE	MODE
0	0	$f_{osc}/4$	RTC
1	0	A6, External	EC
X	1	Reload Signal of Timer 1	CASCADE

Bit 7 of timer control registers T1CTL0 and T2CTL0 is the START bit for Timer 1 and Timer 2, respectively. When a 0 is written to the START bit, the timer chain is disabled and frozen at the current count value, and Timer 1's INT2 FLAG or Timer 2's INT5 FLAG is set to 0. When a 1 is written to the START bit, regardless of whether it was a 0 or a 1 before, the prescaler and counter decrementers are loaded with the corresponding latch values, and the Timer/Event Counter operation begins.

When the prescaler and counter decrement through zero together, an interrupt flag is set and the prescaler and counter decrementers are immediately and automatically reloaded with the corresponding values from the reload registers, and counting continues. The interrupts generated by the timers are INT2 for Timer 1 and INT5 for Timer 2.

Timers 1 and 2 each have a 16-bit capture latch which "captures" the current value of the counter whenever the appropriate input capture signal is generated. The capture latch values for Timer 1 and Timer 2 are loaded on the active edges of $\overline{INT3}$ and $\overline{INT1}$, repsectively, whether or not the interrupts are enabled. Both capture latches are disabled during the IDLE instruction when their corresponding timer HALT bits are 1.

event counter (EC)

When Timer 1 or Timer 2 is in the EC mode, pins A7 and A6 are the decrementer clock sources for Timer 1 and Timer 2, respectively. The maximum clock frequency on A7 or A6 in the EC mode must not be greater than $f_{osc}/4$. The minimum pulse width must not be less than 1.25 machine cycles ($t_{c(C)}$). Each positive pulse transition decrements the count chain.

timer output function

A timer output function exists on both Timer 1 and Timer 2 that allows the B1 and B0 outputs, respectively, to be toggled every time the timer decrements through zero. This function is enabled by the T1OUT bit and T2OUT bit (bit 6) in timer control registers T1CTL1 and T2CTL1.

When operating in the timer output mode, the B0 and/or B1 output cannot be changed by writing to the B port data register. Writing to the respective timer's START bit will reload and start the timer, but will not toggle the output. The output will toggle only when the timer decrements through zero. The timer output feature is independent of INT2 and INT5 and, therefore, will operate with INT2 and INT5 enabled or disabled. Also, if the timer is active during the IDLE instruction, the timer output feature will continue to operate.

Whenever the T2OUT or T1OUT bit is returned to 0, B0 or B1 will become an output-only pin, like B2. The value in the B0 or B1 data register will be the last value output by the timer output function, so that B0 or B1 will not change as the T2OUT or T1OUT bit is returned to 0.

Whenever a read of BPORT is performed, the values on the B0 pin and B1 pin will always be returned, so the current timer output values can be read by reading BPORT.

The T1OUT and T2OUT bits are set to 0 by $\overline{\text{RESET}}$, so the timer output function will not be enabled unless the user sets the T1OUT or T2OUT bit to 1.

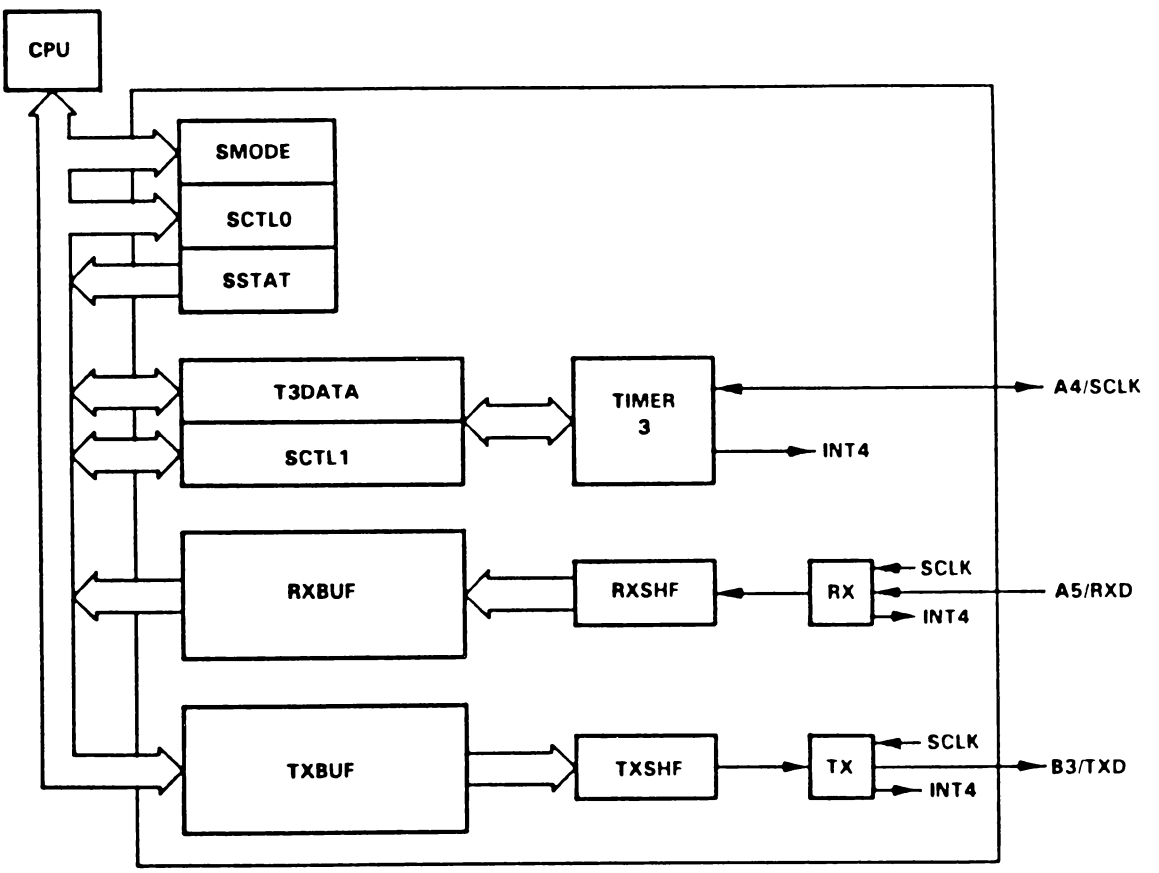
The Timer 2 output (T2OUT) cannot be used if Timer 1 and Timer 2 are cascaded together (CASCADE bit of T2CTL1 set to 1).

serial port

The TMS77C82 contains a serial port which greatly enhances its I/O and communciation capability. The serial port can operate in several modes which permit the TMS77C82 to interface with Universal Asynchronous Receiver/Transmitter (UART) peripheral devices, as well as several microcomputers (e.g., TMS77C82, TMS70C42, TMS7042, TMS7742, 6801, 8051). The serial port consists of a receiver (RX), transmitter (TX), and baud rate generator (Timer 3, T3). It is controlled and accessed through the following registers in the Peripheral File:

REGISTER	ADDRESS	NAME	TYPE	FUNCTION
P20	>0114	SMODE	R/W	Serial Port Mode
P21	>0115	SCTL0	R/W	Serial Port Control 0
P22	>0116	SSTAT	READ	Serial Port Status
P23	>0117	T3DATA	R/W	Timer 3 Data
P24	>0118	SCTL1	R/W	Serial Port Control 1
P25	>0119	RXBUF	READ	Receiver Buffer
P26	>011A	TXBUF	WRITE	Transmission Buffer

For detailed register bit descriptions, refer to the *TMS7000 Family Data Manual,* part number SND001B.



NOTE 5: The INT4 sources are effectively wire-ORed together to generate only one INT4 input. The SCLK sources are wired together to generate only one SCLK input.

FIGURE 10. SERIAL PORT FUNCTIONAL BLOCKS

SMODE
PF number = P20
Address = >0114

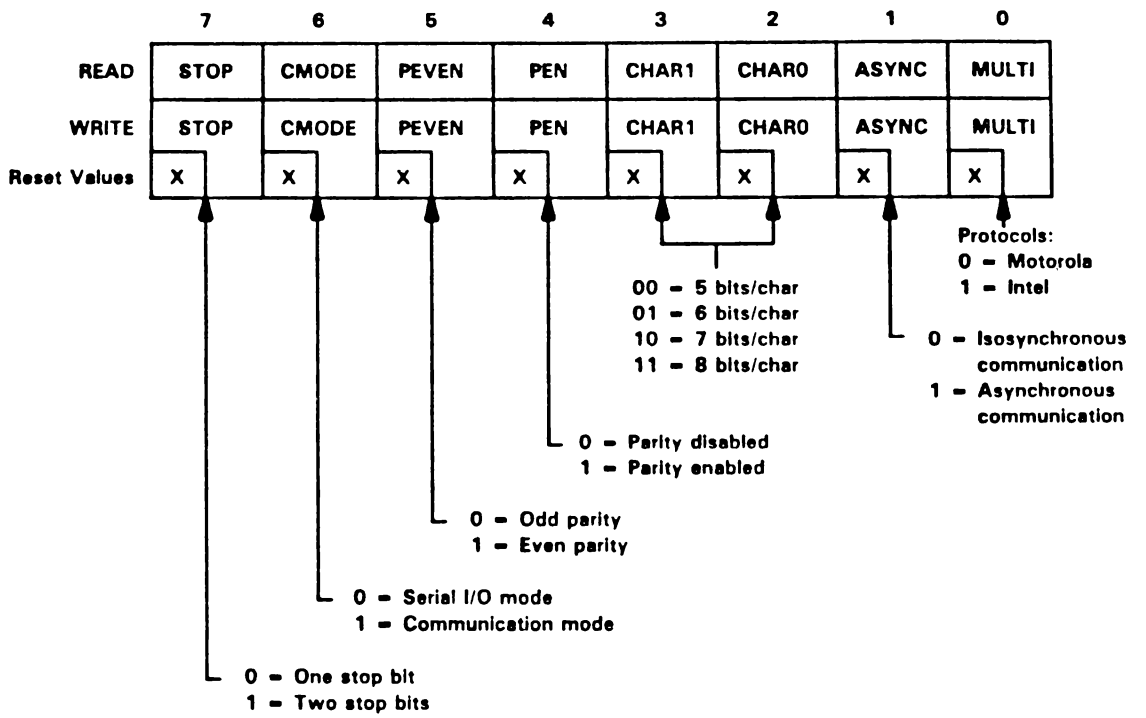


FIGURE 11. SERIAL PORT MODE (SMODE)

SMODE is the RX/TX control register that describes the character format and type of communication mode.

SCTL0
PF number = P21
Address = >0115

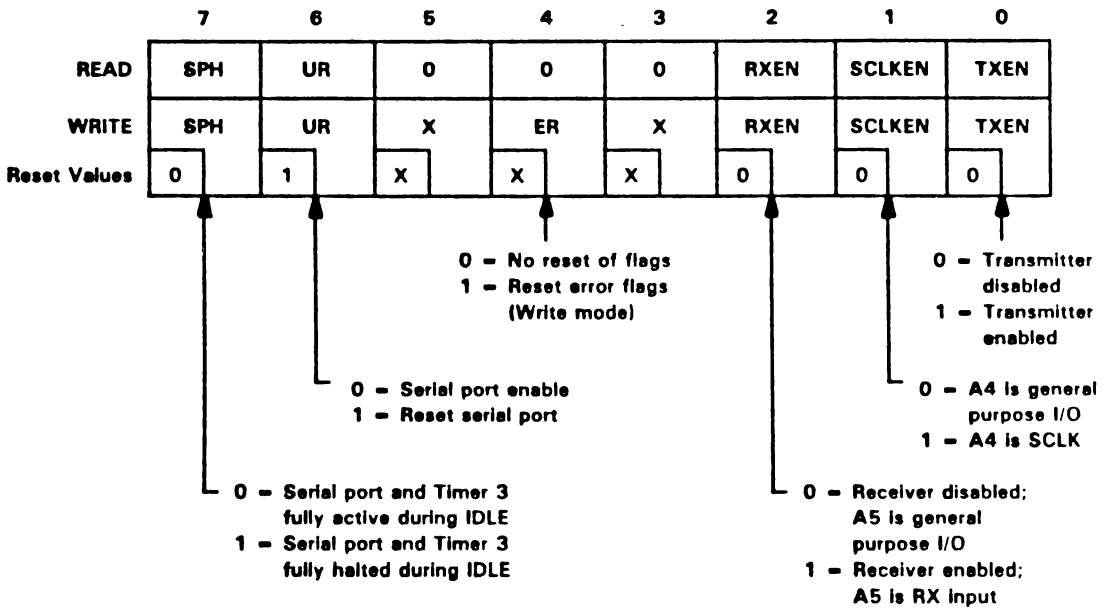


FIGURE 12. SERIAL PORT CONTROL REGISTER 0 (SCTL0)

SCTL0 is RX/TX control register used to control the serial port functions such as TX and RX enable, clearing of error flags, and software enable.

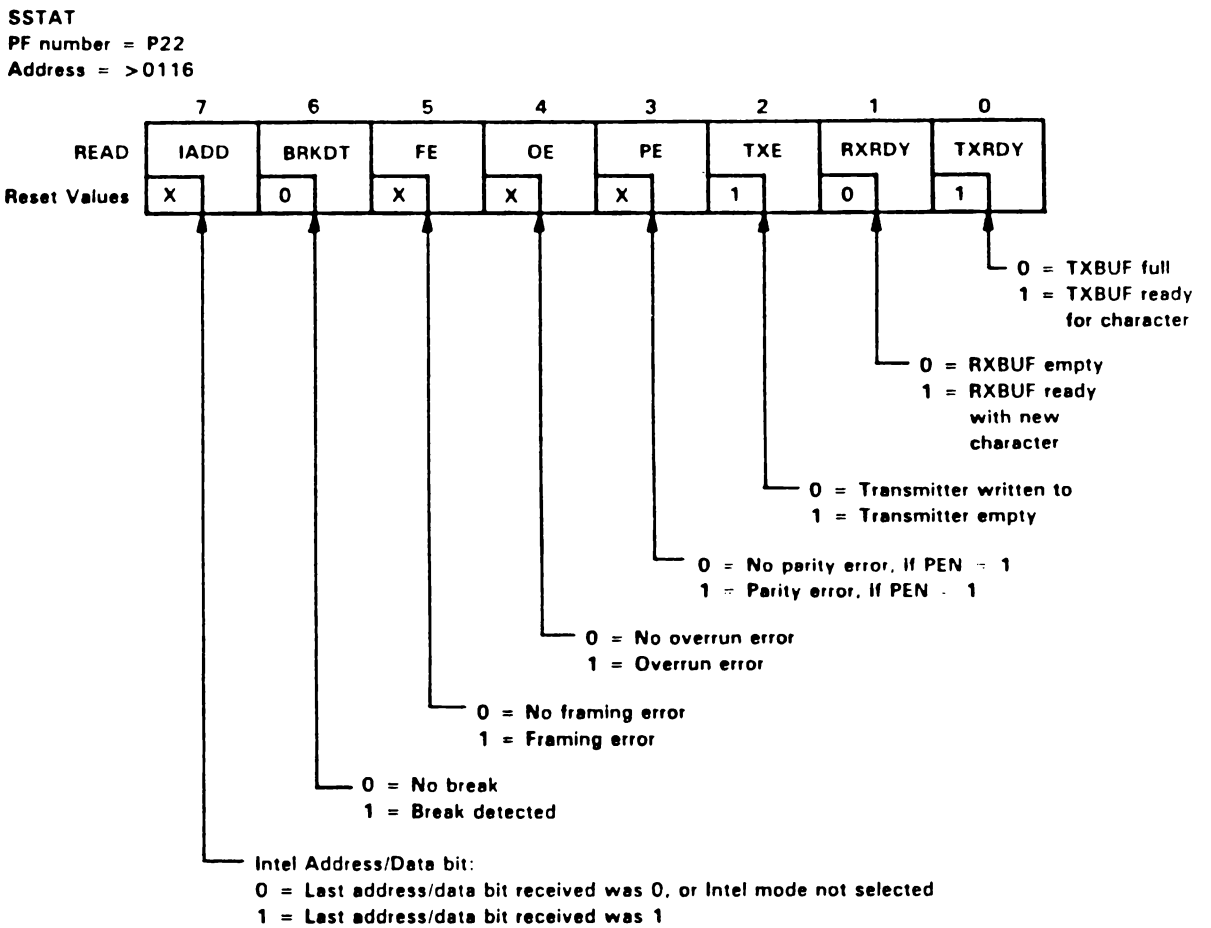


FIGURE 13. SERIAL PORT STATUS (SSTAT)

SSTAT is the read-only register used to report the status of the serial port. Bit 7 (IADD) stores the value of the last address/data bit received when using the Intel multiprocessor mode.

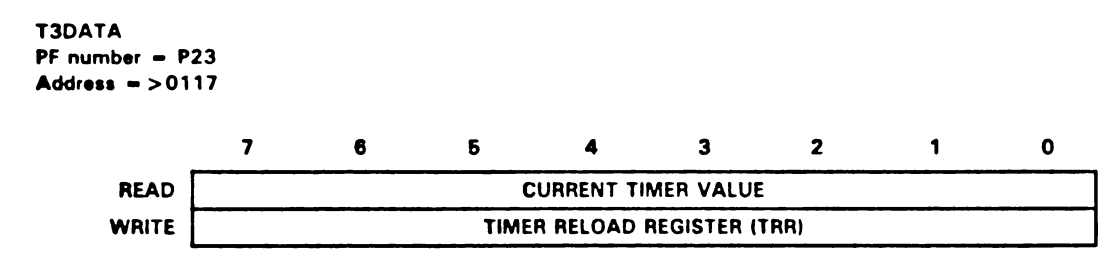


FIGURE 14. TIMER 3 DATA REGISTER (T3DATA)

SCTL1
PF number = P24
Address = >0118

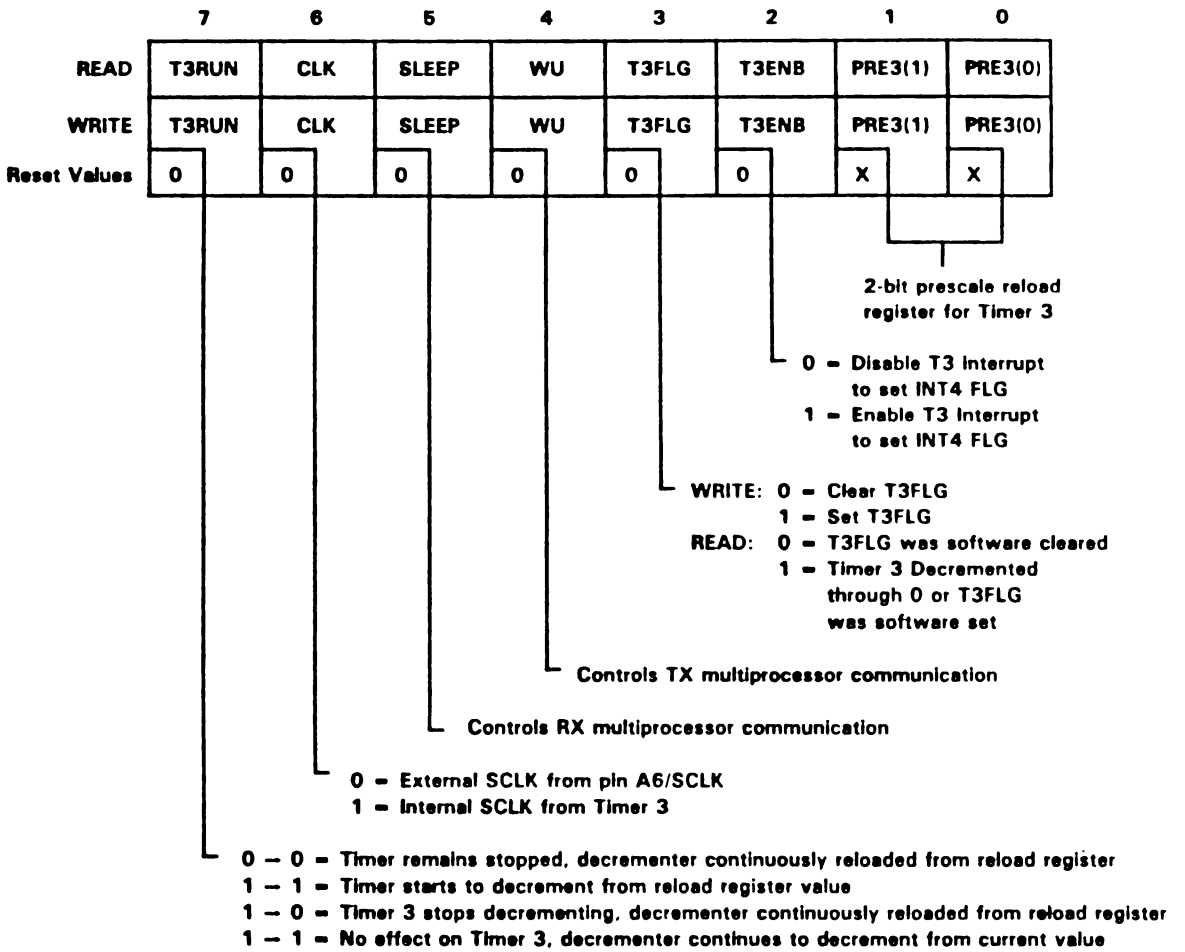


FIGURE 15. SERIAL PORT CONTROL REGISTER (SCTL1)

For a description of the individual timer bits in SCTL1, see the Timer 3 section of this document.

RXBUF
PF number = P25
Address = >0119

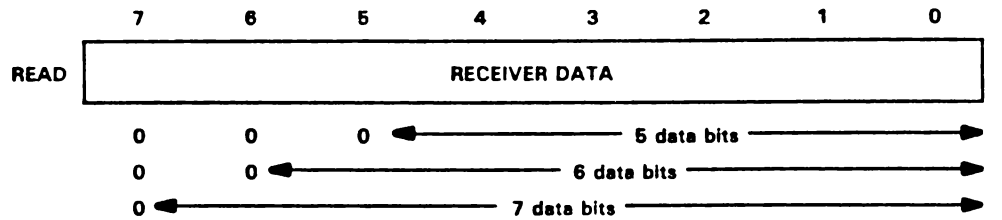
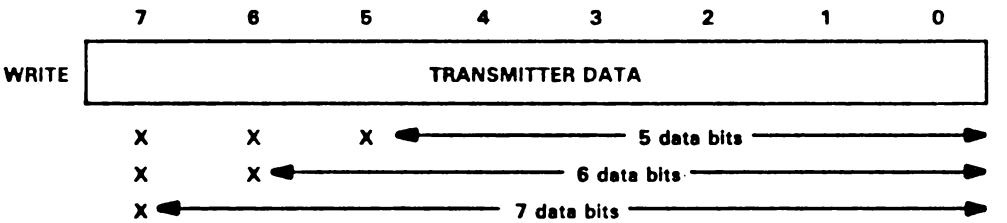


FIGURE 16. RECEIVER BUFFER (RXBUF)

TXBUF
PF number = P26
Address = >011A



X = Ignored

FIGURE 17. TRANSMITTER BUFFER (TXBUF)

serial port clock sources

The serial port can be clocked by Timer 3 or an external baud rate generator. The source of the serial clock (SCLK) is determined by the CLK bit (SCTL1 bit 6) and the SCLKEN bit (SCTL0 bit 1).

SCLKEN	CLK	Serial Port Clock Operation
1	1	A4 is forced to output mode, independent of the data direction register (P5). Timer 3 provides the clock for the Serial Port which is output as SCLK on A4.
1	0	A4 is forced to input mode, independent of the data direction register (P5). An external signal applied to A4 provides the baud rate clock for the Serial Port.
0	1	A4 is available for general-purpose I/O. The clock for the serial port is provided by Timer 3 but is not output on any pin.
0	0	A4 is selected as general-purpose I/O with its direction register controlling the direction of A4. The serial port clock is taken from the A4 pin, so the clock can be provided by an external signal if the pin is in input mode (the same as the SCLKEN = 1, CLK = 0 option above), or by software if the pin is in output mode by writing to the A4 data register.

If SCLKEN is changed from 1 to 0, A4 will have the direction selected by the A port direction register.

In any of these modes, reading from A4 will return the value present at the pin. SCLKEN and CLK are both set to 0 by $\overline{\text{RESET}}$. The A4 direction register is also set to 0 (input) by $\overline{\text{RESET}}$.

timer 3

Timer 3 can be used as a general-purpose timer or as the clock generator for the serial port. Timer 3 is accessed through T3DATA and SCTL1. The Timer 3 clock source is an internal signal with the frequency equal to $f_{osc}/4$. Timer 3 consists of a 2-bit rescaler and an 8-bit counter. These are automatically reloaded from a 2-bit and an 8-bit reload register, respectively, whenever a register decrements through zero.

Timer 3 is continuously reloaded with the prescaler and decrementer reload register values while the T3RUN bit is 0. Timer 3 differs from Timer 1 and Timer 2 in that Timer 3 cannot be held at the value it contained when the T3RUN bit goes to 0. The timer begins decrementing when the T3RUN bit is changed from 0 to 1. The T3RUN bit is initialized to 0 by reset.

Each time the timer decrements through zero, the Timer 3 flag is set to 1 and the INT4 FLAG is set to 1 if T3ENB (SCTL1 bit 2) is 1. Timer 3 and its flags are not affected by the serial port software reset (UR). Therefore, Timer 3 can be used independent of the serial port.

When using Timer 3 as the serial port clock source, the reload pulse (timer decremented through zero) output of Timer 3 goes to the serial port via a divide-by-two circuit, producing an equal mark-space ratio internal SCLK (see Timer 3 block diagram). The baud rate generated by Timer 3 is user-programmable and is determined by the value of the 2-bit prescaler and the 8-bit timer reload registers.

The equations for determining the output baud rates for both the asynchronous and isosynchronous modes are:

$$\text{Asynchronous Baud Rate} = \frac{f_{osc}}{64(PRR+1)(TRR+1)} = \frac{SCLK}{8}$$

$$\text{Isosynchronous Baud Rate} = \frac{f_{osc}}{8(PRR+1)(TRR+1)} = SCLK$$

where: f_{osc} = frequency of the crystal or external system clock
TRR = Timer 3 decrementer reload register (P23)
PRR = Timer 3 prescale reload register (P24)
SCLK = Serial clock either input or output from the SCLK pin

The baud rate for the serial I/O mode is determined with the same equation used to determine the isosynchronous baud rate.

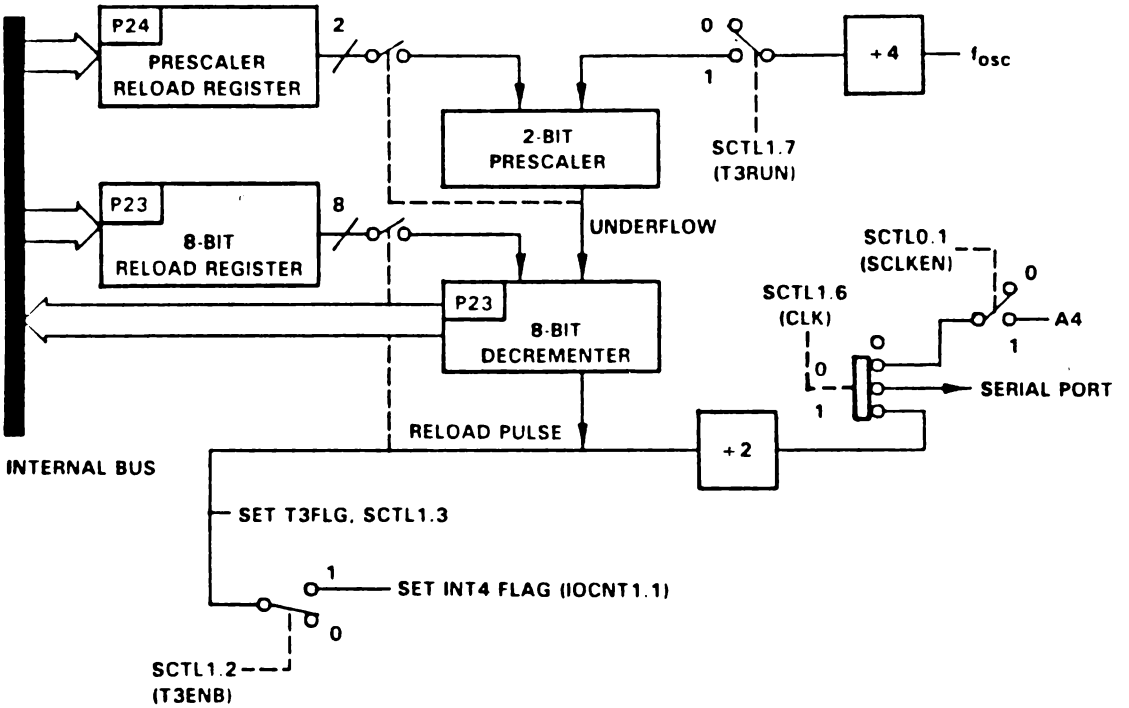


FIGURE 18. TIMER 3 SCHEMATIC DIAGRAM

serial port initialization and reset

After a system reset, the UR bit in SCTL0 will be set to 1 and the serial port will be held in its reset condition. The serial port registers are then set in the order shown below. A serial port reset can be performed by writing a 1 to the UR bit (SCTL0 bit 6) or by writing data to the SMODE register at any time. Whenever a write to the SMODE register is performed, the UR bit is set to 1 and the serial port will be reset. The data written to SMODE will become the new SMODE register contents.

SERIAL PORT INITIALIZATION

SET B3 DATA = 1
WRITE TO SMODE
WRITE TO SCTL0 (SET BIT 6 TO 0)
WRITE TO SCTL1

The BPORT pin 3 must be set to 1 to transmit.

UART reset by software

Setting the UR bit (SCTL0 bit 6) to 1 affects the following:

SCTL0	Bits 7, 2, 1, 0 set to 0 Bit 6 set to 1 Bits 5, 4, 3 not affected
SSTAT	Bits 6, 1 set to 0 Bits 2, 0 set to 1 Bits 7, 5, 4, 3 not affected
SCTL1	Bits 6, 5, 4 set to 0 Bits 7, 3, 2, 1 0 not affected
Pin 37 (B3/TXD)	Outputs the value of bit 3 of P6
Pin 10 (A4/SCLK)	Configures to the corresponding values stored in P4 and P5
Pin 16 (A5/RXD)	Configures to the corresponding values stored in P4 and P5

You cannot write to the affected bits of SCTL0 and SCTL1 while the UR bit is set to 1. The configuration of all bits in SCTL0 can be written to with a single instruction as long as the value of bit 6 (UR) within that instruction is 0.

software example

The following software example initializes the TMS77C82.

```
*****************************************************************************
*       R E S E T    A N D    I N I T I A L I Z A T I O N
*****************************************************************************
*
*                              E Q U A T E   T A B L E
*
APORT   EQU    P4              Port A Data Register
BPORT   EQU    P6              Port B Data Register
CPORT   EQU    P8              Port C Data Register
DPORT   EQU    P10             Port D Data Register
ADDR    EQU    P5              Port A Data Direction Register
CDDR    EQU    P9              Port C Data Direction Register
DDDR    EQU    P11             Port D Data Direction Register
*
*                              I/O CONTROL REGISTERS
*
IOCNT0  EQU    P0              Interrupts 1,2,3 and Expansion mode
IOCNT1  EQU    P2              Interrupts 4,5
IOCNT2  EQU    P1              Polarity and level control for external ints.
*
*                              TIMER 1 REGISTERS
*
T1CTL0  EQU    P15             Timer 1 control register 0
T1CTL1  EQU    P14             Timer 1 control register 1
T1LSDA  EQU    P13             Timer 1 LSB reload Register
T1MSDA  EQU    P12             Timer 1 MSB reload Register
PRESC1  EQU    >00             Timer 1 Prescale value for 10 ms
T10MSL  EQU    >97             Timer 1 MSB value for 10 ms
T10MSM  EQU    >3A             Timer 1 LSB value for 10 ms
```

```
*                               TIMER 2 REGISTERS
*
T2CTL0 EQU   P19                Timer 2 control register 0
T2CTL1 EQU   P18                Timer 2 control register 1
T2LSDA EQU   P17                Timer 2 LSB reload Register
T2MSDA EQU   P16                Timer 2 MSB reload Register
PRESC2 EQU    0                 Timer 2 Prescale value for 10 KHz
T10KHL EQU   74                 Timer 2 MSB value for 10 KHz
T10KHM EQU    0                 Timer 2 LSB value for 10 KHz
*
*                               UART REGISTERS
*
T3DATA EQU   P23                Timer 3 relaod register
SMODE  EQU   P20                Serial port Mode Control Register
SCTL0  EQU   P21                Serial port Control Register 0
SSTAT  EQU   P22                Serial port Status Register
SCTL1  EQU   P24                Serial port Control Register 1
RXBUF  EQU   P25                Receiver buffer
TXBUF  EQU   P26                Transmitter buffer
B300   EQU   103                Count for 300 baud at 6 MHz
*-------------------------------------------------------------------
*
*      T H I S   I S   T H E    R E S E T    E N T R Y    P O I N T
*
START  DINT                     Disable interrupts
       MOVP  %?01000000,SCTL1   Halt timer 3, sleep & WU bits off
*
       MOV   %100,B             Set stack pointer to R100
       LDSP
*
*                               I N T E R R U P T S
*
       MOVP  %?00101110,IOCNT0  Set Mode, enable int 2, clear all flags
       MOVP  %?00001111,IOCNT1  Enable interrupts 4,5 ; clear all flags
       MOVP  %?00000000,IOCNT2  Set INTs sense; type = level
*
*                               P O R T    D A T A
*
       MOVP  %?00001000,APORT   Initialize Port A
       MOVP  %?10111100,BPORT   Initialize Port B (B3=1 for UART operation)
       MOVP  %?10101011,CPORT   Initialize Port C
       MOVP  %?00001001,DPORT   Initialize Port D
       MOVP  %?10001110,ADDR    Initialize Port A
       MOVP  %?10111111,CDDR    Initialize Port C directions registers
       MOVP  %?01001001,DDDR    Initialize Port D directions registers
*
*                               T I M E R   1
*
*      Timer 1 is configured as an internal real time clock which
*      interrupts the CPU every 10 ms (at 6 MHz) on interrupt level 2
*
       MOVP  %?00000000,T1CTL1  Timer 1 output pin turned off
       MOVP  %T10MSL,T1LSDA     LSB timer latch value for 10 ms
       MOVP  %T10MSM,T1MSDA     MSB timer latch value for 10 ms
       MOVP  %>80+PRESC1,T1CTL0 start bit + prescale value set
```

```
*
*                              T I M E R    2
*
*       Timer 2 will output a square wave with a 10 KHz frequency
*       The square wave will output on Port B pin 0.  Once configured,
*       Timer 2 will run continuously, without futher CPU servicing.
*
        MOVP   %?01000000,T2CTL1  Timer 2 output pin turned on
        MOVP   %T10KHL,T2LSDA     LSB timer latch value for 10 KHz
        MOVP   %T10KHM,T2MSDA     MSB timer latch value for 10 KHz
        MOVP   %>80+PRESC2,T2CTL0 Start bit + prescale value set
*
*                              S E R I A L    P O R T
*
        MOVP   %B300,T3DATA       Configure UART at 300 baud
        MOVP   %?01111110,SMODE   data bits =8,Stop=1,Parity=even,Protocol=motor
        MOVP   %?00010100,SCTL0   Reset errors, enable RX,disable sclk and TX
        MOVP   %?11000010,SCTL1   Start UART, CLK=int, prescale=2;sleep & WU=off
*
        EINT                      LET THE INTERRUPTS IN NOW
*
*       E N D   O F   I N I T I A L I Z A T I O N
```

power reduction modes

The TMS77C82 supports the Wake-up and Halt modes for low power consumption. These low power modes are entered via execution of the IDLE instruction. The power reduction mechanisms for each timer and the UART are completely independent of each other and are selected individually via the T1HALT, T2HALT, and SPH bits, located in the T1CTL0, T2CLT0, and SCTL0 registers, respectively.

The Wake-up mode is entered when the IDLE instruction is executed. If the T1HALT, T2HALT, or SPH bits are set, then the corresponding timer or UART will be disabled. The Wake-up mode is exited by assertion of an enabled interrupt to the CPU or $\overline{\text{RESET}}$.

The HALT modes are entered when the IDLE instruction is executed and the T1HALT, T2HALT, and SPH bits are set, causing the corresponding timers and UART to be disabled. The oscillator will be active or inactive depending on which mask option is chosen. The HALT OSC-ON mode is exited by assertion of an enabled external interrupt or $\overline{\text{RESET}}$, while the HALT OSC-OFF mode is exited only by $\overline{\text{RESET}}$.

MODE	FUNCTIONAL BLOCK STATUS			ENTER MODE VIA	EXIT† MODE VIA
	CPU	T1, T2, T3-UART	OSC		
Wake-up	Halted	T1, T2, and T3-UART individually programmed as fully active or halted	Active	IDLE	$\overline{\text{RESET}}$ $\overline{\text{INT}}1$ INT2‡ $\overline{\text{INT}}3$ INT4‡ INT5‡
HALT OSC-ON§	Halted	T1,T2, and T3-UART are all halted	Active	IDLE	$\overline{\text{RESET}}$ $\overline{\text{INT}}1$ $\overline{\text{INT}}3$
HALT OSC-OFF§	Halted	T1, T2, and T3-UART are all halted	Inactive	IDLE	$\overline{\text{RESET}}$

†Interrupts must be enabled to exit.
‡May be used to exit wake-up mode if not programmed to be inactive during IDLE.
§Mask Options. Not programmable.

I/O port operation during power reduction

The following table indicates the state of the memory expansion ports (B, C, and D) in the low power mode, for each of the expansion modes. All of the other I/O pins will maintain their current direction (input or output) and will continue to output the same data if in the output mode. No outputs become three-state when Wake-up mode is entered.

I/O PIN	SINGLE-CHIP	PERIPHERAL EXPANSION	FULL EXPANSION AND MICROPROCESSOR
CLOCKOUT (B7)	B7 data register value	0	0
$\overline{\text{ENABLE}}$ (B6)	B6 data register value	1	1
R/$\overline{\text{W}}$ (B5)	B5 data register value	1	1
ALATCH (B4)	B4 data register value	0	0
ADDR/DATA (C7-C0)	Individual I/O	X	X
HIGH ADDR (D7-D0)	Individual I/O	X	X

X = Indeterminate

capture latch operation during power reduction

In Wake-up mode, Timer 1's capture latch will not be loaded when the $\overline{\text{INT3}}$ pin is taken to its active level if T1HALT is 1. If T1HALT is 0 then the capture latch will be loaded every time the $\overline{\text{INT3}}$ pin is taken to its active level, regardless of the value of the INT3EN flag. Similarly, Timer 2's capture latch in Wake-up mode will be loaded when the $\overline{\text{INT1}}$ pin is taken to its active level if T2HALT is 1. If T2HALT is 0, then the capture latch will be loaded every time the $\overline{\text{INT1}}$ pin is taken to its active level, regardless of the value of the INT1EN flag.

Once the TMS77C82 has been brought out of Wake-up mode, the capture latch will always be loaded when the appropriate interrupt pin is taken to its active level.

instruction set

The TMS7000 family instruction set consists of 57 instructions that control input, output, data manipulation, data comparisons, and program flow. The instruction set is supported with eight addressing modes to provide the flexibility to optimize programs to the user's applications. For example, the MOV instruction has ten operand combinations supported by its addressing modes.

ADDRESSING MODE	EXAMPLE		OPERATION
Single Register	DEC	R24	(R24) – 1 → (R24)
Dual Register	ADD	R32,R17	(R32) + (R17) → (R32)
Peripheral File	XORP	A,P17	(P17) .XOR. (A) → (P17)
Immediate	AND	%>C5,R35	(R35) .AND. >C5 → (R35)
Program Counter Relative	JMP	LABEL	(PC) + off8 → (PC)
Direct Memory	LDA	@>F3D4	(F3D4) → A
Register File Indirect	STA	*R22	(A) → (R22)
Indexed	BR	@>1AAA(B)	(>1AAA) + (B) → (PC)

The CPU controls instruction execution by executing microinstructions from a dedicated control memory. The number of system clock cycles required to execute one assembly language instruction varies depending on the instruction complexity and operand addressing mode. Instruction execution times are stated in terms of the number of system clock cycles per instruction. This decouples the bus transaction protocol/timing from specific memory performance requirements. Instruction execution times vary from 5 to 49 internal system clock cycles, with most instructions requiring less than ten cycles to complete.

Similarly, the number of bytes of program memory required to store an instruction will vary with instruction complexity and addressing mode. TMS7000 instructions require from one to four bytes of program memory space, with most instructions occupying one or two bytes.

The TMS7000 FAMILY INSTRUCTION SET SUMMARY, beginning on page 30, shows the instruction set, the addressing modes, the program memory byte length, and the execution cycle count for each instruction. The Addressing Mode entries are in the format of BYTE LENGTH/CYCLE COUNT. The following symbols and abbreviations are used:

SYMBOL	DEFINITION	SYMBOL	DEFINITION
s	Source Operand	d	Destination Operand
A	Register A or R0 in Register File	B	Register B or R1 in Register File
RF	Source or Destination Register in Register File	label	16-bit Label
Pn	Source or Destination Register in Peripheral File	iop16	16-bit Immediate Operand
Rp	Source or Destination Register Pair (Rn, Rn – 1)	PCN	16-bit Address of Next Instruction
iop	8-bit Immediate Operand	ST	Status Register
off8	8-bit Signed Offset (label – PC)	@	Extended Addressing Operand (Direct, Indirect, Indexed)
PC	Program Counter		
SP	Stack Pointer	→	Is Assigned To
%	Immediate Operand	Stack	Present Address of Stack Pointer
C	Status Register Carry Bit	()	Contents of

TMS7000 FAMILY INSTRUCTION SET SUMMARY

OPERATION		ADDRESSING MODES								DESCRIPTION
		DIRECT				EXTENDED			OTHER	
		A	B	RF	Pn	@label	*RF	@label(B)		
ADC	B,_	1/5								Add with Carry
	RF,_	2/8	2/8	3/10						(s) + (d) + (C) — (d)
	%iop,_	2/7	2/7	3/9						
ADD	B,_	1/5								Add
	RF,_	2/8	2/8	3/10						(s) + (d) — (d)
	%iop,_	2/7	2/7	3/9						
AND	B,_	1/5								And
	RF,_	2/8	2/8	3/10						(s) .AND. (d) — (d)
	%iop,_	2/7	2/7	3/9						
ANDP	A,_				2/10					And Peripheral
	B,_				2/9					(s) .AND. (Pn) — (Pn)
	%iop,_				3/11					
BR	_					3/10	2/9	3/12		Branch
										(d) — (PC)
BTJO†	B,_,off8	2/7								Bit Test and Jump If One
	RF,_,off8	3/10	3/10	4/12						If (s) .AND. (d) ≠ 0, then
	%iop,_,off8	3/9	3/9	4/11						(PC) + off8 — (PC)
BTJOP†	A,_,off8				3/11					Bit Test and Jump If One Peripheral
	B,_,off8				3/10					If (s) .AND. (d) ≠ 0, then
	%iop,_,off8				4/12					(PC) + off8 — (PC)
BTJZ†	B,_,off8	2/7								Bit Test and Jump If Zero
	RF,_,off8	3/10	3/10	4/12						If (s) .AND. NOT (d) ≠ 0, then
	%iop,_,off8	3/9	3/9	4/11						(PC) + off8 — (PC)
BTJZP†	A,_,off8				3/11					Bit Test and Jump If Zero Peripheral
	B,_,off8				3/10					If (s) .AND. NOT (d) ≠ 0, then
	%iop,_,off8				4/12					(PC) + off8 — (PC)
CALL	_					3/14	2/13	3/16		Call
										(SP) + 1 — (SP)
										(PC MSB) — (Stack)
										(SP) + 1 — (SP)
										(PC LSB) — (Stack)
										Operand Address — (PC)
CLR	_	1/5	1/5	2/7						Clear
										0 — (d)
CLRC									1/6	Clear Carry Bit
										0 — (C)
CMP	B,_	1/5								Compare
	RF,_	2/8	2/8	3/10						(d) - (s) computed; sets flags on result
	%iop,_	2/7	2/7	3/9						
CMPA	_					3/12	2/11	3/14		Compare A
										(A) - (s) computed; sets flags on result
DAC	B,_	1/7								Decimal Add with Carry
	RF,_	2/10	2/10	3/12						(s) + (d) + (C) — (d) (BCD)
	%iop,_	2/9	2/9	3/11						

† Add 2 to cycle count if jump is taken.

TMS7000 FAMILY INSTRUCTION SET SUMMARY (CONTINUED)

OPERATION		ADDRESSING MODES								DESCRIPTION
		DIRECT				EXTENDED			OTHER	
		A	B	RF	Pa	@ab	*RF	@ab(B)		
DEC	_	1/5	1/5	2/7						Decrement (d) - 1 → (d)
DECD	_	1/8	1/8	2/11						Decrement Double (Rp) - 1 → (Rp)
DINT									1/5	Disable Interrupts 0 → (Global Interrupt Enable Bit)
DJNZ†	A,off8	2/7								Decrement and Jump If Not 0 (d) - 1 → (d); if (d) ≠ 0, then (PC) + off8 → (PC)
	B,off8		2/7							
	RF,off8			3/9						
DSB	B,_	1/7								Decimal Subtract with Borrow (d) - (s) - 1 + (C) → (d) (BCD)
	RF,_	2/10	2/10	3/12						
	%iop,_	2/8	2/8	3/11						
EINT									1/5	Enable Interrupts 1 → (Global Interrupt Enable Bit)
IDLE									1/6+	Idle (PC) → (PC) until interrupt (PC) + 1 → (PC) after return from interrupt
INC	_	1/5	1/5	2/7						Increment (d) + 1 → (d)
INV	_	1/5	1/5	2/7						Invert NOT(d) → (d)
JMP	off8								2/7	Jump (PC) + off8 → (PC)
Jcnd†	off8									Jump on Condition (PC) + off8 → (PC)
JC									2/5	Jump if Carry
JEQ									2/5	Jump if Equal
JGE									2/5	Jump if Greater Than or Equal
JGT									2/5	Jump if Greater Than
JHS									2/5	Jump if Higher or Same value
JL									2/5	Jump if Lower
JNC									2/5	Jump if No Carry
JNE									2/5	Jump if Not Equal
JNZ									2/5	Jump if Not Zero
JP									2/5	Jump if Positive
JPZ									2/5	Jump if Positive or Zero
JZ									2/5	Jump if Zero
LDA	_					3/11	2/10	3/13		Load Accumulator (s) → (A)
LDSP									1/5	Load Stack Pointer (B) → (SP)
MOV	A,_		1/8	2/8						Move (s) → (d)
	B,_	1/5		2/7						
	RF,_	2/8	2/8	2/10						
	%iop,_	2/7	2/7	3/9						

† Add 2 to cycle count if jump is taken.

TMS7000 FAMILY INSTRUCTION SET SUMMARY (CONTINUED)

OPERATION		ADDRESSING MODES								DESCRIPTION
		DIRECT				EXTENDED			OTHER	
		A	B	RF	Pn	@lab	*RF	@lab(B)		
MOVD	%iop16,_			4/15						Move Double
	%iop16(B),_			4/17						(Rp) — (Rp), or
	Rp,_			3/14						iop16 — (Rp)
MOVP	A,_				2/10					Move Peripheral
	B,_				2/9					(s) — (Pn)
	%iop,_				3/11					
	Pn,_	2/9	2/8							
MPY	B,_	1/44								Multiply
	Rn,_	2/47	2/47	3/49						(s) × (d) — (A,B)
	%iop,_	2/46	2/46	3/48						A = MSB, B = LSB
NOP									1/4	No Operation
										(PC) + 1 — (PC)
OR	B,_	1/5								OR
	RF,_	2/8	2/8	3/10						(s) .OR. (d) — (d)
	%iop,_	2/7	2/7	3/9						
ORP	A,_				2/10					OR Peripheral
	B,_				2/9					(s) .OR. (Pn) — (Pn)
	%iop,_				3/11					
POP	_	1/6	1/6	2/8						Pop
										(Stack) — (d); (SP) - 1 — (SP)
POP	ST								1/6	Pop Status
										(Stack) — (ST); (SP) - 1 — (SP)
PUSH	_	1/6	1/6	2/8						Push
										(s) — (Stack)
										(SP) + 1 — (SP)
PUSH	ST								1/6	Push Status
										Status Register — (Stack);
										(SP) + 1 — (SP)
RETI									1/9	Return from Interrupt
										(Stack) — (PC) LSB
										(SP) - 1 — (SP)
										(Stack) — (PC) MSB
										(SP) - 1 — (SP)
										(Stack) — (Status Register)
										(SP) - 1 — (SP)
RETS									1/7	Return from Subroutine
										(Stack) — (PC) LSB
										(SP) - 1 — (SP)
										(Stack) — (PC) MSB
										(SP) - 1 — (SP)
RL	_	1/5	1/5	2/7						Rotate Left
										Bit(n) — Bit(n + 1)
										Bit(7) — Bit(0) + (C)

TMS7000 FAMILY INSTRUCTION SET SUMMARY (CONCLUDED)

OPERATION		ADDRESSING MODES								DESCRIPTION
		DIRECT				EXTENDED			OTHER	
		A	B	RF	Pn	@lab	*RF	@lab(B)		
RLC	_	1/5	1/5	2/7						Rotate Left Through Carry Bit(n) — Bit(n + 1) (C) — Bit(0) Bit(7) — (C)
RR	_	1/5	1/5	2/7						Rotate Right Bit(n) — Bit(n + 1) Bit(0) — Bit(7) + (C)
RRC	_	1/5	1/5	2/7						Rotate Right Through Carry Bit(n) — Bit(n + 1) (C) — Bit(n) Bit(0) — (C)
SBB	B,_	1/5								Subtract with Borrow (s) − (d) − 1 + (C) — (d)
	RF,_	2/8	2/8	3/10						
	%iop,_	2/7	2/7	3/9						
SETC									1/5	Set Carry 1 — (C)
STA	_					3/11	2/10	3/13		Store Accumulator; (A) — (d)
STSP									1/6	Store Stack Pointer (SP) — (B)
SUB	B,_	1/5								Subtract (d) − (s) — (d)
	RF,_	2/8	2/8	3/10						
	%iop,_	2/7	2/7	3/9						
SWAP	_	1/8	1/8	2/10						Swap Nibbles d(Hn,Ln) — d(Ln,Hn)
TRAP	0-23								1/14	Trap (SP) + 1 — (SP) (PC MSB) — (Stack) (SP) + 1 — (SP) (PC LSB) — (Stack) (Entry Vector) — (PC)
TSTA									1/6	Test A C — 0 N, Z set on (A)
TSTB									1/5	Test B C — 0 N, Z set on (B)
XCHB	_	1/8		2/8						Exchange B (B) — (d)
XOR	B,_	1/5								Exclusive OR (s) .XOR. (d) — (d)
	RF,_	2/8	2/8	3/10						
	%iop,_	2/7	2/7	3/9						
XORP	A,_				2/10					Exclusive OR Peripheral (s) .XOR. (Pn) — (Pn)
	B,_				2/9					
	%iop,_				3/11					

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 6) . . . . . −0.3 to 7 V
Supply voltge, V_{PP} (MC pin) . . . . . −0.3 V to 14 V
Input voltage range . . . . . −0.3 V to V_{CC} +0.3 V
Output voltage range . . . . . −0.3 V to V_{CC} +0.3 V
Maximum I/O buffer current (per pin) . . . . . ±10 mA
Maximum supply current, I_{CC} . . . . . 60 mA
Maximum supply current, I_{SS} . . . . . −60 mA
Storage temperature range . . . . . −55°C to 150°C
Operating free air temperature . . . . . −40°C to 85°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 6: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage		3		6	V
Programming supply voltage (MC pin)		12	12.5	13	V
INT1, INT3, RESET, X'TAL PIN					
High level input voltage	$5.5V \leqslant V_{CC} \leqslant 6V$	$V_{CC}-1.0$		V_{CC}	V
	$4.5V \leqslant V_{CC} \leqslant 5.5V$	$V_{CC}-0.7$		V_{CC}	V
	$3.5V \leqslant V_{CC} \leqslant 4.5V$	$V_{CC}-0.5$		V_{CC}	V
	$2.5V \leqslant V_{CC} \leqslant 3.5V$	$V_{CC}-0.35$		V_{CC}	V
Low level input voltage	$5.5V \leqslant V_{CC} \leqslant 6V$	0		1.00	V
	$4.5V \leqslant V_{CC} \leqslant 5.5V$	0		0.70	V
	$3.5V \leqslant V_{CC} \leqslant 4.5V$	0		0.50	V
	$2.5V \leqslant V_{CC} \leqslant 3.5V$	0		0.35	V
MC PIN					
High level input voltage, VIH	$5V \leqslant V_{CC} \leqslant 6V$	$V_{CC}-0.5$		V_{CC}	V
	$4V \leqslant V_{CC} \leqslant 5V$	$V_{CC}-0.4$		V_{CC}	V
	$3V \leqslant V_{CC} \leqslant 4V$	$V_{CC}-0.3$		V_{CC}	V
	$2.5V \leqslant V_{CC} \leqslant 3V$	$V_{CC}-0.2$		V_{CC}	V
Low level input voltage, VIL	$5V \leqslant V_{CC} \leqslant 6V$	0		0.5	V
	$4V \leqslant V_{CC} \leqslant 5V$	0		0.4	V
	$3V \leqslant V_{CC} \leqslant 4V$	0		0.3	V
	$2.5V \leqslant V_{CC} \leqslant 3V$	0		0.2	V
PORT (EXCEPT INT1, INT3, RESET, X'TAL, MC					
High level input voltage, VIH	$5V \leqslant V_{CC} \leqslant 6V$	$V_{CC}-1.3$		V_{CC}	V
	$4V \leqslant V_{CC} \leqslant 5V$	$V_{CC}-1.0$		V_{CC}	V
	$3V \leqslant V_{CC} \leqslant 4V$	$V_{CC}-0.7$		V_{CC}	V
	$2.5V \leqslant V_{CC} \leqslant 3V$	$V_{CC}-0.4$		V_{CC}	V
Low level input voltage, VIL	$5V \leqslant V_{CC} \leqslant 6V$	0		1.5	V
	$4V \leqslant V_{CC} \leqslant 5V$	0		1.1	V
	$3V \leqslant V_{CC} \leqslant 4V$	0		0.7	V
	$2.5V \leqslant V_{CC} \leqslant 3V$	0		0.3	V

ADVANCE INFORMATION

electrical characteristics over full range of operating conditions (V_{CC} = 4.5 V to 5.5 V)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ICC Supply current	Operating mode	V_{CC} = 5.0 V, f = 6.0 Mhz		16.1	24.8	mA
		V_{CC} = 5.0 V, f = 4.0 Mhz		14.4	22.2	mA
		V_{CC} = 5.0 V, f = 1.0 Mhz		11.2	17.2	mA
	Wake-up modes 1 & 5 (see Note 1)	<Freq = F Mhz> <Freq = 6.0 Mhz>		1.2*F + 0,3 7.5	2.0*F + 0,5 12.5	mA mA
	Wake up mode 2 (see Note 1)	<Freq = F Mhz> <Freq = 6.0 Mhz>		0.86*F + 0.3 5.5	1.44*F + 0.5 9.1	mA mA
	Wake-up modes 3 & 4 (see Note 1)	<Freq = F MHz> <Freq = 6 MHz>		0.52*F + 0.3 3.4	0.8*F + 0.5 5.8	mA mA
	Halt-off mode	V_{CC} = 5 V			See note 2	μA
V_{OH} High-level output voltage		V_{CC} = 5.0 V, I_{OH} = −1.0 mA	2.50	4.5		mA
		V_{CC} = 5.0 V, I_{OH} = 0.3 mA	4.50	4.8		V
V_{OL} Low-level output voltage		V_{CC} = 5.0, I_{OL} = 1.7 mA		0.3	0.4	V
I_{OH} Output source current ($V_{HO} = V_{CC} - 0.5$ V)		V_{CC} = 3.0 V	−100	−700		μA
		V_{CC} = 4.0 V	−0.2	1.0		mA
		V_{CC} = 5.0 V	−0.3	−1.2		mA
	V_{OH} = 2.5 V	V_{CC} = 5.0 V	−1.0	−5.0		mA
I_{OL} Output sink current (V_{OL} = 0.4 V)		V_{CC} = 3.0 V	0.7	2.0		mA
		V_{CC} = 4.0 V	1.02	0.4		mA
		V_{CC} = 5.0 V	1.7	2.0		mA
I_I Input leakage current	MC	$V_I = V_{SS}$ or V_{CC}		±0.1	±5	μA
	All others	$V_I = V_{SS}$ to V_{CC}		±0.1	±5	μA
C_I Input capacitance				5		pF

All inputs = V_{CC} or V_{SS} (except XTAL2). All I/O and output pins are open circuit.

Note 1:

MODE	TIMER-1		TIMER-2	UART
WAKE-UP1	USE		USE	USE
WAKE-UP2	TIMER-1	OR	USE	USE
WAKE-UP3	OFF		OFF	USE
WAKE-UP4	TIMER-1	OR	USE	OFF
WAKE-UP5	USE		USE	OFF
HALT-OFF	OFF		OFF	OFF

Note 2:

TMS 77C82BJDL TMS 77C82BNL/NLL/FNL	$I_{Halt-off}$ = 10μA
TMS 77C82JDL TMS 77C82NL/NLL/FNL	$I_{Halt-off}$ = 500μA

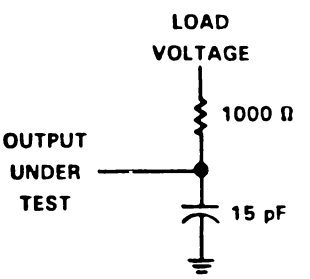
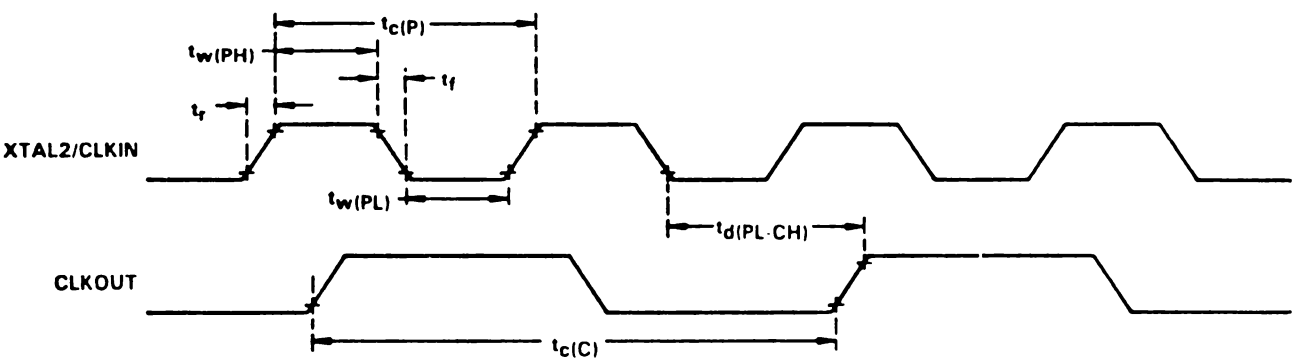


FIGURE 26. OUTPUT LOAD CIRCUIT USED FOR ALL TIMING MEASUREMENTS

recommended crystal operating conditions over full operating range

PARAMETER			MIN	TYP	MAX	UNIT
f_{osc}	Crystal frequency	V_{CC} = 3.0 V	0.5		1.0	MHz
		V_{CC} = 4.0 V	0.5		3.0	MHz
		V_{CC} = 5.0 V ± 10%	0.5		6.0	MHz
		V_{CC} = 6.0 V	0.5		6.0	MHz
	CLKIN duty cycle		45		55	%
$t_{c}(P)$	Crystal cycle time	V_{CC} = 2.5 V	1000		2000	ns
		V_{CC} = 4.0 V	333		2000	ns
		V_{CC} = 5.0 V	167		2000	ns
		V_{CC} = 6.0 V	167		2000	ns
$t_{c}(C)$	Internal state cycle time	V_{CC} = 2.5 V	2000		4000	ns
		V_{CC} = 4.0 V	666		4000	ns
		V_{CC} = 5.0 V	333		4000	ns
		V_{CC} = 6.0 V	333		4000	ns
$t_{w}(PH)$	CLKIN pulse duration high		50			ns
$t_{w}(PL)$	CLKIN pulse duration low		50			ns
t_{r}	CLKIN rise time				30	ns
t_{f}	CLKIN fall time				30	ns
$t_{d}(PL\text{-}CH)$	CLKIN fall to CLKOUT rise delay time			140	250	ns

clock timing



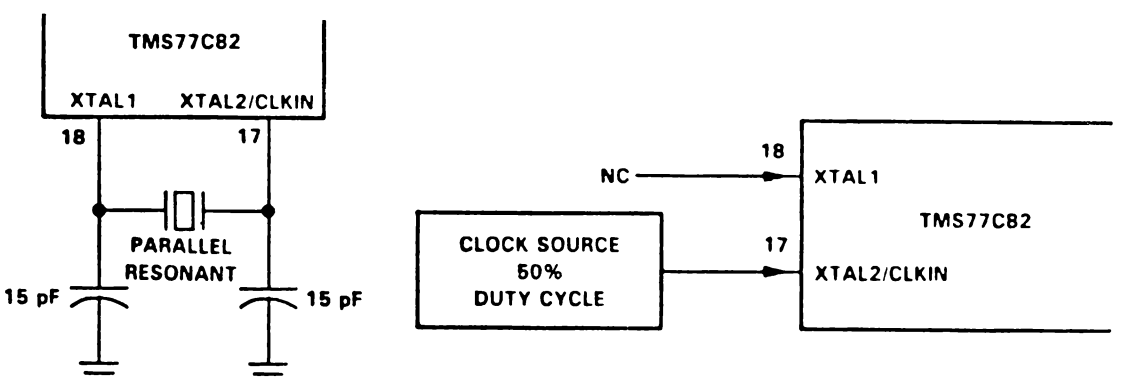


FIGURE 27. RECOMMENDED CLOCK CONNECTIONS

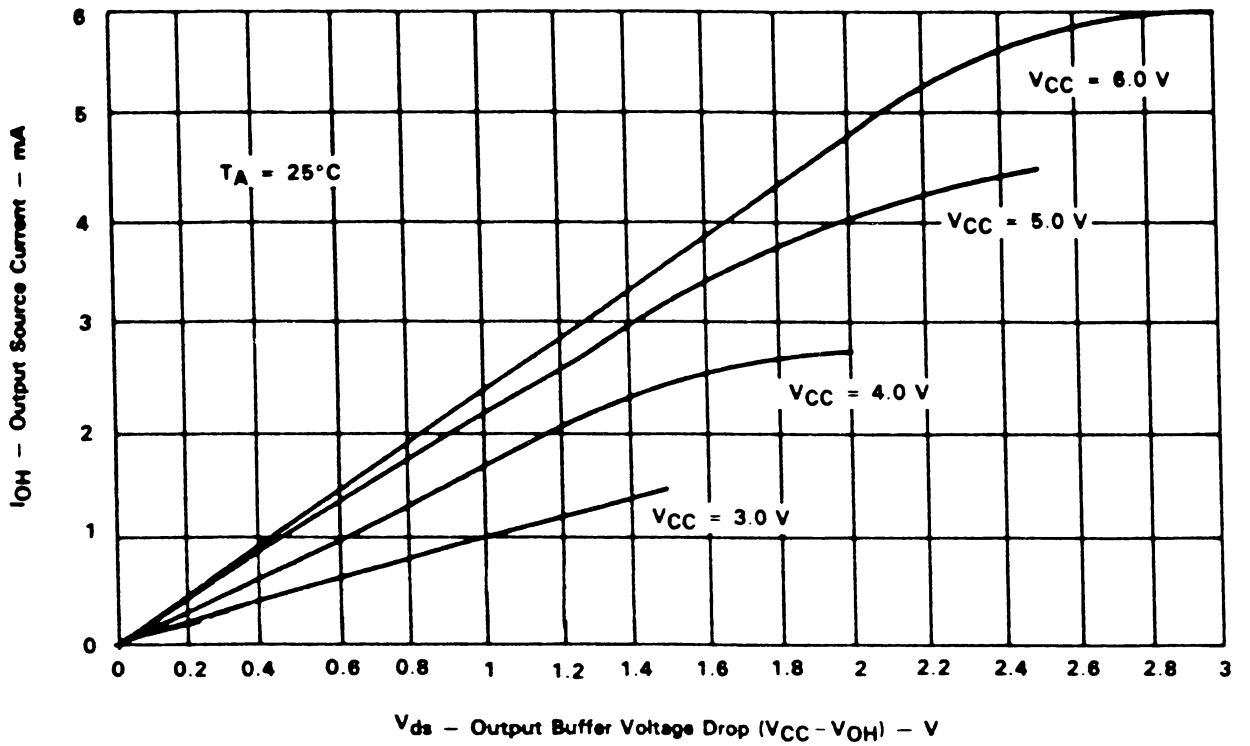


FIGURE 24. TYPICAL OUTPUT SOURCE CHARACTERISTICS

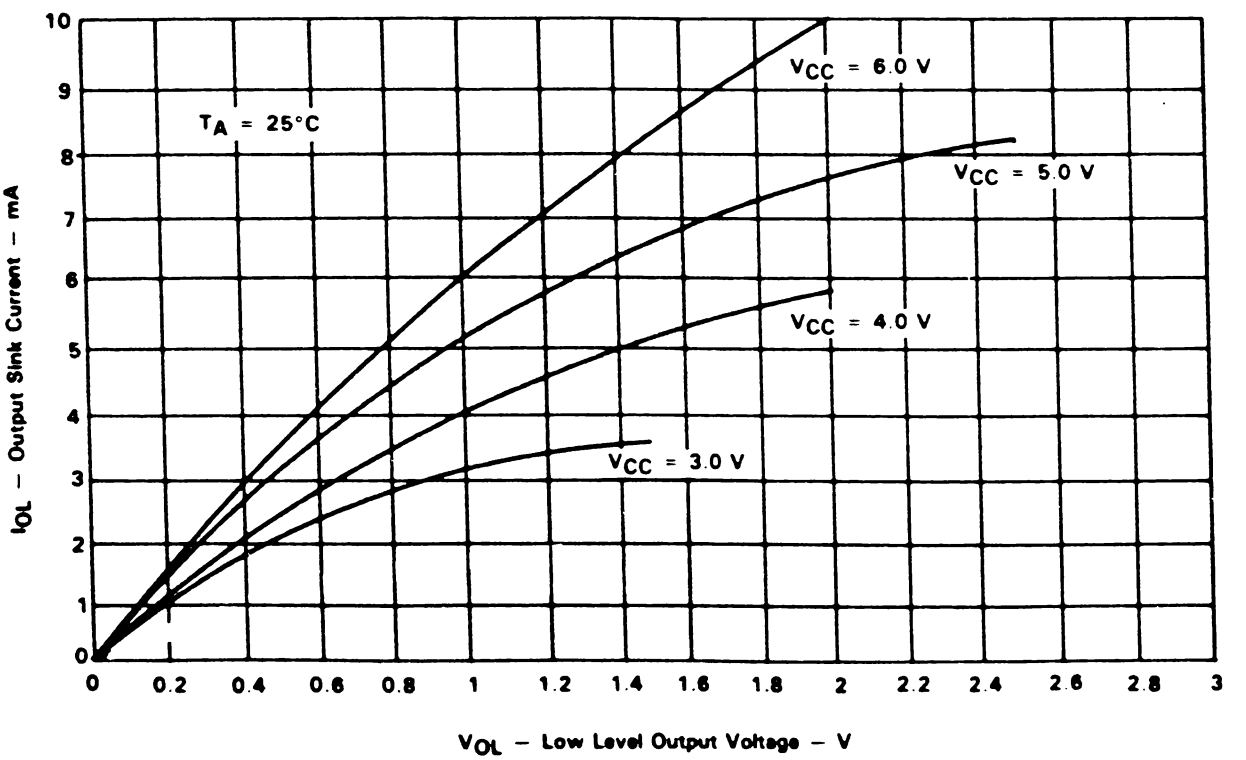


FIGURE 25. TYPICAL OUTPUT SINK CHARACTERISTICS

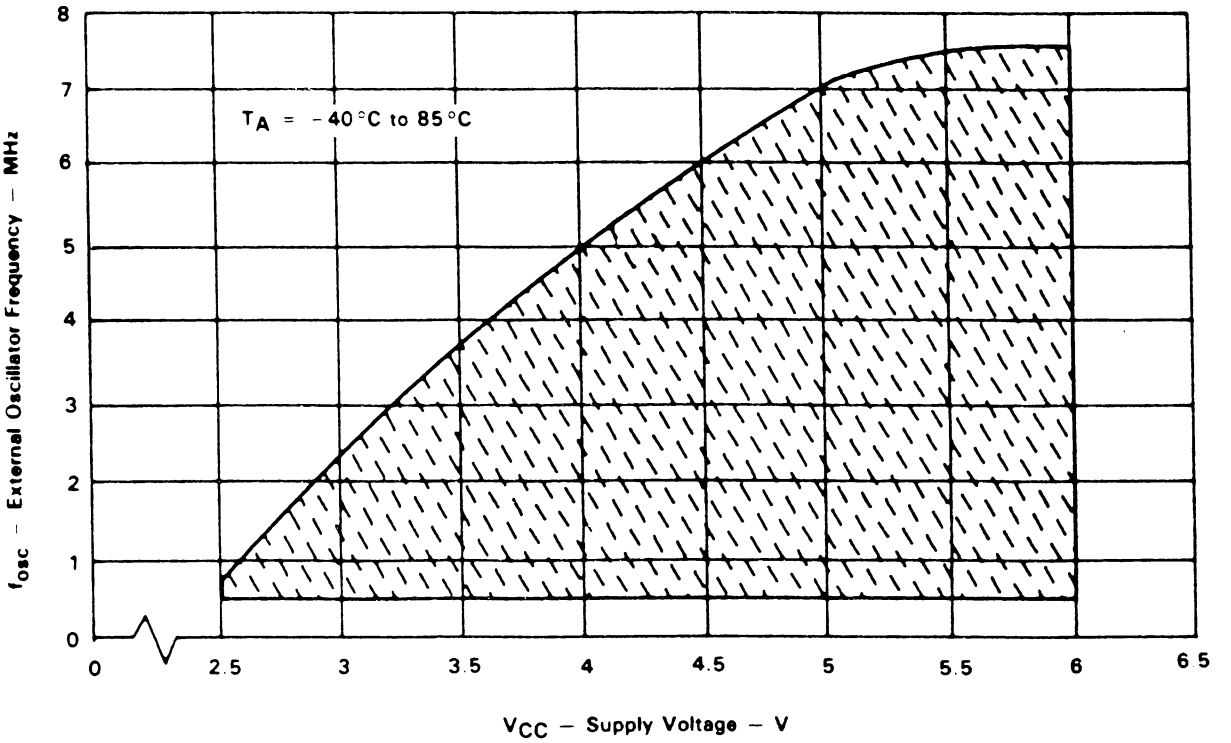


FIGURE 20. OPERATING FREQUENCY RANGE

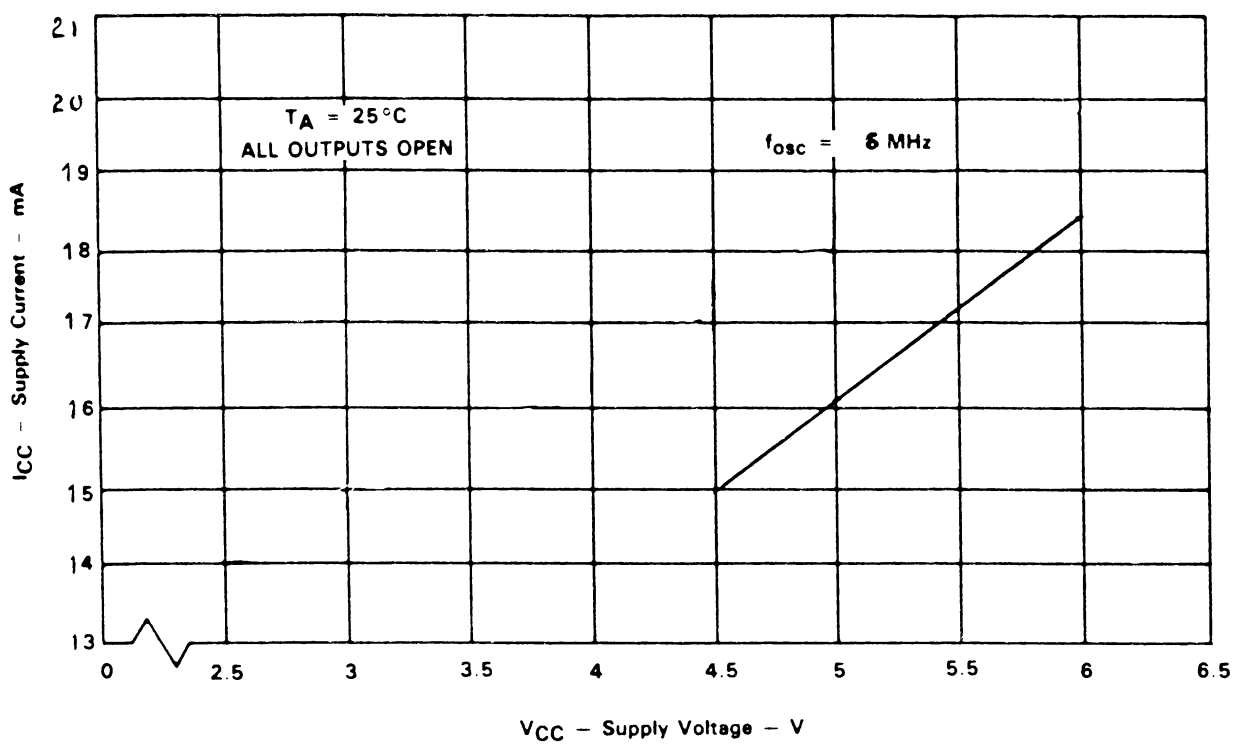


FIGURE 22. TYPICAL OPERATING CURRENT VS. SUPPLY VOLTAGE

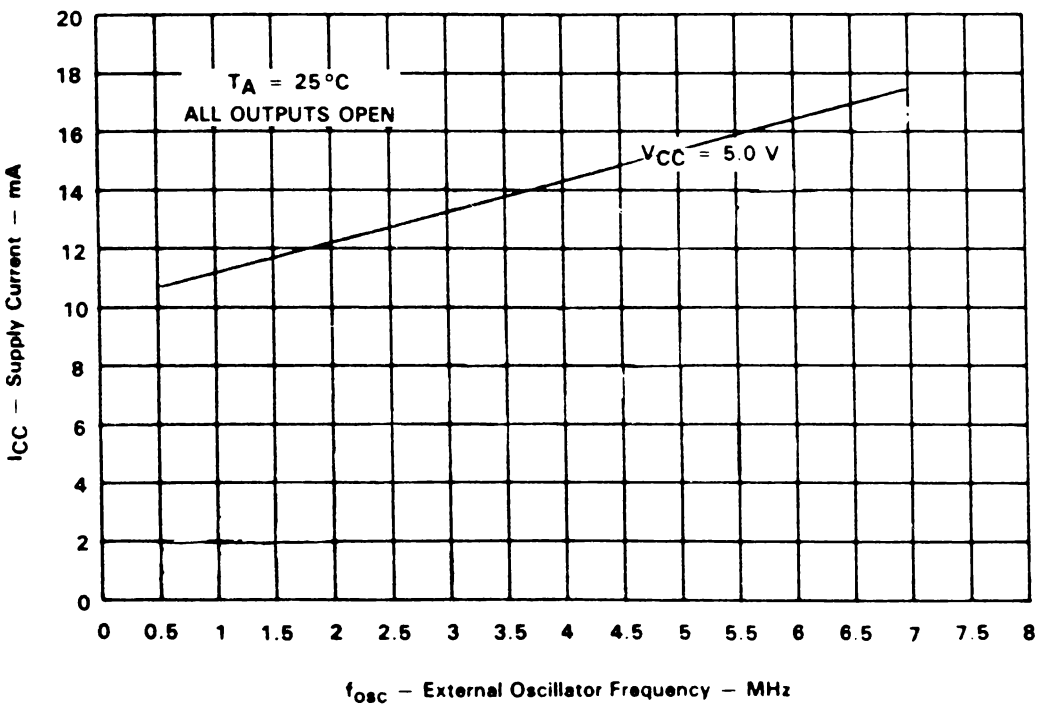


FIGURE 23. TYPICAL OPERATING I_{CC} VS. OSCILLATOR FREQUENCY

memory interface timing as a function of frequency

In the table below, $t_{c(C)}$ is the period of the internal clock, and $t_{c(C)} = 2/f_{osc}$. At 6 MHz $t_{c(C)}$ would be 333 ns. Minimum and maximum times may be calculated by using the formulas below with the appropriate clock period.

	PARAMETER	MIN	TYP	MAX	UNIT
$t_{c(C)}$	CLKOUT cycle time (see Note 7)	333		2000	ns
$t_{w(CH)}$	CLKOUT high pulse duration	$0.5t_{c(C)} - 50$	$0.5t_{c(C)}$	$0.5t_{c(C)} + 50$	ns
$t_{w(CL)}$	CLKOUT low pulse duration	$0.5t_{c(C)} - 50$	$0.5t_{c(C)}$	$0.5t_{c(C)} + 50$	ns
$t_{d(CH-JL)}$	Delay time, CLKOUT rise to ALATCH fall	$0.5t_{c(C)} - 50$	$0.5t_{c(C)}$		ns
$t_{d(CH-JH)}$	Delay time, CLKOUT rise to ALATCH rise	$0.25t_{c(C)} - 40$	$0.25t_{c(C)}$		ns
$t_{d(CH-HA)}$	Delay time, CLKOUT rise to high address valid	$0.25t_{c(C)} - 40$	$0.25t_{c(C)}$		ns
$t_{w(JH)}$	ALATCH high pulse duration	$0.25t_{c(C)} - 40$	$0.25t_{c(C)}$		ns
$t_{su(HA-JL)}$	Setup time, high address valid before ALATCH fall	$0.25t_{c(C)} - 40$	$0.25t_{c(C)}$		ns
$t_{su(LA-JL)}$	Setup time, low address valid before ALATCH fall	$0.25t_{c(C)} - 55$	$0.25t_{c(C)}$		ns
$t_{h(JL-LA)}$	Hold time, low address valid after ALATCH fall	$0.25t_{c(C)} - 50$	$0.25t_{c(C)}$		ns
$t_{su(RW-JL)}$	Setup time, R/$\overline{W}$ valid before ALATCH fall	$0.25t_{c(C)} - 60$	$0.25t_{c(C)}$		ns
$t_{h(EH-RW)}$	Hold time, R/$\overline{W}$ valid after $\overline{ENABLE}$ rise	$0.5t_{c(C)} - 60$	$0.5t_{c(C)}$		ns
$t_{h(EH-HA)}$	Hold time, high address valid after $\overline{ENABLE}$ rise	$0.5t_{c(C)} - 60$	$0.5t_{c(C)}$		ns
$t_{su(Q-EH)}$	Setup time, data output valid before $\overline{ENABLE}$ rise	$0.5t_{c(C)} - 35$	$0.5t_{c(C)}$		ns
$t_{h(EH-Q)}$	Hold time, data output valid after $\overline{ENABLE}$ rise	$0.5t_{c(C)} - 50$	$0.5t_{c(C)}$		ns
$t_{d(LA-EL)}$	Delay time, low address high impedance to $\overline{ENABLE}$ fall	$0.33t_{c(C)} - 35$	$0.25t_{c(C)}$		ns
$t_{d(EH-A)}$	Delay time, $\overline{ENABLE}$ rise to next address drive	$0.5t_{c(C)} - 60$	$0.5t_{c(C)}$		ns
$t_{a(EL-D)}$	Access time, data input valid after $\overline{ENABLE}$ fall	$0.75t_{c(C)} - 130$	$0.5t_{c(C)} - 20$		ns
$t_{a(A-D)}$	Access time, address valid to data input valid	$1.5t_{c(C)} - 175$	$1.5t_{c(C)} - 100$		ns
$t_{d(A-EH)}$	Delay time, address valid to $\overline{ENABLE}$ rise	$1.5t_{c(C)} - 50$	$1.5t_{c(C)}$		ns
$t_{h(EH-D)}$	Hold time, data input valid after $\overline{ENABLE}$ rise	0			ns
$t_{d(EH-JH)}$	Delay time, $\overline{ENABLE}$ rise to ALATCH rise	$0.5t_{c(C)} - 60$	$0.5t_{c(C)}$		ns
$t_{d(CH-EL)}$	Delay CLKOUT rise to $\overline{ENABLE}$ fall		30		ns

NOTE 7: $t_{c(C)}$ is defined to be $2/f_{osc}$ and may be referred to as a machine state or simply a state.

As an example, consider calculating the minimum data out hold time from $\overline{ENABLE}$ rising [$t_{h(EH-Q)}$]. At 6 MHz this would give:

$$t_{h(EH-Q)} = 0.5t_{c(C)} - 50 \text{ ns}$$
$$= 0.5(333 \text{ ns}) - 50 \text{ ns}$$
$$= 166.5 \text{ ns} - 50 \text{ ns}$$
$$\therefore t_{h(EH-Q)} = 116.5 \text{ ns}$$

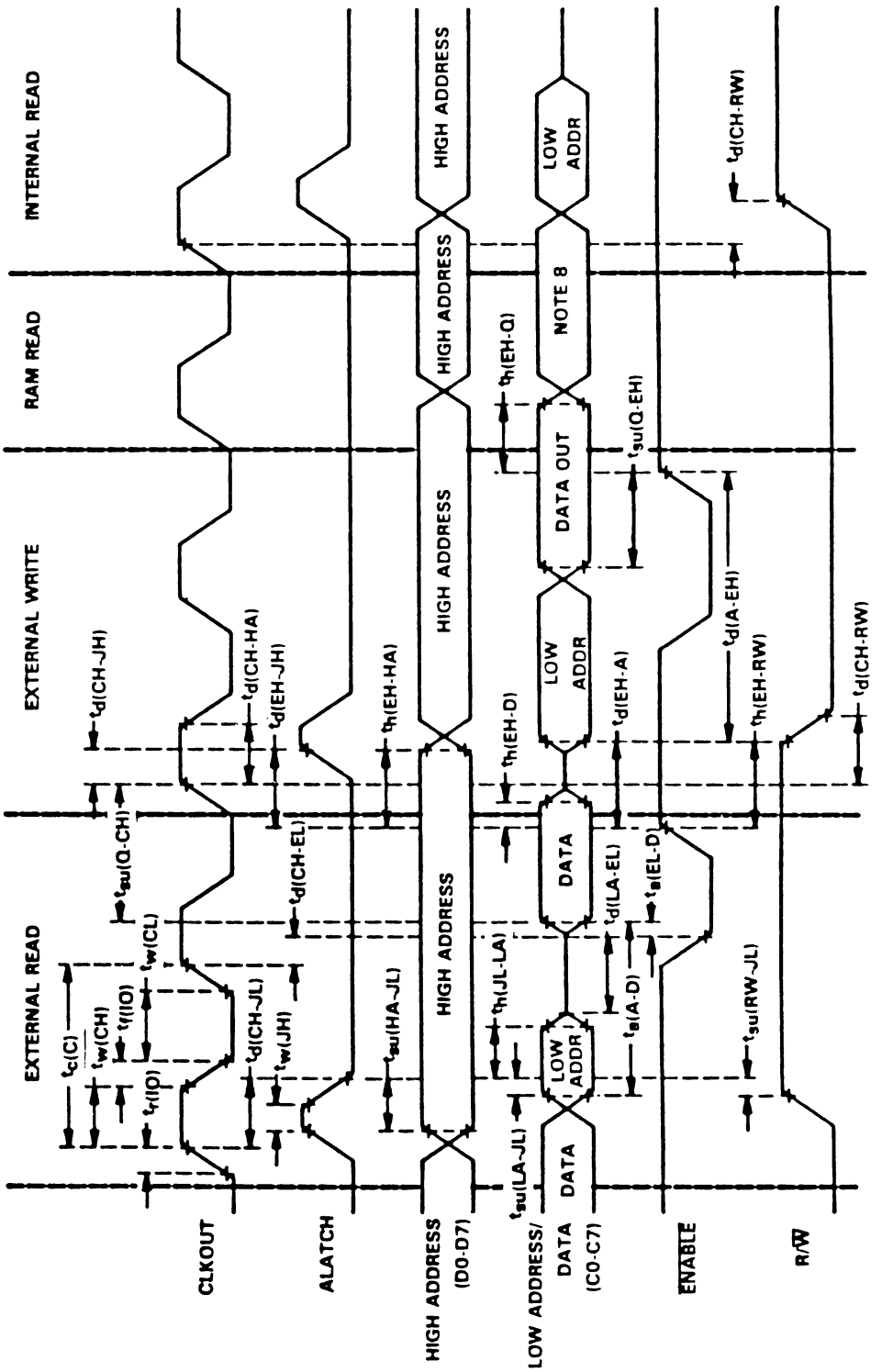
ADVANCE INFORMATION

memory interface timing at 6 MHz

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{c(C)}$	CLKOUT cycle time (see Note 7)	f = 6 MHz duty cycle = 50% V_{CC} = 4.5 V to 5.5 V	333		2000	ns
$t_{w(CH)}$	CLKOUT high pulse duration		116	166	216	ns
$t_{w(CL)}$	CLKOUT low pulse duration		116	166	216	ns
$t_{d(CH-JL)}$	Delay time, CLKOUT rise to ALATCH fall		116	166		ns
$t_{d(CH-JH)}$	Delay time, CLKOUT rise to ALATCH rise		43	83		ns
$t_{d(CH-HA)}$	Delay time, CLKOUT rise to high address valid		43	83		ns
$t_{w(JH)}$	ALATCH high pulse duration		43	83		ns
$t_{su(HA-JL)}$	Setup time, high address valid before ALATCH fall		43	83		ns
$t_{su(LA-JL)}$	Setup time, low address valid before ALATCH fall		28	83		ns
$t_{h(JL-LA)}$	Hold time, low address valid after ALATCH fall		33	83		ns
$t_{su(RW-JL)}$	Setup time, R/$\overline{W}$ valid before ALATCH fall		23	63		ns
$t_{h(EH-RW)}$	Hold time, R/$\overline{W}$ valid after $\overline{ENABLE}$ rise		106	166		ns
$t_{h(EH-HA)}$	Hold time, high address valid after $\overline{ENABLE}$ rise		106	166		ns
$t_{su(Q-EH)}$	Setup time, data output valid before $\overline{ENABLE}$ rise		131	166		ns
$t_{h(EH-Q)}$	Hold time, data output valid after $\overline{ENABLE}$ rise		116	166		ns
$t_{d(LA-EL)}$	Delay time, low address high impedance to $\overline{ENABLE}$ fall		75	83		ns
$t_{d(EH-A)}$	Delay time, $\overline{ENABLE}$ rise to next address drive		106	166		ns
$t_{a(EL-D)}$	Access time, data input valid after $\overline{ENABLE}$ fall		120	146		ns
$t_{a(A-D)}$	Access time, address valid to data input valid		325	400		ns
$t_{d(A-EH)}$	Delay time, address valid to $\overline{ENABLE}$ rise		450	500		ns
$t_{h(EH-D)}$	Hold time, data input valid after $\overline{ENABLE}$ rise		0			ns
$t_{d(EH-JH)}$	Delay time, $\overline{ENABLE}$ rise to ALATCH rise		106	166		ns
$t_{d(CH-EL)}$	Delay time, CLKOUT rise to ENABLE fall			30		ns

NOTE 7: $t_{c(C)}$ is defined to be $2/f_{osc}$ and may be referred to as a machine state or simply a state.

read and write cycle timing

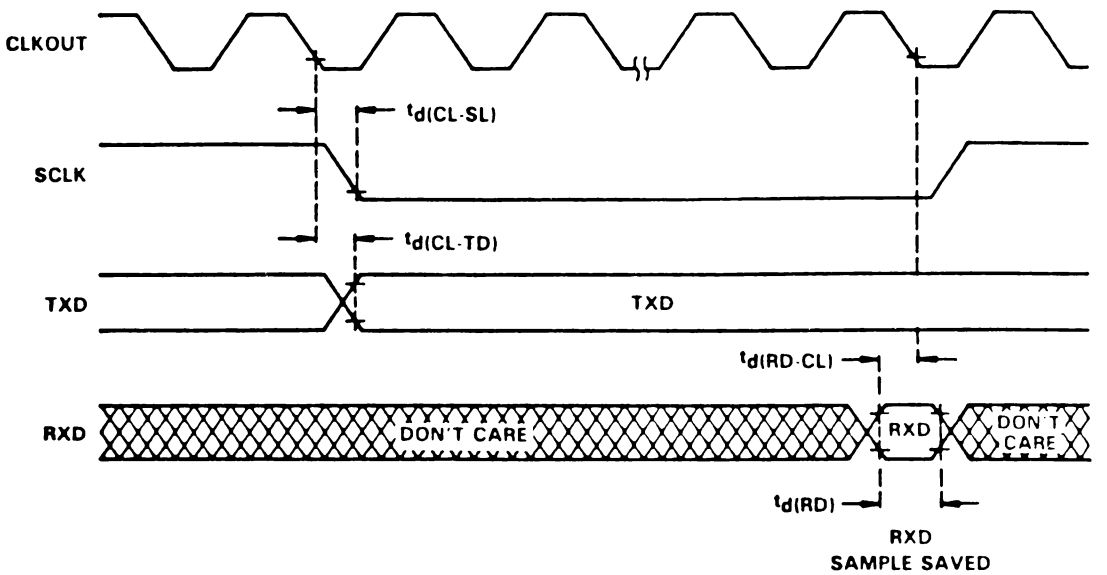


NOTE 8: During an internal RAM access, the CPORT outputs are stable but the data is a "don't care".

ADVANCE INFORMATION

serial port timing

internal serial clock

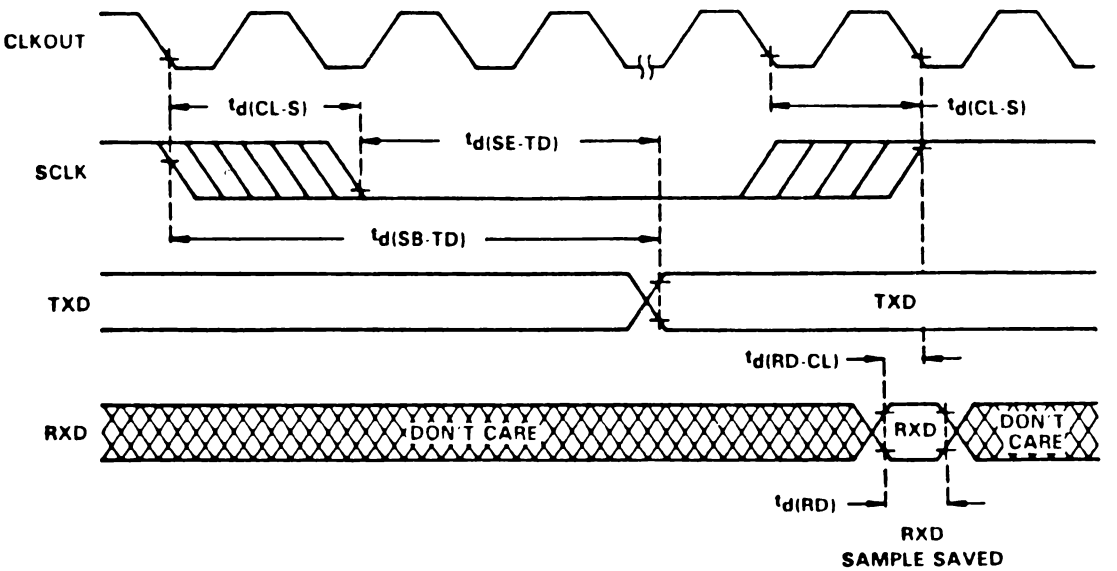


NOTES: 9. The CLKOUT signal is not available in Single-Chip mode.
10. CLKOUT = $t_{c(C)}$.

PARAMETER		TYP	UNIT
$t_{d(CL-SL)}$	CLKOUT low to SCLK low	1/4 $t_{c(C)}$	ns
$t_{d(CL-TD)}$	CLKOUT low to new TXD data	1/4 $t_{c(C)}$	ns
$t_{d(RD-CL)}$	RXD data valid before CLKOUT low	1/4 $t_{c(C)}$	ns
$t_{d(RD)}$	RXD data valid time	1/2 $t_{c(C)}$	ns

ADVANCE INFORMATION

external serial clock

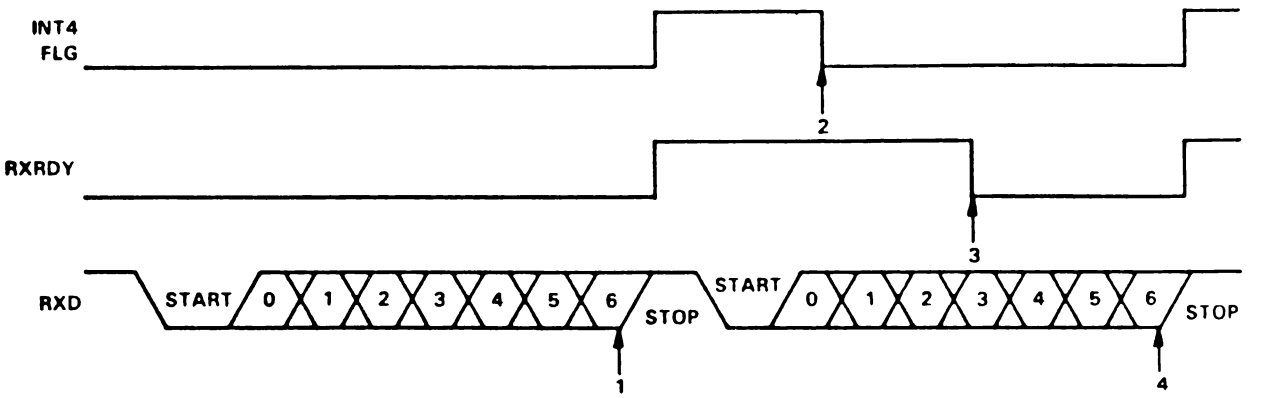


NOTES: 10. CLKOUT = $t_{c(C)}$.
11. The CLKOUT signal is not available in Single-Chip mode.
12. SCLK sampled; if SCLK = 1 then 0, fall transition found.
13. SCLK sampled; if SCLK = 0 then 1, rise transition found.

	PARAMETER	TYP	UNIT
$t_{d(RD-CL)}$	RXD data valid before CLKOUT low	1/4 $t_{c(C)}$	ns
$t_{d(RD)}$	RXD data valid time	1/2 $t_{c(C)}$	ns
$t_{d(SB-TD)}$	Start of SCLK sample to new TXD data	3 1/4 $t_{c(C)}$	ns
$t_{d(SE-TD)}$	End of SCLK sample to new TXD data	2 1/4 $t_{c(C)}$	ns
$t_{d(CL-S)}$	CLKOUT low to SCLK transition	$t_{c(C)}$	ns

ADVANCE INFORMATION

RX signals in communication modes

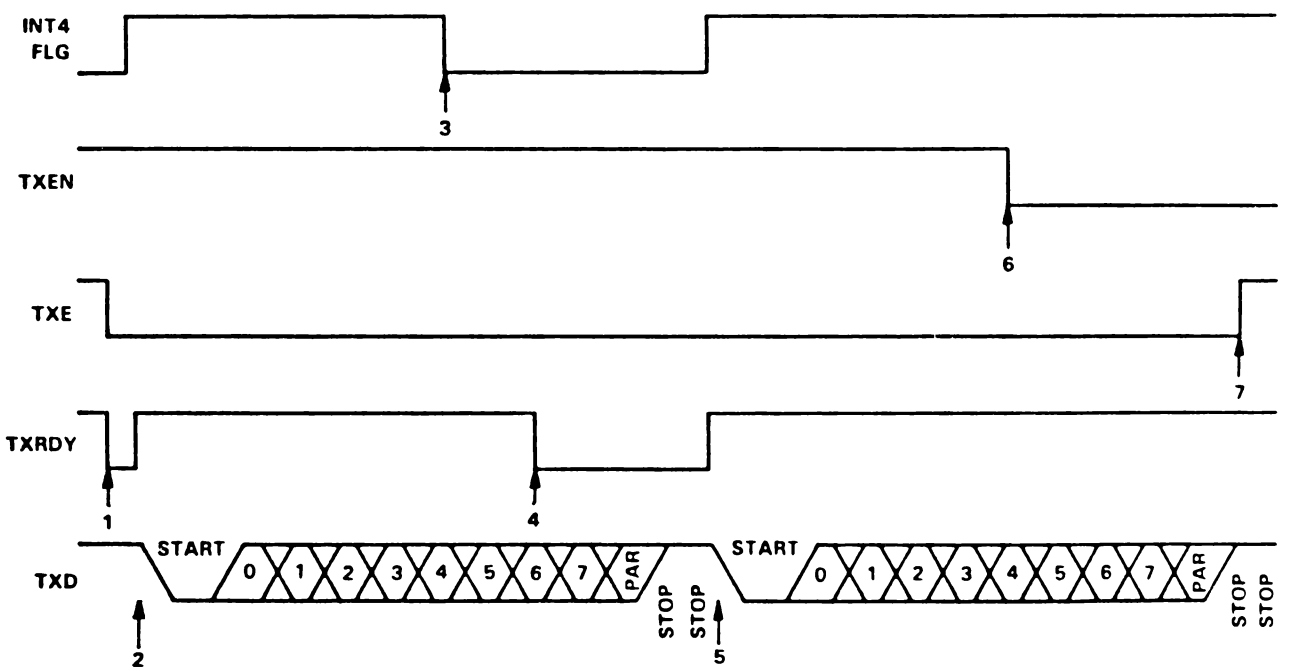


NOTES: 14. Format shown is start bit + seven data bits + stop bit.
15. SCLK is continuous, external or internal.
16. If RXEN = 0, RXSHF still receives data from RXD. However, the data is not transferred to RXBUF and RXRDY and INT4FLG are not set.

Sequence of Events:

1. RXSHF data is transferred to RXBUF. Error status bits are set if an error is detected.
2. Software writes to INT4CLR to clear INT4FLG; or, CPU clears INT4FLG on entry to level 4 interrupt routine.
3. Software reads RXBUF.
4. Repeat step 1.

TX signals in communication modes

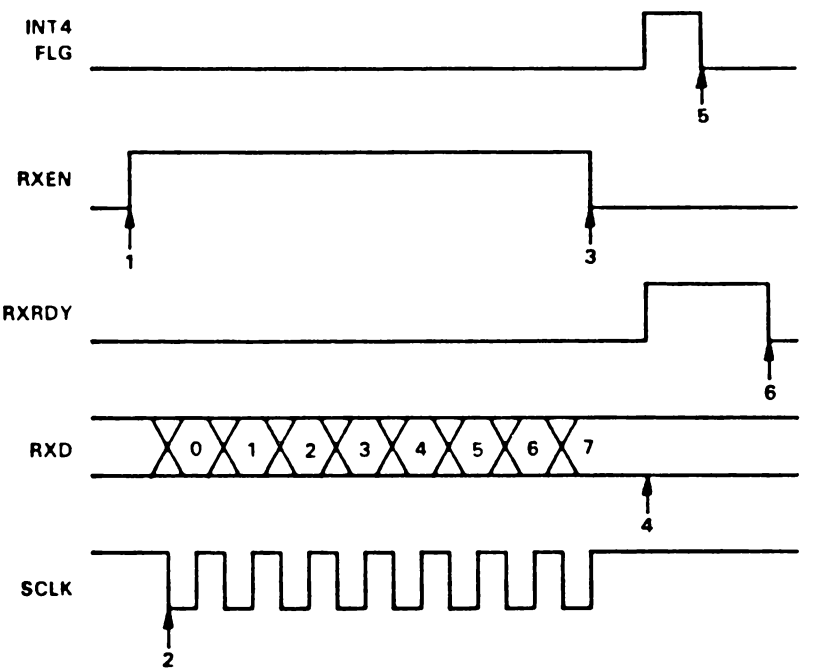


NOTES: 17. Format shown is start bit + eight data bits + parity bit + two stop bits.
18. SCLK is continuous whether internal or external.

Sequence of Events:

1. Software writes to TXBUF.
2. TXBUF and WU data are transferred to TXSHF and WUT (Wake-up temporary flag). INT4FLG and TXRDY are set.
3. Software writes to INT4CLR to clear INT4FLG or CPU clears INT4FLG on entry to level 4 interrupt routine.
4. Software writes to TXBUF.
5. TXBUF and WU data are transferred to TXSHF and WUT (Wake-up temporary flag). INT4FLG and TXRDY are set.
6. Software resets TXEN; current frame will finish and transmission will stop whether TXBUF is full or empty.
7. TXE is set if TXBUF and TXSHF are empty.

RX signals in serial I/O modes



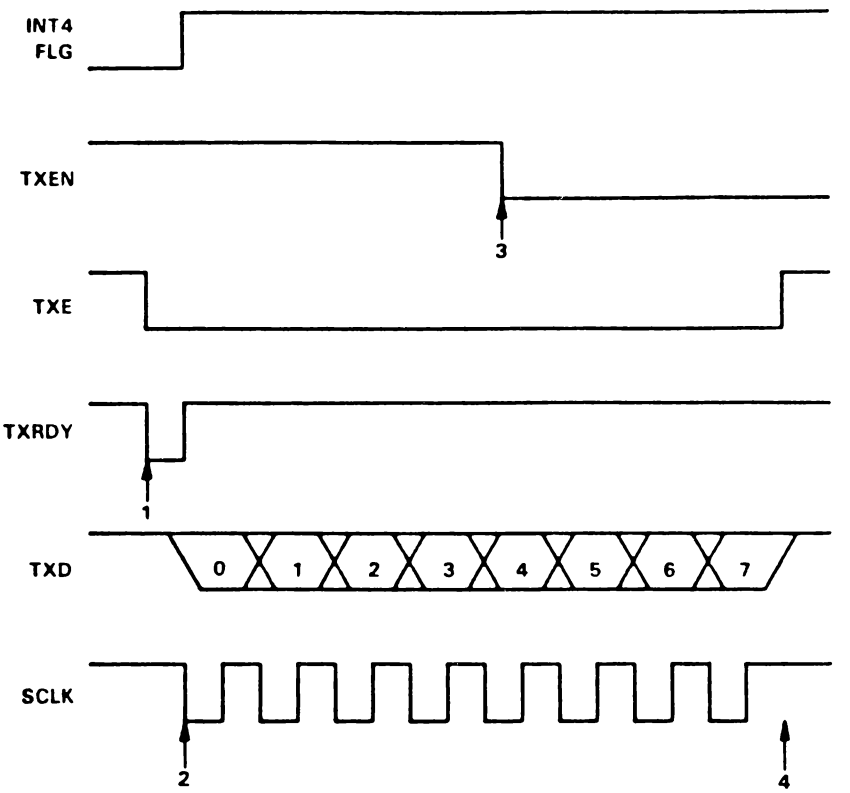
NOTES: 19. RXEN has no effect on INT4FLG or RXRDY in Serial I/O mode.
20. RXD is sampled on SCLK rise; external shift registers should be clocked on SCLK fall.

Sequence of Events

1. Software starts receiving by setting RXEN.
2. Gated SCLK starts and data is received.
3. RXEN is automatically cleared in last data bit.
4. RXSHF data is transferred to RXBUF, and RXRDY and INT4 are set.
5. Software writes to INT4CLR to clear INT4FLG; or, CPU clears INT4FLG on entry to level 4 interrupt routine.
6. Software reads RXBUF.

ADVANCE INFORMATION

TX signals in serial I/O modes



NOTE 21: Format shown is eight data bits.

Sequence of Events

1. Software writes to TXBUF.
2. TXBUF data is transferred to TXSFT; INT4FLG and TXRDY are set, and SCLK starts.
3. Software resets TXEN, current frame will finish and transmission will halt whether TXBUF is full or empty.
4. Frame ends and SCLK stops because TXEN = 0.

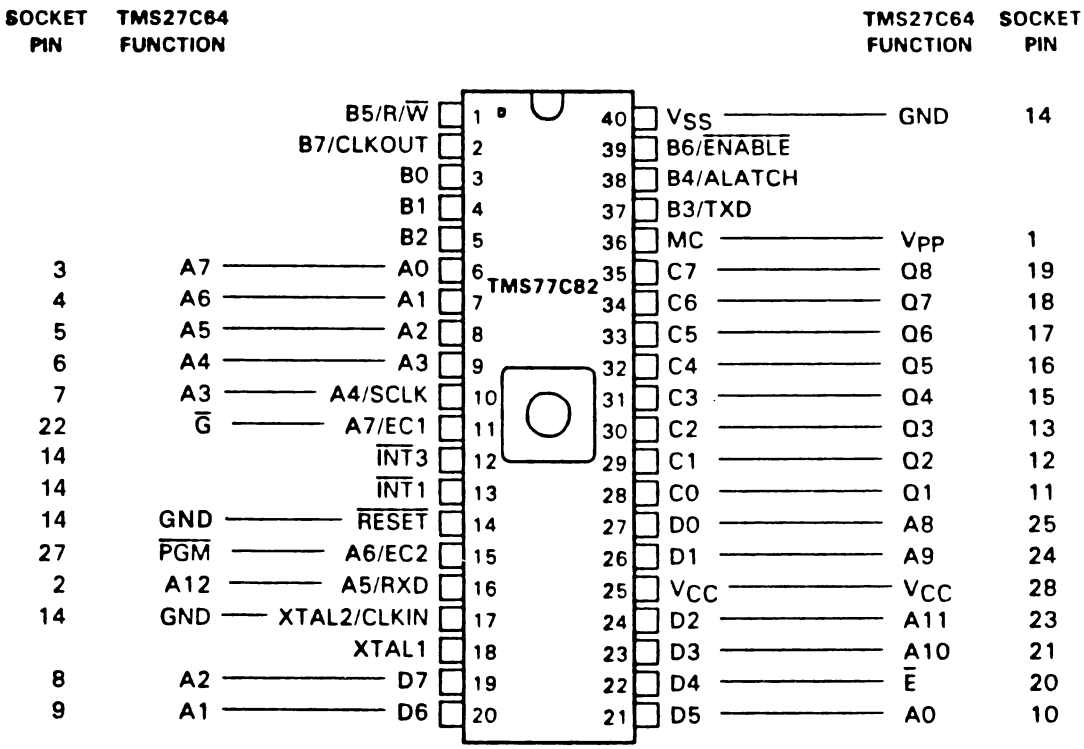
programming the TMS77C82 using a PROM programmer

The TMS77C82 can be programmed like any Texas Instruments TMS27C64 on a wide variety of PROM programmers. Programming the TMS77C82 requires a 40-to-28 pin adapter socket with the $\overline{\text{RESET}}$ and XTAL2 pins grounded. Contact your PROM programmer manufacturer or local TI field sales office for programming support.

adapter sockets

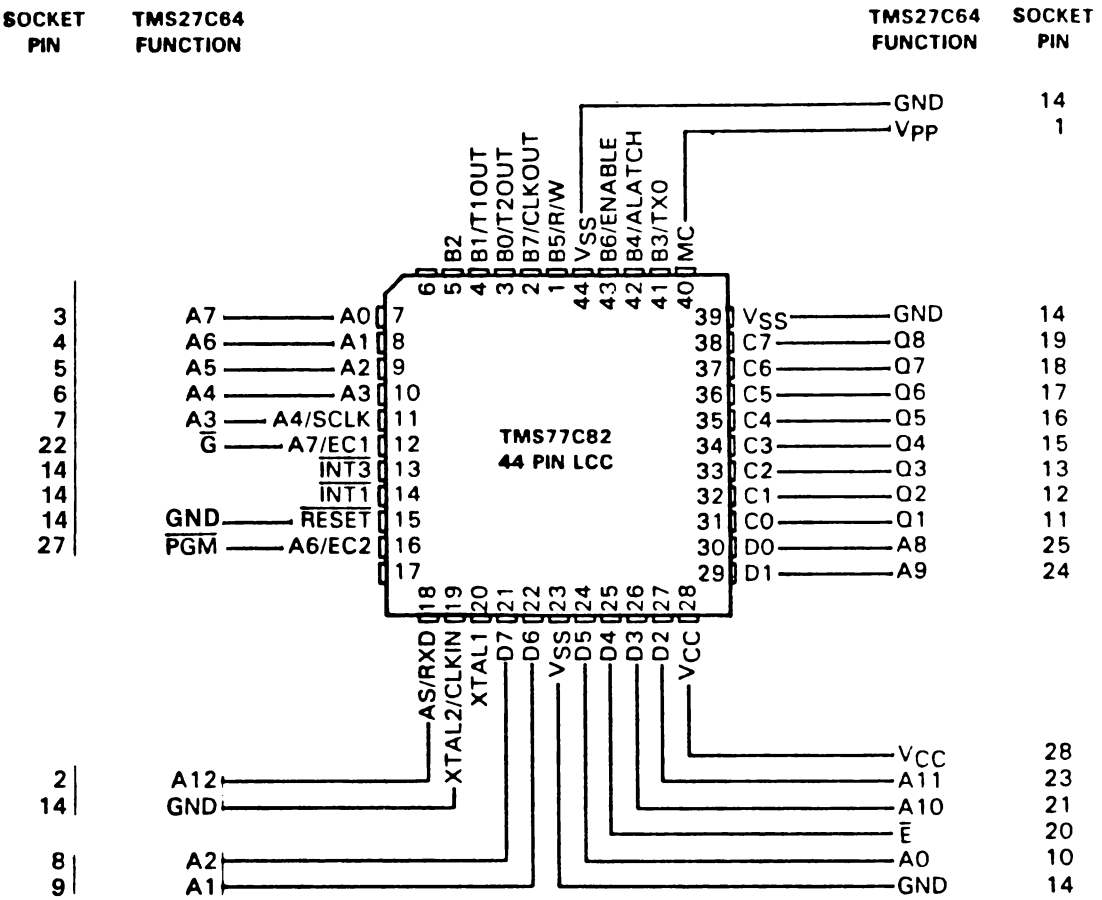
The following diagram shows the connections needed to be made on the 40-to-28 pin socket.

40-pin DIP to 28-pin socket



ADVANCE INFORMATION

44-pin PLCC to 44-pin socket



ADVANCE INFORMATION

EPROM Integrity protection using the R bit

Once the TMS77C82 has been programmed with the desired code, the contents of the EPROM may be protected with the use of the R bit integrity feature. The function of the R bit is to disable all external accesses to the on-chip EPROM while in the EPROM mode, which will prevent a protected code from being modified or read externally. The only way to "unprotect" the TMS77C82 after the R bit has been programmed is by erasing the EPROM, thereby destroying the protected code.

The following table and procedure demonstrates how to program and verify the R bit.

TMS77C82		R BIT	
FUNCTION	PIN #	PROGRAM	VERIFY
XTAL/CLKIN	17	V_{SS}	V_{SS}
$\overline{\text{RESET}}$	14	V_{SS}	V_{SS}
MC	36	12.5 V	V_{CC}
$\overline{\text{INT3}}$	12	12.5 V	12.5 V
D4	22	V_{CC}	V_{SS}
A7/EC1	11	V_{CC}	V_{SS}
A6/EC2	15	V_{CC}	V_{CC}
A3	9	V_{CC}	X
A1	7	X	V_{SS}
C7	35	$V_{IH}/V_{IL}/V_{IH}$	Refer to Step 3 in R Bit Verify Procedure

Note: X = Don't Care.

R bit Programming Procedure:

1. Configure all referenced pins for the R bit Program mode.
2. Power up the device.
3. Toggle C7 from a logical high (1), to a logical low (0), and back to a logical high (1).
4. Power down the device.

R bit Verify Procedure:

1. Configure all referenced pins for the R bit Verify mode.
2. Power up the device.
3. Read C7. Zero (0) is programmed, one (1) is not programmed.
4. Power down the device.

erasure

The TMS77C82 is erased by exposing the chip to shortwave ultraviolet light that has a wavelength of 253.7 nanometers (2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is 15 watt-seconds-per-square-centimeter. The lamp should be located about 2.5 centimeters (1 inch) above the chip during erasure. After erasure, all bits are at a high level. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS77C82 the window should be covered with an opaque label.

programming characteristics over recommended supply voltage range and operating free-air temperature range T_A = 25°C, V_{CC} = 6 V, V_{PP} = 12.5 V

PARAMETER		TEST CONDITIONS†	MIN	MAX	UNIT
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, $t_r \leq 20$ ns, $t_f \leq 20$ ns		450	ns
$t_{a(E)}$	Access time from chip enable			450	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns
t_{dis}‡	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first		0	130	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$ whichever occurs first		0		ns

†For all switching characteristics and timing measurements, input pulse levels are 0.40 V to 2.4 V and V_{PP} = 12.5 ± 0.5 V during programming.

‡Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

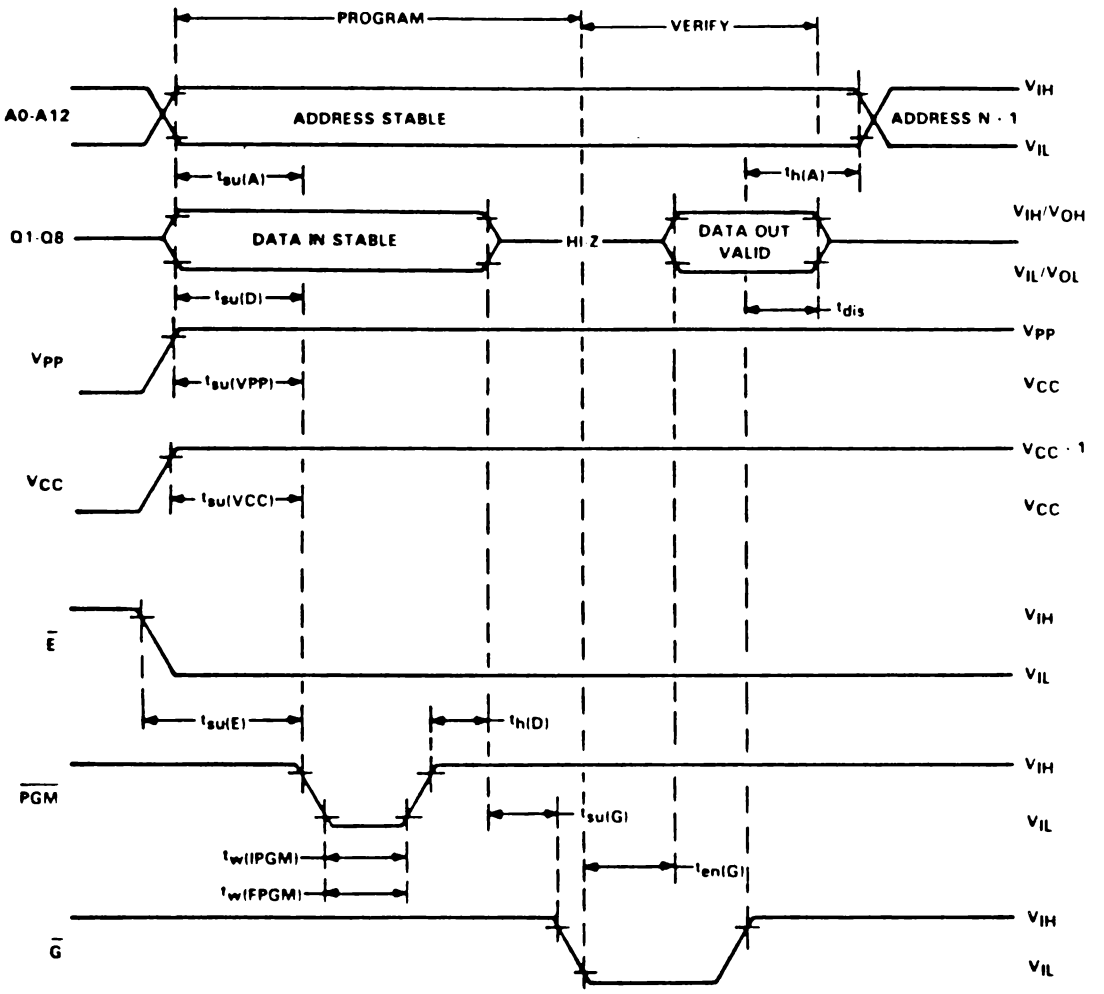
recommended conditions for programming, T_A = 25°C§

		MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	0.95	1	1.05	ms
$t_{w(FPGM)}$	Final pulse duration	2.85		78.75	ms
$t_{su(A)}$	Address setup time	2			μs
$t_{su(E)}$	$\overline{E}$ setup time	2			μs
$t_{su(G)}$	$\overline{G}$ setup time	2			μs
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	V_{PP} setup time	2			μs
$t_{su(VCC)}$	V_{CC} setup time	2			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	2			μs

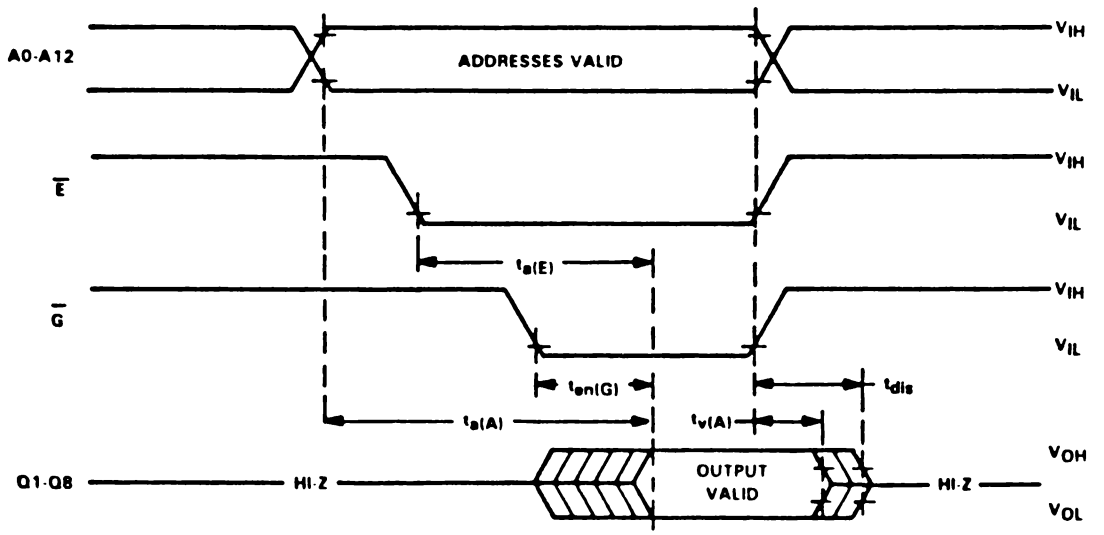
§Common test conditions apply for $t_{dis(G)}$ except during programming.

ADVANCE INFORMATION

program cycle timing



read cycle timing

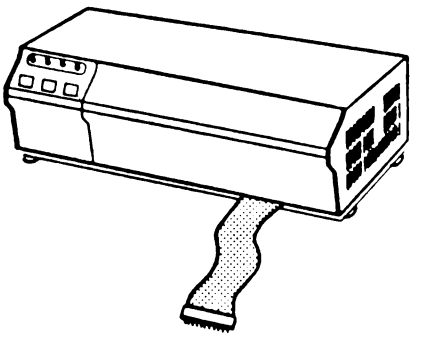


NOTE: The timing measurement reference levels for inputs and outputs are 0.8 V and 2 V.

ADVANCE INFORMATION

TMS77C82 DEVELOPMENT SUPPORT

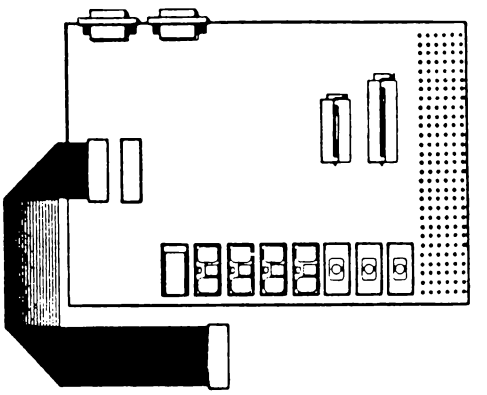
TMS7000 CMOS XDS† — extended development system



- Full TMS7000 Family Development System
- Host Independent/RS-232-C Interface
- Full Speed In-Circuit Emulation
- Extensive Breakpoint and Trace Functions
  - —Detailed Timing Analysis
  - —2K-Byte Trace Samples
  - —Breakpoint Sequencing Ability
- Command/Default Storage
- Removable Target Connector
- External Probe for Breakpoint/ Trace Qualifiers
- On-Board Assembler and reverse Assembler
- Multiprocessing Capabilities

CMOS EVM — evaluation module RTC/EVM7000C-1

- TMS7000 Family Low Cost Development System
- Single-Chip Mode Emulation Only
- On-Board Assembler/Line Text Editor
- Multiple Breakpoints
- Trace Display Function
- EPROM Programmer Utilities



assembler/linker packages

Crossware† assembler/linker packages are available through Texas Instruments for the following operating systems:

Operating System	TI Part Number
MS†-DOS and PC-DOS	TMDS7040810-02
DEC VAX† VMS	TMDS7040210-08

†XDS and Crossware are registered trademarks of Texas Instruments Incorporated. MS is a trademark of Microsoft, Inc. VAX is a trademark of Digital Equipment Corporation.

EPROM programming support

The following third-party companies support programming the TMS77C82 EPROM microcontroller directly or with an adapter socket (see note 24).

- Data I/O Corporation

  10525 Willows Road N.E.
  P.O. Box 97046
  Redmond, WA 98073-9746
  (206) 881-6444

- PROMAC

  Adams MacDonald Enterprises, Inc.
  2999 Monterey/Salinas Highway
  Monterey, CA 93940
  (408) 373-3607

- Advanced Microcomputer System Inc.

  2780 S.W. 14th Street
  Pompano Beach, Fl 33069
  (305) 975-9515

- Logical Devices, Inc.

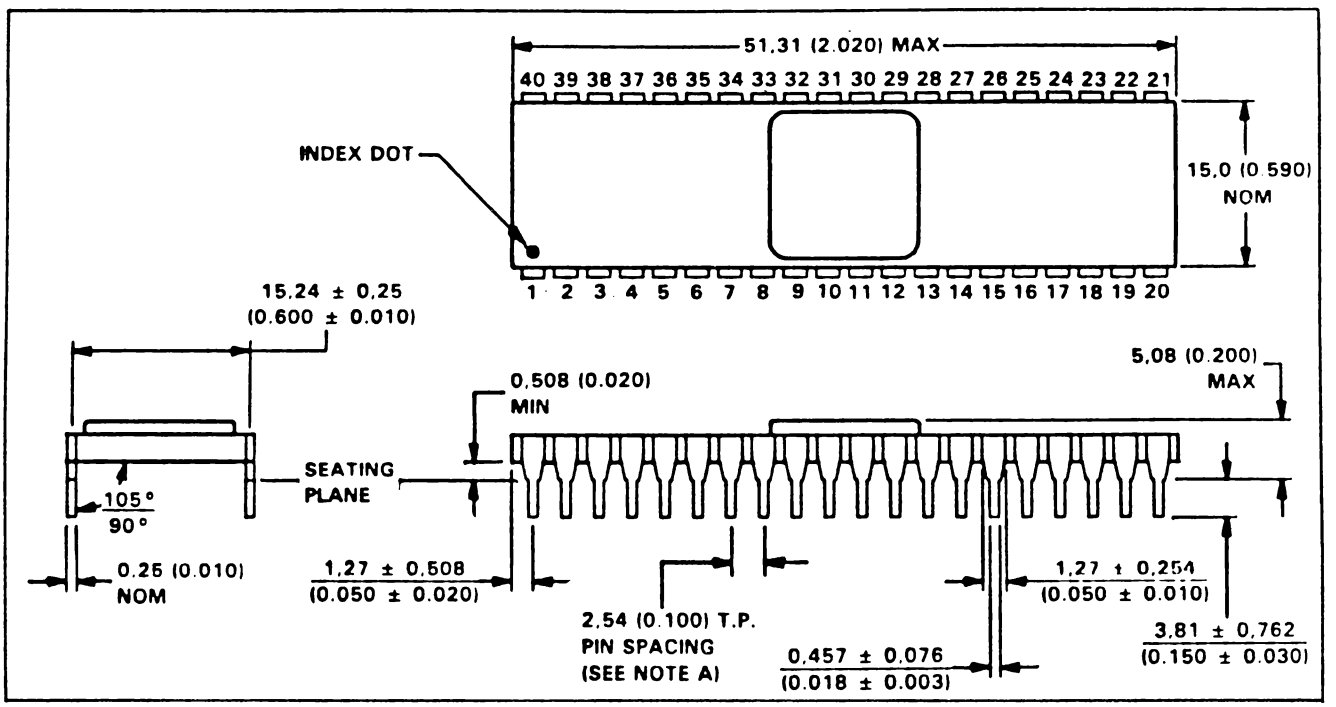
  1321-E N.W. 65th Place
  Fort Lauderdale, FL 33309

NOTE: Contact your local Texas Instruments field sales office for availability of the 40-to-28 pin programmer adapter socket (part no. RTC/PGMC82A-06).

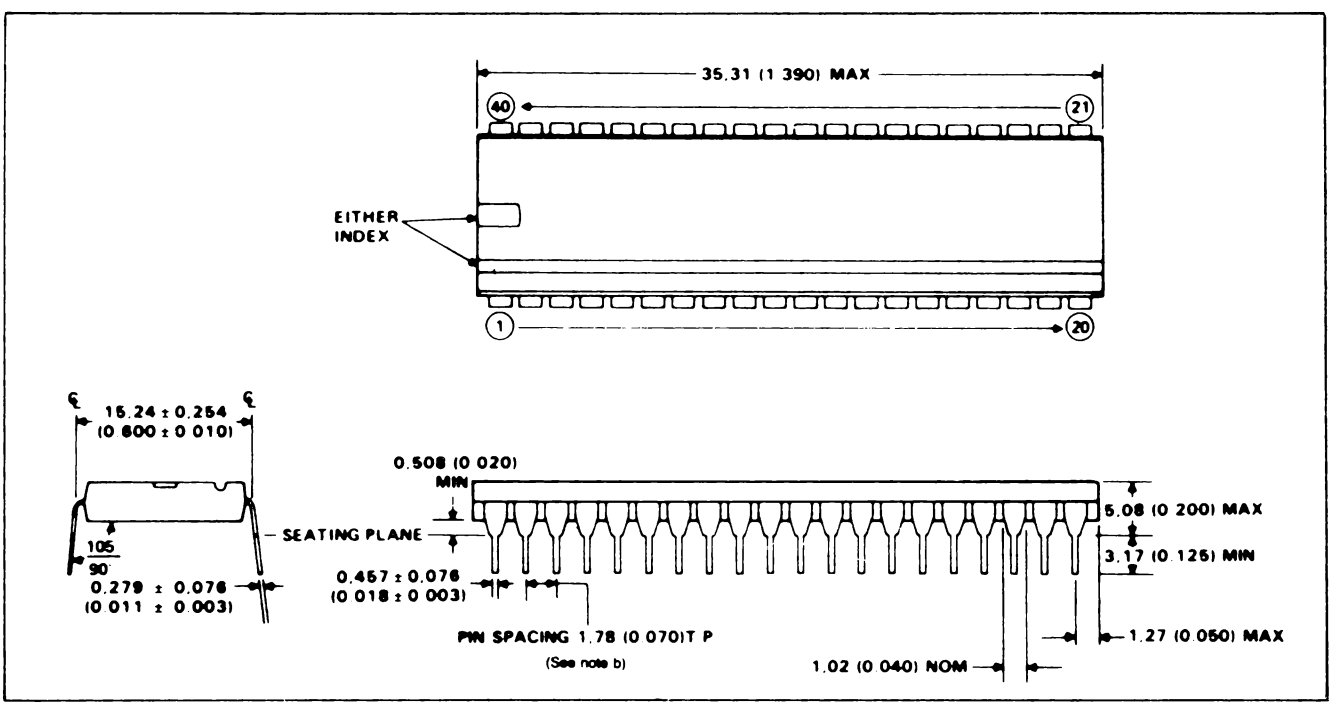
ADVANCE INFORMATION

MECHANICAL DATA

40-pin JD ceramic sidebraze package



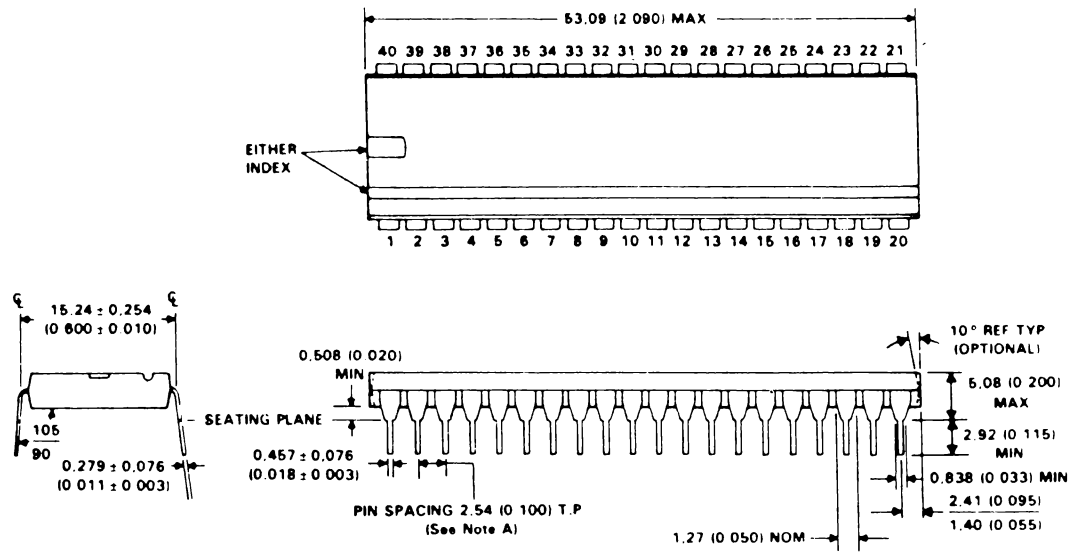
40-pin plastic package (70 mil spacing)



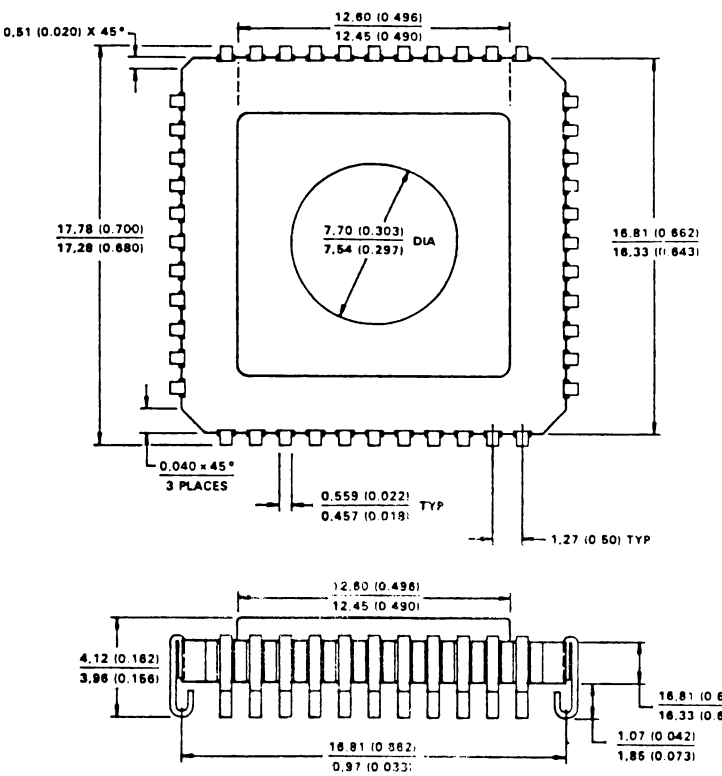
Note: All dimensions are in millimeters and parenthetically in inches.

MECHANICAL DATA

40-pin N dual-in-line package



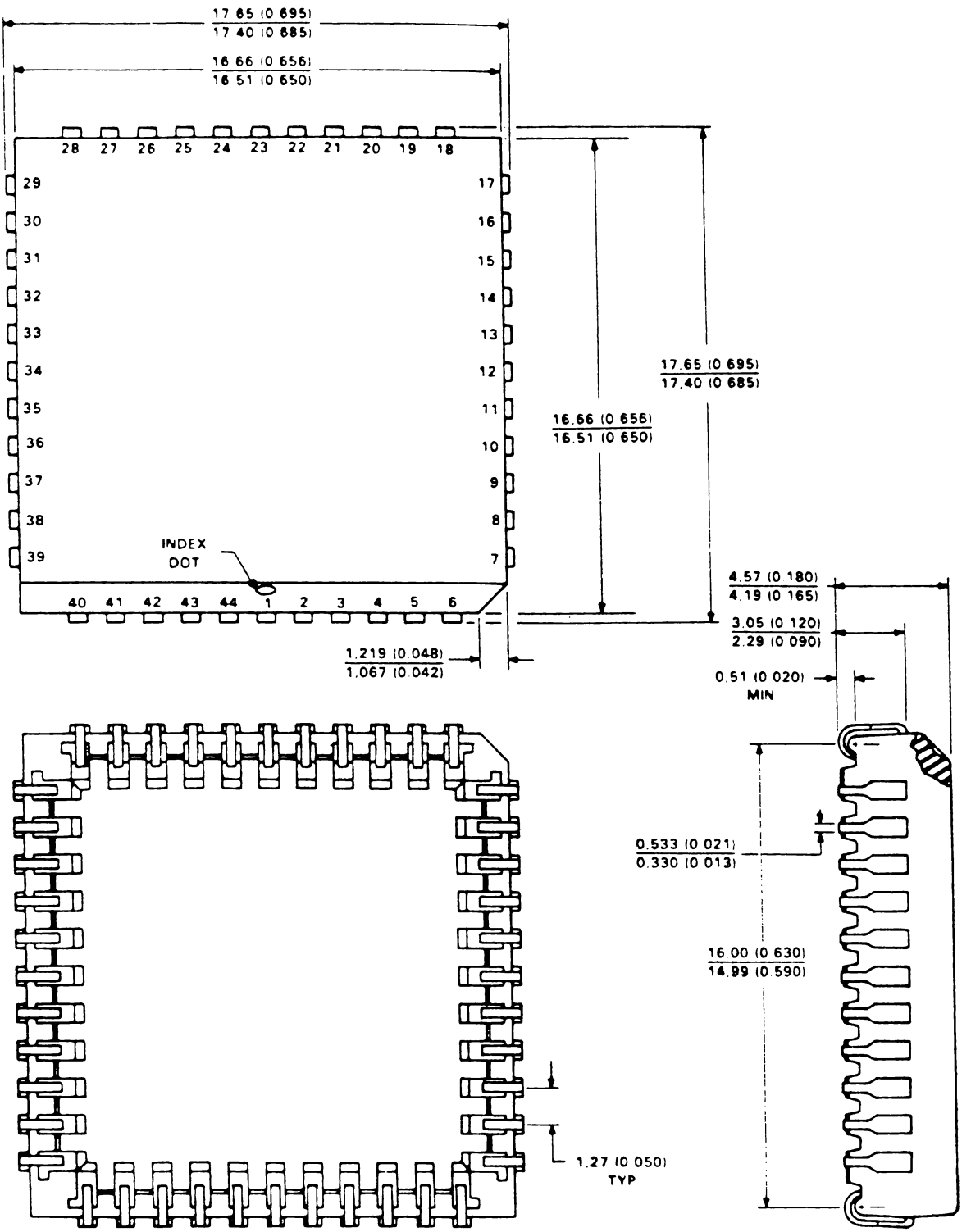
44-pin leaded chip carrier with window



Note: All dimensions are in millimeters and parenthetically in Inches.

MECHANICAL DATA

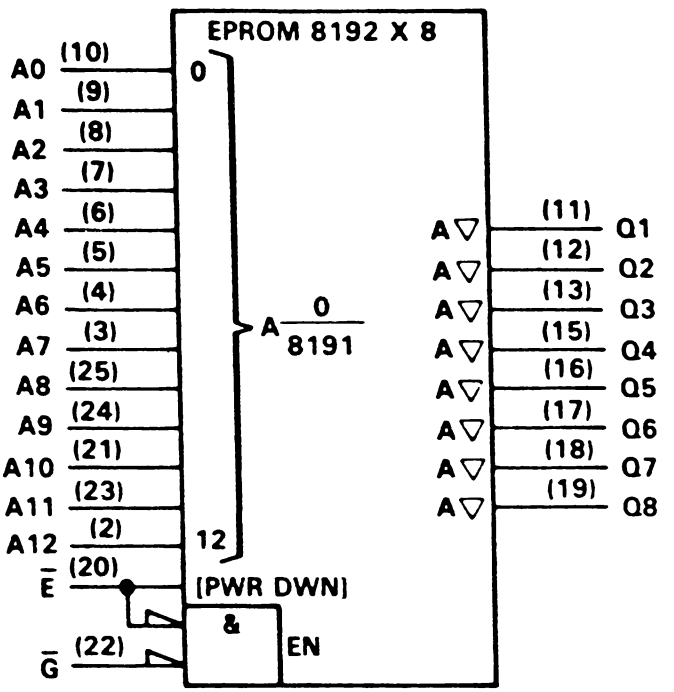
44-lead plastic chip carrier package



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

TEXAS INSTRUMENTS

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	−0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1)	−0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9	−0.6 V to 6.5 V
A9	−0.6 V to 13.5 V
Output voltage range (see Note 1)	−0.6 V to V_{CC} + 1 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

recommended operating conditions

			TMS27C64-1, TMS27C64-2, TMS27C64, TMS27C64-3, TMS27C64-4			TMS27C64-15, TMS27C64-20, TMS27C64-25, TMS27C64-30, TMS27C64-45			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		4.75	5	5.25	4.5	5	5.5	V
V_{PP}	Supply voltage (see Note 3)			V_{CC}			V_{CC}		V
V_{IH}	High-level input voltage	TTL	2		$V_{CC}+1$	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+0.2$	$V_{CC}-0.2$		$V_{CC}+0.2$	V
V_{IL}	Low-level input voltage	TTL	−0.5		0.8	−0.5		0.8	V
		CMOS	GND−0.2		GND+0.2	GND−0.2		GND+0.2	V
T_A	Operating free-air temperature		0		70	0		70	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC}+I_{PP}$. During programming, V_{PP} must be maintained at 12.5 V (±0.5 V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −400 µA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
I_I	Input current (leakage)		V_I = 0 V to 5.5 V			±10	µA
I_O	Output current (leakage)		V_O = 0 V to V_{CC}			±10	µA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V			100	µA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 13 V		30	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}			500	µA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}			250	µA
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, t_{cycle} = minimum cycle time, outputs open		30	40	mA

†Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	V_I = 0 V, f = 1 MHz		6	9	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz		8	12	pF

†Capacitance measurements are made on sample basis only.
‡Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Note 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C64-1 '27C64-15		'27C64-2 '27C64-20		'27C64 '27C64-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns		150		200		250	ns
$t_{a(E)}$	Access time from chip enable			150		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C64-3 '27C64-30		'27C64-4 '27C64-45		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns		300		450	ns
$t_{a(E)}$	Access time from chip enable			300		450	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			120		150	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	105	0	130	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		ns

†Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

recommended timing requirements for programming, T_A = 25°C, V_{CC} = 6 V, V_{PP} = 12.5 V (see Note 4)

		MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	0.95	1	1.05	ms
$t_{w(FPGM)}$	Final pulse duration	2.85		78.75	ms
$t_{su(A)}$	Address setup time	2			μs
$t_{su(E)}$	$\overline{E}$ setup time	2			μs
$t_{su(G)}$	$\overline{G}$ setup time	2			μs
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	V_{PP} setup time	2			μs
$t_{su(VCC)}$	V_{CC} setup time	2			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	2			μs

NOTES: 4. For all switching characteristics and timing measurements, input pulse levels are 0.40 V to 2.4 V and V_{PP} = 12.5 V ± 0.5 V during programming.

5. Common test conditions apply for $t_{dis(G)}$ except during programming.

TI Sales Offices

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