TMS7000 FAMILY

TMS77C01 (PIT) USER'S MANUAL

JUNE 1984
AUG 20 1984 REVISION A

TEXAS

INSTRUMENTS

ERRATA SHEET OF TMS77C01 USER'S MANUAL

8/20/'84

MAKE THE FOLLOWING CHANGES FOR TMS77C01 USER'S MANUAL

ITEM	PAGE	CONTENTS
1.	14	REPLACE ALL PAGE WITH THE ATTACHMENT SHEET.
2.	15	"
3.	18	REPLACE LAST 2 LINES WITH THE FOLLOWING: "WHEN A '0' IS WRITTEN IN, THE COUNT DOWN IS STOPPED AFTER THE TIMER INITIAL LATCH VALUE IS LOADED INTO THE 16 BIT DECREMENTER".
4.	24	DELETE ",WHEN THE SYSTEM CLOCK (INTERNAL CLOCK) IS USED," OF 9.2.1.(1): AND INSERT THE SENTENCE "OR EXTERNAL SIGNAL PERIOD (SECOND)" IMMEDIATELY BEFORE "TL: TIMER LATCH VALUE (16 BITS)".

NOTE: AS TO ITEM 1 AND 2, ONLY THE TIMING OF PULSED CXOUT /CYOUT IS CHANGED.

IF YOU HAVE ANY QUESTION, PLS CONTACT ME.

HAJIME KARASAWA 8/20/'84 JAPL

Page

1. Outline

TMS77C01 is a Parallel Interface & Timer (PIT) of the TMS7000 family, designed to enable direct INTERFACE to TMS7000 FAMILY CPU.

PIT is provided with 3 sets of bi-directional peripheral buses and 2 sets of 16 bit timers. Of the 3 sets of bi-dreictional peripheral buses, 2 sets possess handshake (or H/S) functions and can be interfaced with most peripheral devices.

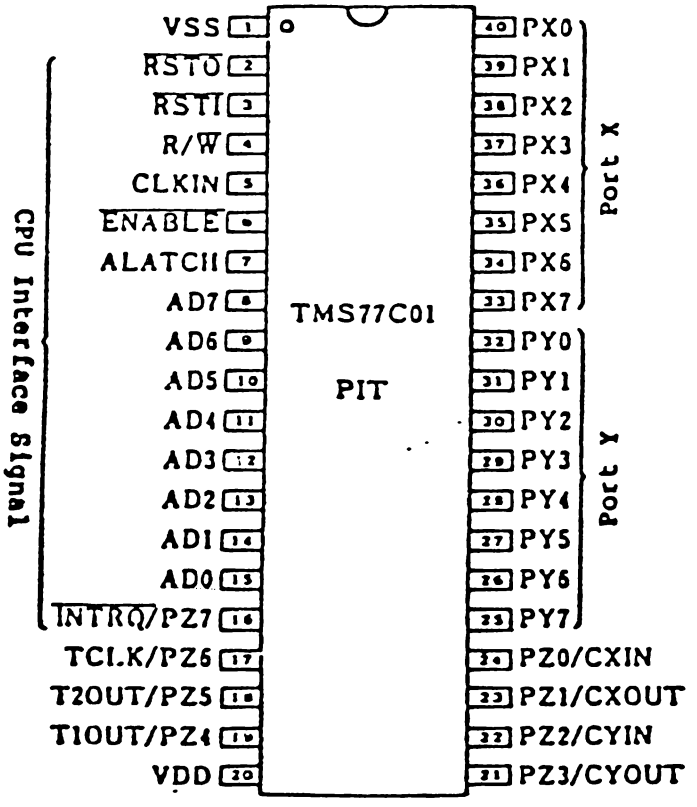
Daisy Chain Enables Max. 15 pcs of TMS77C01 to Interface with TMS7000 CPU directly using Address Mapping Register.

2. Features

- o Direct Interface possible to the TMS7000 family CPU (7040/7041/70C20/70C40/70P161)
- o 3 sets of bidirectional peripheral ports (2 sets with handshake functions)
- o Easily expandable to MAX. 15 pcs of TMS77C01 using Address Mapping register and Daisy Chain.
- o 2 sets of built-in 16 bit timers (1 set with capture latch)
- o Software controlled interrupt
- o Capable of driving 1 standard TTL

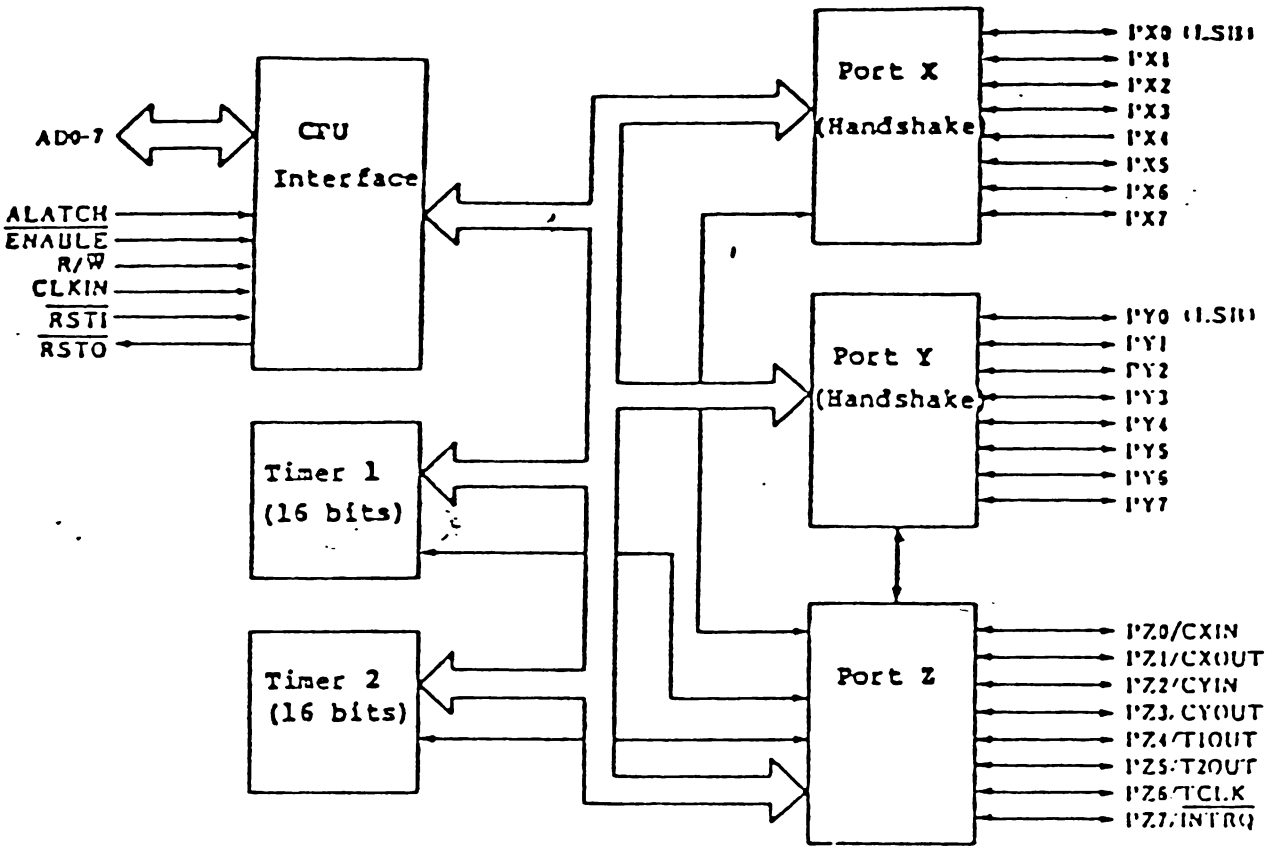
- o CMOS B series compatible peripheral line
- o 40 pin shrink package
- o I/O Port, Timer, Control Register on PIT are operable through TMS7000 peripheral instructions and memory addressing instructions (MOVP, ANDP, ORP, XORP, BTJOP, BTJZP, LDA, STA).

3. Pin Assignment



PZ0–PZ7 : Port Z
PZ0 : LSB
INTRQ : Interrupt output
TCLK : External clock input for timer
T2OUT : T2 output
T1OUT : T1 output
CYOUT, CYIN : PY H/S control line for H/S
CXOUT, CXIN : PX H/S control line for H/S

4. TMS77C01 Block Diagram



5. PIT CPUT Interface

- o CLKIN (IN) — CLKOUT signal (or similar signal) from 7000CPU may be connected for Timer and Handshake control
- o $\overline{\text{ENABLE}}$ (IN) — $\overline{\text{ENABLE}}$ signal from 7000CPU may be connected for strobe timing of data
- o R/$\overline{\text{W}}$ (IN) — R/$\overline{\text{W}}$ signal from 7000CPU may be connected to select READ/WRITE of accessed data.

- o ALATCH (IN) — ALATCH signal from 7000CPU may be connected for the Internal Address Latch Timing.

- o AD_{0-7} (INOUT) — Bidirectional 8-bit bus for low address/data transfer. Connect to Port C of 7000CPU.

- o $\overline{\text{INTRQ}}$/PZ7 (OUT/INOUT) — If bit 7 of Port Z Control register is a "1", $\overline{\text{INTREQ}}$ is set to a "Low" when both an INTFLG (interrupt flag) and the corresponding INTEN (Interrupt Enable) are a "1".

- o $\overline{\text{RSTI}}$ (IN) — A system reset input terminal, which at a "0" sets the PIT internal circuit to initial condition .

- o $\overline{\text{RSTO}}$ (OUT) — When $\overline{\text{RSTI}}$ = a "0", $\overline{\text{RSTO}}$ is also cleared to a "0" of an initial condition. If the base address is written into the Mapping Register (Register $(FF)_{16}$) after $\overline{\text{RSTI}}$ returns form a "0" to a "1", $\overline{\text{RSTO}}$ will be set a "1". $\overline{\text{RSTI}}$ and $\overline{\text{RSTO}}$ are used by daisy chain in this manner.

6. Register Address Map

A list of the registers is given on the following page. The address of the registers are shown in the address column, the first 4 bits marked by a "␣" are assigned by the Address Mapping Register. The register marked by a '•' in the 'Read' column indicates 'Read Enable', while the register marked by a '•' in the 'Write' column indicates 'Write Enable'.

Address HEX	Register name	Read	Write	Register contents								Register by Application					Remarks
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	I/O	T1	T2	H/S(X)	H/S(Y)	
_0	Port X Data Register	●	●	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0	●			●		
_1	Port X Direction register	●	●	dir_7	dir_6	dir_5	dir_4	dir_3	dir_2	dir_1	dir_0 Note 1	●			●		0:Input All 0 at reset 1:Output
_2	Port Y Data register	●	●	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0	●				●	
_3	Port Y Direction register	●	●	dir_7	dir_6	dir_5	dir_4	dir_3	dir_2	dir_1	dir_0 Note 1	●				●	0:Input All 0 at reset 1:Output
_4	Port Z Data register	●	●	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0	●					
_5	Port Z Direction register	●	●	dir_7	dir_6	dir_5	dir_4	dir_3	dir_2	dir_1	dir_0	●					0:Input All 0 at reset 1:Output
_6	XY Control register	●	●	Port X				Port Y					● Note 2	● Note 2	●	●	All 0 at reset
				PXHSE	CXIPE	CXOPL	CXODT	PYHSE	CYIPE	CYOPL	CYODT						
_7	Port Z Control register	●	●	INTRQ	TCLK	TXOUT	TIOUT	CYOUT	CYIN	CXOUT	CXIN		● Note 2	● Note 2	●	●	All 0 at reset
_8	Timer 1 High data register	●	●	d_{15}	d_{14}	d_{13}	d_{12}	d_{11}	d_{10}	d_9	d_8		●				Write: Timer latch value Read: Current timer value (By reading _9 after _8)
_9	Timer 1 Low data register	●	●	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
_A	Timer 1 control register		●	Start	Source	Free run	External enable	—	—	—	—		●				
_B	Timer 1 capture latch High data register	●		d_{15}	d_{14}	d_{13}	d_{12}	d_{11}	d_{10}	d_9	d_8		●				
_C	Timer 1 capture latch low data register	●		d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
_C	Timer 2 high data register	●	●	d_{15}	d_{14}	d_{13}	d_{12}	d_{11}	d_{10}	d_9	d_8			●			Write: Timer latch value Read: Current timer value (By reading _D after _C)
_D	Timer 2 low data register	●	●	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
_E	Timer 2 control register		●	—	—	—	—	Start	Source	Free run	External trigger			●			
_E	Timer status register	●		T1 Start	T1 Source	T1 Free run	T1 External enable	T2 Start	T2 Source	T2 Free run	T2 External trigger		●	●			
_F	Interrupt control register		●	CXIN Clear	CXIN enable	CYIN Clear	CYIN enable	T1 Clear	T1 enable	T2 Flag	T2 enable		●	●	●	●	CXIN/CYIN flags automatically cleared by data read/write T1/T2 flags should be cleared through software
_F	Interrupt status register	●		CXIN Flag	CXIN enable	CYIN Flag	CYIN enable	T1 Flag	T1 enable	T2 Flag	T2 enable						
FF	Address mapping register		●	ADDR 7	ADDR 6	ADDR 5	ADDR 4	—	—	—	—						One write operation enables only after reset

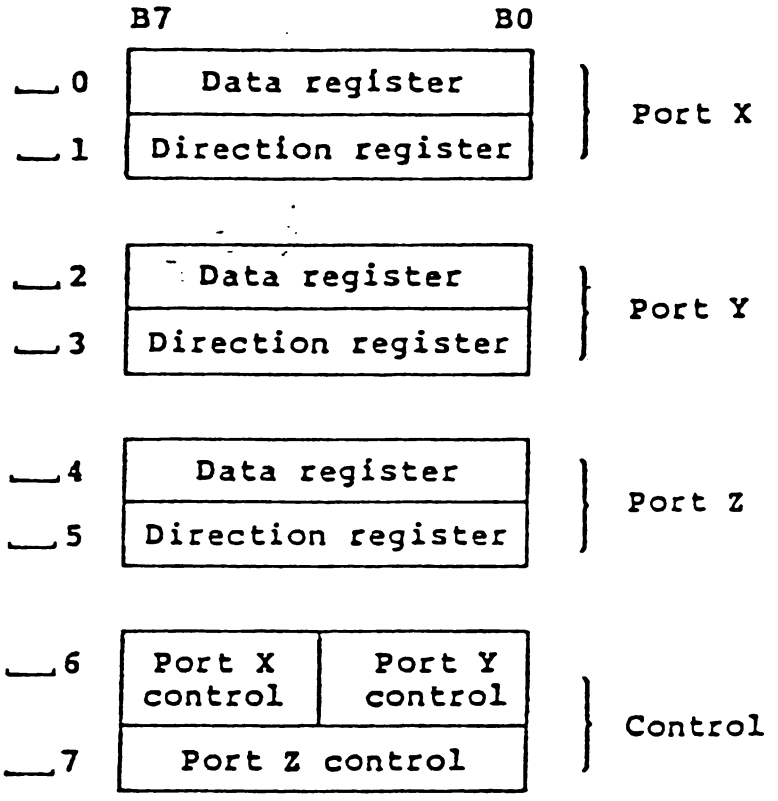
*Note : '_' on address column indicates contents of address mapping register ($ADDR_7$ - $_4$).

*Note 1 : When port X/port Y are used with H/S, Bit 0 of port X/Port Y direction register programs each port as an input OR output.

*Note 2 : CXIN/CYIN can be used for timer without H/S. In detail refer Section 9.2.

7.. I/O Port Register

There are a total of 8 registers for the PIT bidirectional I/O ports: Control register, Direction register and Data register for Ports X, Y, Z. Each register is mapped as follows:



This '⌴' mark indicates the contents of the Address Mapping register, and all the '⌴' marks in this manual have the same meaning.

Fig. 1 I/O Port Register

7.1 Data Register and Direction Register

Each bidirectional 8 bit port may be programmed to be an input or output by the corresponding direction register. A bit set to a '1' in the direction register will cause the corresponding PIN to be an output, while a zero will cause the PIN to be a high impedance input.

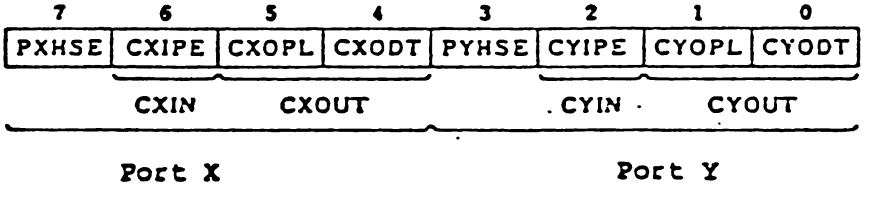
* Setting of the direction register

  0 : Input 1 : Output

  (All set to 0 at reset)

7.2 XY Control Register

XY Control registers are used for handshaking port X or port Y.



o Bits 7/3: Port X, Port Y handshake enable bits

If a '0',port X,Port Y are general-purpose I/O ports. The direction register progams each I/O pin as an input or an output.

If a '1',enables I/O with H/S, each bit of each port may be programmed to be an input or an output by the corresponding direction register.

- Bits 6/2: Selects active edge of CXIN, CYIN. (For H/S or T1 external enable, T2 external trigger)

  If a '0',falling edge is selected. (¯|_) (*1)

  If a '1',rising edge is selected. (_|¯) (*1)

  CXIN flag or CYIN flag of Interrupt Control register is set to a '1' when the active edge of the corresponding PIN is acknowledged.

- Bits 5/1: Selects the output mode for CXOUT, CYOUT under H/S.

  If a '0', 'Level' output selected for CXOUT/CYOUT

  If a '1','Pulse' output selected for CXOUT/CYOUT

- Bits 4/0: Selects output data for CXOUT, CYOUT without handshaking $\overline{(H/S)}$

  If a'0',CXOUT or CYOUT is a 'Low' output (*2)

  If '1', CXOUT or CYOUT is a 'High' output (*2)

  *1 Even if CXIN bit or CYIN bit of Port Z Control register is a'1'under $\overline{H/S}$ disenable (HSE=0), CXIN flag or CYIN flag of Interrupt Control register is set to a '1' when the active edge of the corresponding PIN (CXIN or CYIN) is acknowledged.

  *2 If CXOUT bit or CYOUT bit of Port Z Control register is a '1' under H/S disenable (HSE='0'), the output value from CXOUT or CYOUT pin equals the value of the corresponding bit (CYODT bit or CYODT bit) of XY Control register.

*3 After reset, XY control register is set to all '0'

7.3 Port Z Control Register

When each bit of this register is set to a '0', the corresponding pin of Port Z is used as a I/O pin programmed to an input or an output by Port Z direction register. When set to a '1', the corresponding pin of port Z is used as a special function pin as shown below;

	7	6	5	4	3	2	1	0
⌴7	INTRQ	TCLK	T2OUT	T1OUT	CYOUT	CYIN	CXOUT	CXIN
	INT	Timer			Port Y		Port X	

- o Bit 7: Selects $\overline{\text{INTREQ}}$ output that is a logical OR of all INTFLGS.
- o Bit 6: (IN) Selects TCLK pin as an input of the external clock source for the timer.
- o Bit 5/4: (OUT) Select T2OUT/T1OUT pins as outputs of Timer 1, Timer 2. T1OUT/T2OUT outputs are Toggle Flip-Flop (T-F/F) outputs.
- o Bit 3/1: (OUT) Select CXOUT/CYOUT pins as outputs. The CXOPL/CXODT of XY Control register specify the output mode/output data of CXOUT,

and the CYOPL/CYODT specify the output mode/ output data of CYOUT.

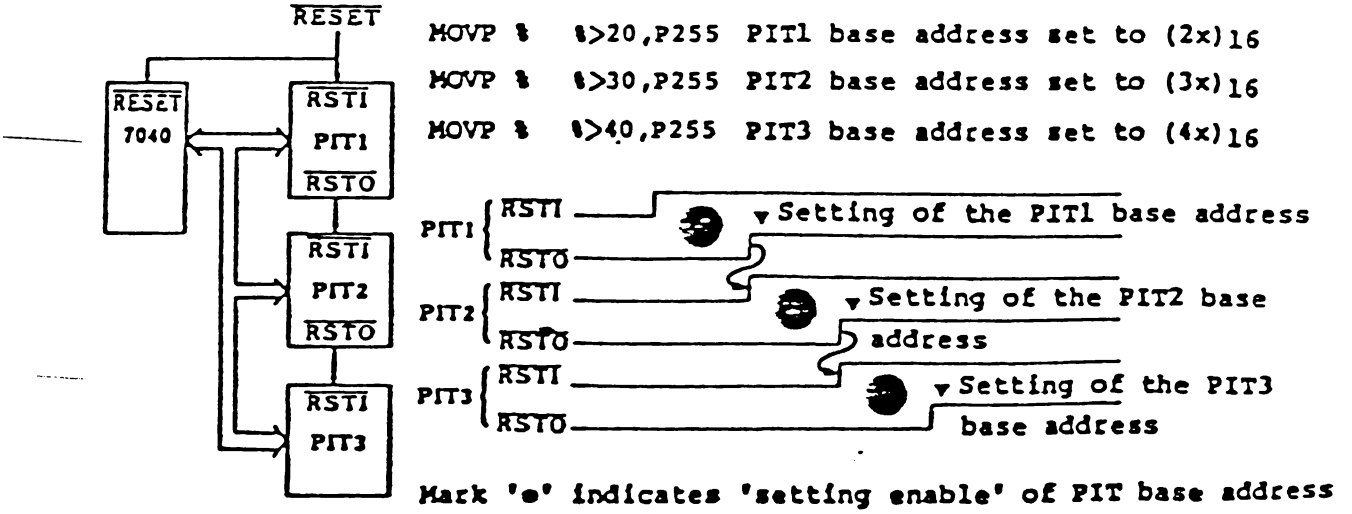
o Bit 2/0: Select CXIN/CYIN pins as inputs.

7.4 Address Mapping Register (Internal Register)

When $\overline{RSTI}$ = a 'H' and $\overline{RSTO}$ = a 'L' (after system reset), the PIT base address is programmed through the 4 bit Address Mapping register located at address $(FF)_{16}$. Once written in, $\overline{RSTO}$ becomes a 'L' and cannot be accessed until $\overline{RSTI}$ returns from a 'L' to 'H'.

Note: Don't set a zero into this Address Mapping register.

Example: PIT base address set after system reset



Setting timing of base address

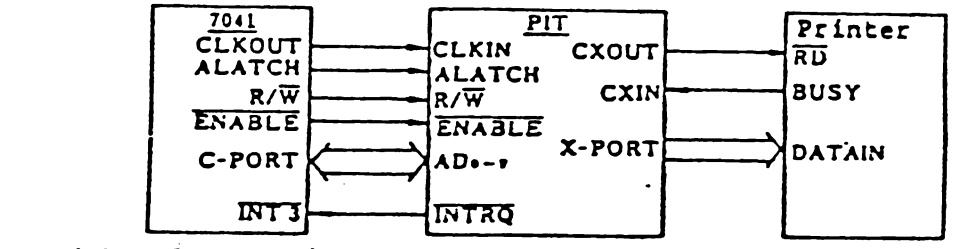
8. Handshake

Handshaking is very useful for a communication with peripherals, CPUS, and simplifies the associated software.

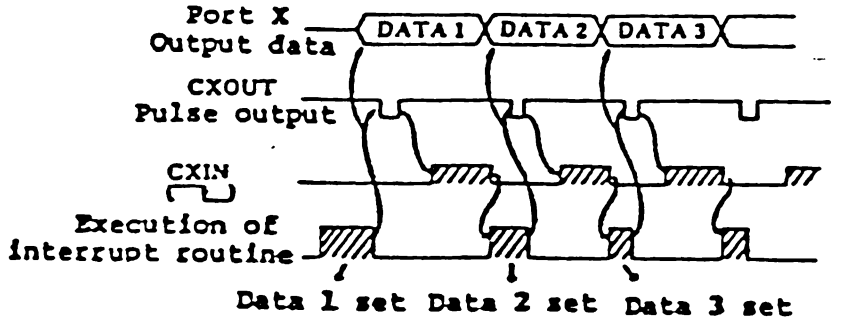
8.1 Handshaking

CXIN, CXOUT/CYIN, CYOUT are H/S signals for Port X/Port Y. Port X (or port Y) H/S is available when PXHSE (PYHSE) of XY Control register and CXIN, CXOUT (CYIN, CYOUT) of port Z Control register are set to a '1'.

Example: Transferring data to the output device through Centronix.



(Peripheral expansion mode)



o Initializing port X

1 Initialize XY control register

i) Specify CXODT bit if need (ex. CXODT = 1)

ii) Specify CXOPL bit (ex. CXOPL =1.....CXOUT pulse output)

iii) Specify CXIPE bit (ex. CXIPE = 0 .... falling edge)

iv) Set a '1' to PXHSE bit to Enable Port X H/S

2 Set CXIN (PZ0), CXOUT (PZ1) of the port Z Control register to a '1'.

3 Set bit 0 of the Port X direction register to a '1' (output mode).

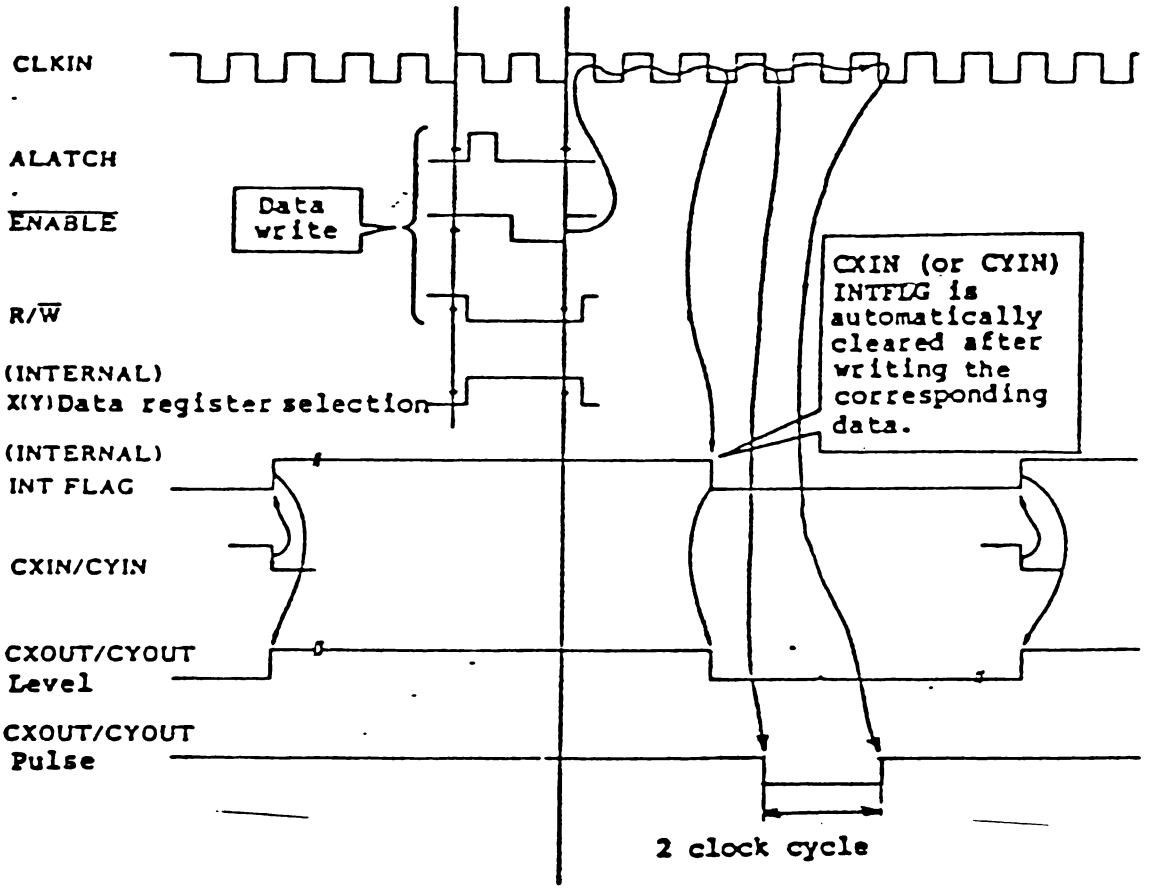
4 Set cxin enable bit of Interrupt Control register to a '1'.

o Interrupt Routine

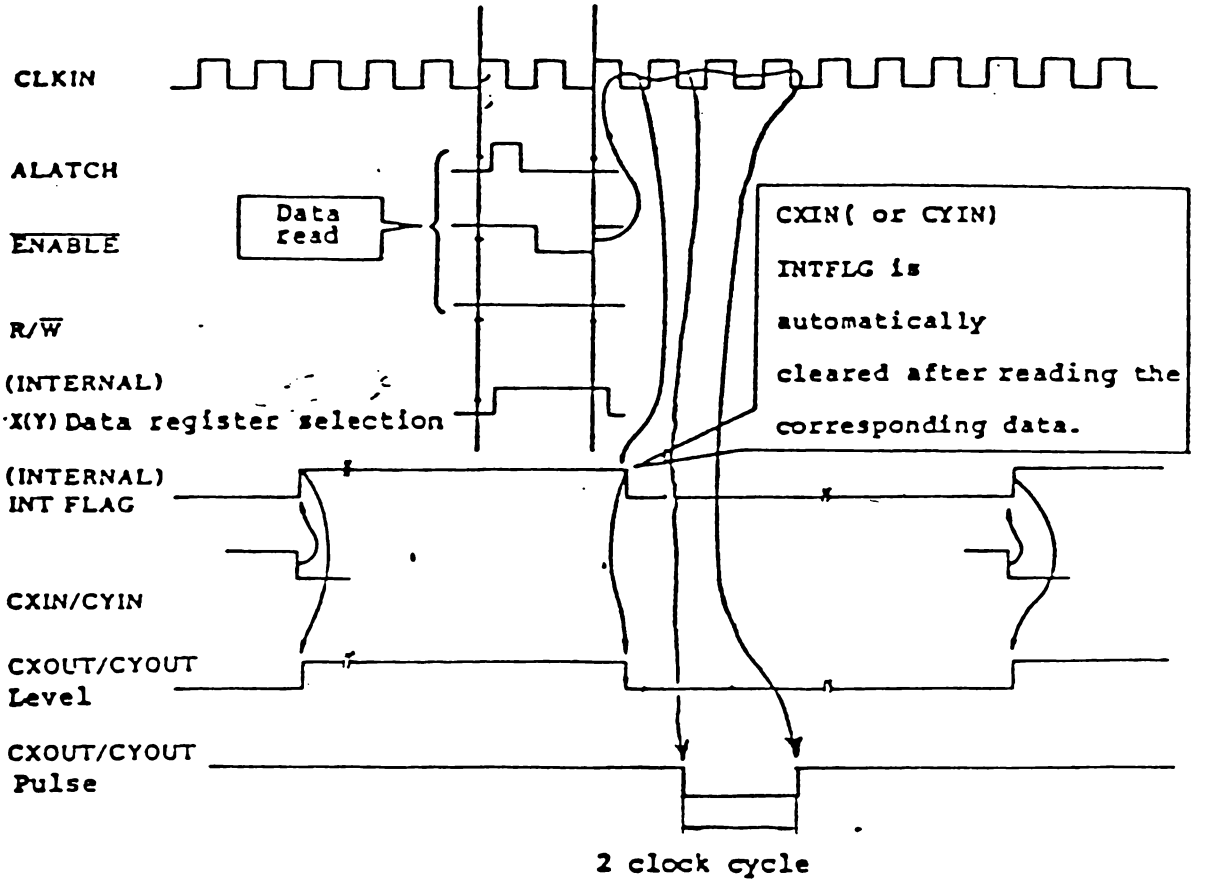
5 If the CXIN INTFLG is a '1', output data to Port X. Otherwise go to the next routine.

8.2. Handshake Timing Chart

Data output through H/S.



Data Input through H/S



9. Timer

By independently programming the bits in the Timer Control register, the 2 Timers can be used in modes to fit a wide variety of applications such as the timer, counter or PWM.

9.1 Configuration and Function of the Timer

9.1.1 Timer Register Map

The addresses of Timer registers are mapped as shown in Fig. 2. The meaning of each register during Read differs from that during Write.

The address for Write ($\llcorner A_{16}$) of Timer 1 Control register is not same as that ($\llcorner E_{16}$) of timer 2 Control register to allow Timer 1, Timer 2 to start independently.

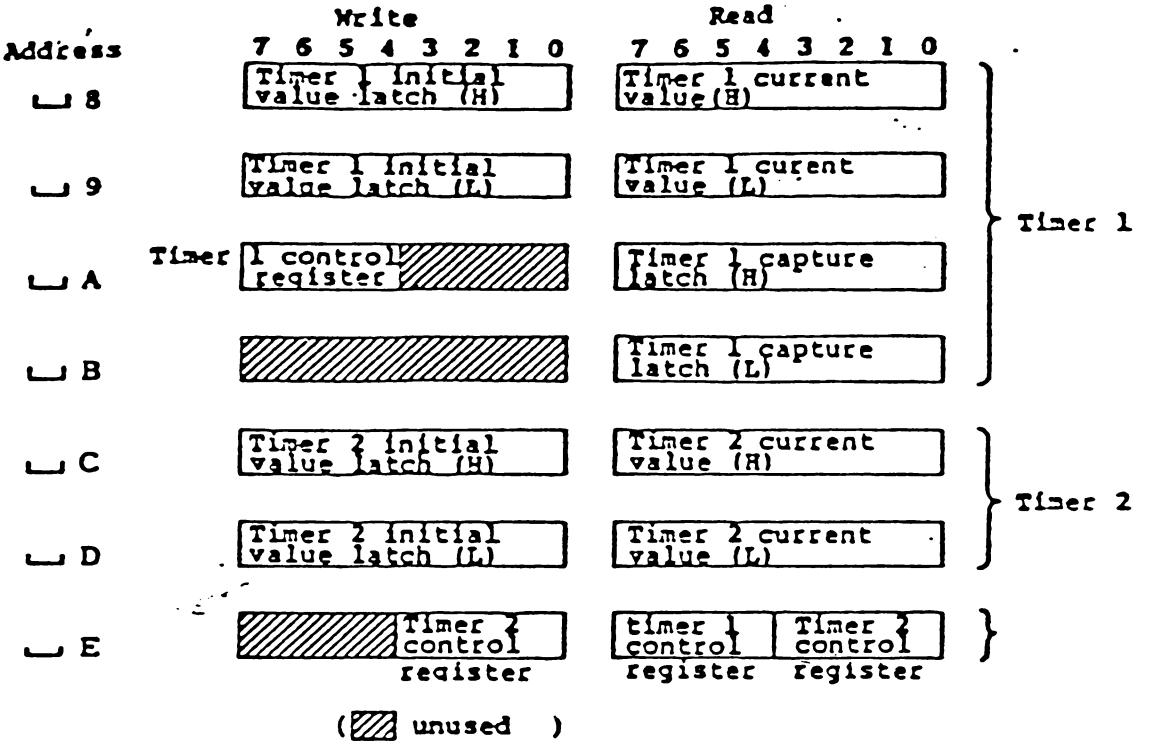


Fig. 2 Timer Register

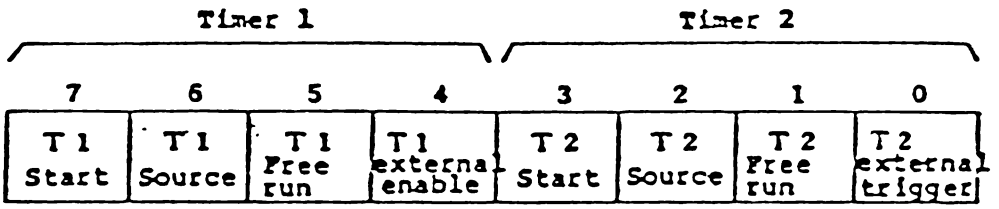
1) Timer Latch/Current Value, Capture Latch Register

The initial value for Timer Latch has 16 bits length, divided into two 8-bits. The initial value for Timer 1 Initial Value Latch is written into address$(_8)_{16}$ for the high address,$(\_9)_{16}$ for the low address, and that for Timer 2 Initial Value Latch into address$(_C)_{16}$ for the high address,$(\_D)_{16}$ for the low address. The high byte of Timer Current Value must be read preceding the low byte. When the high byte of Timer Current Value is read, the Low Data is automatically latched to avoid a data conflict.

Timer 1 Capture Latch Value is stored into $(\_A)_{16}$, $(\_B)_{16}$ when the active edge from CYIN pin is sensed.

2) Timer Control Register

Timer Control registers are for controlling Timer functions as shown below.



Read : Address $(\_E)_{16}$ for both T1,T1

Write : T1 ⇒ high 4 bits of Address $(\_A)_{16}$

T2 ⇒ low 4 bits of Address $(\_E)_{16}$

Fig. 3 Timer Control Register

o Bits 7/3: Timer/Counter start Bit

When a '1' is written in regardless of whether it was a '0' or a '1' before, the Timer initial latch value is loaded into the 16 bit Decrementer and the count down begins.

When a '0' is written in, the ~~Timer is frozen at the current count value.~~ COUNT DOWN IS STOPPED AFTER THE TIMER INITIAL LATCH VALUE IS LOADED INTO THE 16 BIT DECREMENTER.

- Bits 6/2: Decrementer Clock Source Bit

  The clock source of Timer 1/Timer 2 is selected by bit 6/bit 2 of this clock source bit. This bit of a '0' selects the internally generated $\phi/4$ clock (ϕ=CLKIN). This bit of a '1' selects the external clock source from TCLK pin for Timer 1 or CYIN pin for Timer 2. This TCLK/CYIN source are specified by the TCLK bit/CYIN bit of Port Z Control register.

- Bits 5/1: Free Run Mode Bit

  Timer 1, Timer 2 have been designed to operate in a One-shot Timer mode or a Free-run Timer mode (= continuous operating mode).
  This bit of a '0' selects a One-shot Timer mode, and after one Time-Out the start bit of Timer Control register is automatically set to a '0' and then the count is stopped. This bit of a '1' selects a Free-Run Timer mode. Counting is continued until a '0' is written into the start bit of Timer Control register.

- Bit 4: Timer 1 External Enable Bit

  This bit of a '1' selects CXIN pin for Timer 1 Enable signal. If the active level (Note 1) is sensed from CXIN, Timer 1 continues to operate as it is. And, if the non-active level (Note 1) is sensed from CXIN, Timer 1 stopsto count.

Note 1: If a falling edge is specified as the CXIN active edge, the active level=low level and the non-active level=high level.

- Bit 0: Timer 2 External Trigger Bit

  This bit of a '1' selects CXIN pin for Timer 2 external trigger. When the active edge is sensed from CXIN, a '1' is automatically written into the Timer 2 start bit of Timer 2 Control register, and Timer 2 count down begins.

9.1.2 Configuration and Function of Timer 1

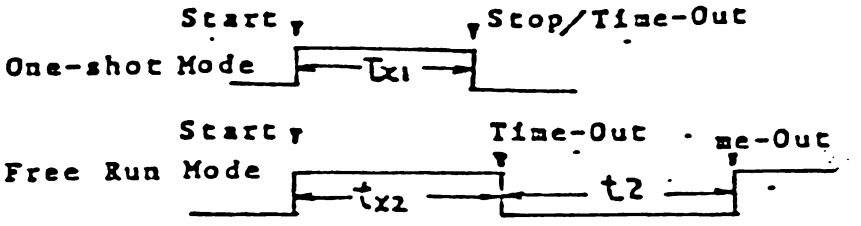
① Write the initial value of Timer 1 Latch into address $(\_^{8})_{16}$, $(\_^{9})_{16}$.

② When the start bit (Bit 7) of Timer Control register is set to a '1', the initial value is loaded into the Decrementer and the count down begins. When set to a '0' the count down is stopped. Re-triggable.

③ Read the address $(\_^{8})_{16}$, $(\_^{9})_{16}$ to obtain the Timer 1 current value. The high byte of the Timer current value must be read preceding the low byte.

④ One-Shot or Free-Run mode can be selected.

⑤ After Timer 1 count starts, T1OUT goes low and then at 1st timeout T1OUT goes high. In Free-Run mode T1OUT is reversed at each timeout.



$t_2 = t_{INTN} = t_{CLK}(TL+1)$
$t_{x1} = t_2 - 2\,t_{CLKIN}$
$t_{x2} = t_2 - (t_{CLKIN}/2)$

t_{CLKIN} : CLKIN PERIOD

⑥ T1 flag bit of Interrupt Control register is set to a '1' at each timeout.

⑦ Internal clock (ø4) or external clock (TCLK) can be selected as the clock source.

⑧ CXIN usable as a External Enable signal by setting the T1 external enable bit of Timer Control register to a '1'.

⑨ Timer 1 has a capture latch. AT the CYIN active edge, the timer value is latched ito Timer 1 Capture Latch mapped to the address $\llcorner A_{16}$, $\llcorner B_{16}$. It doesn't mind whether the address $\llcorner A_{16}$ is read preceding the address $\llcorner B_{16}$ or not.

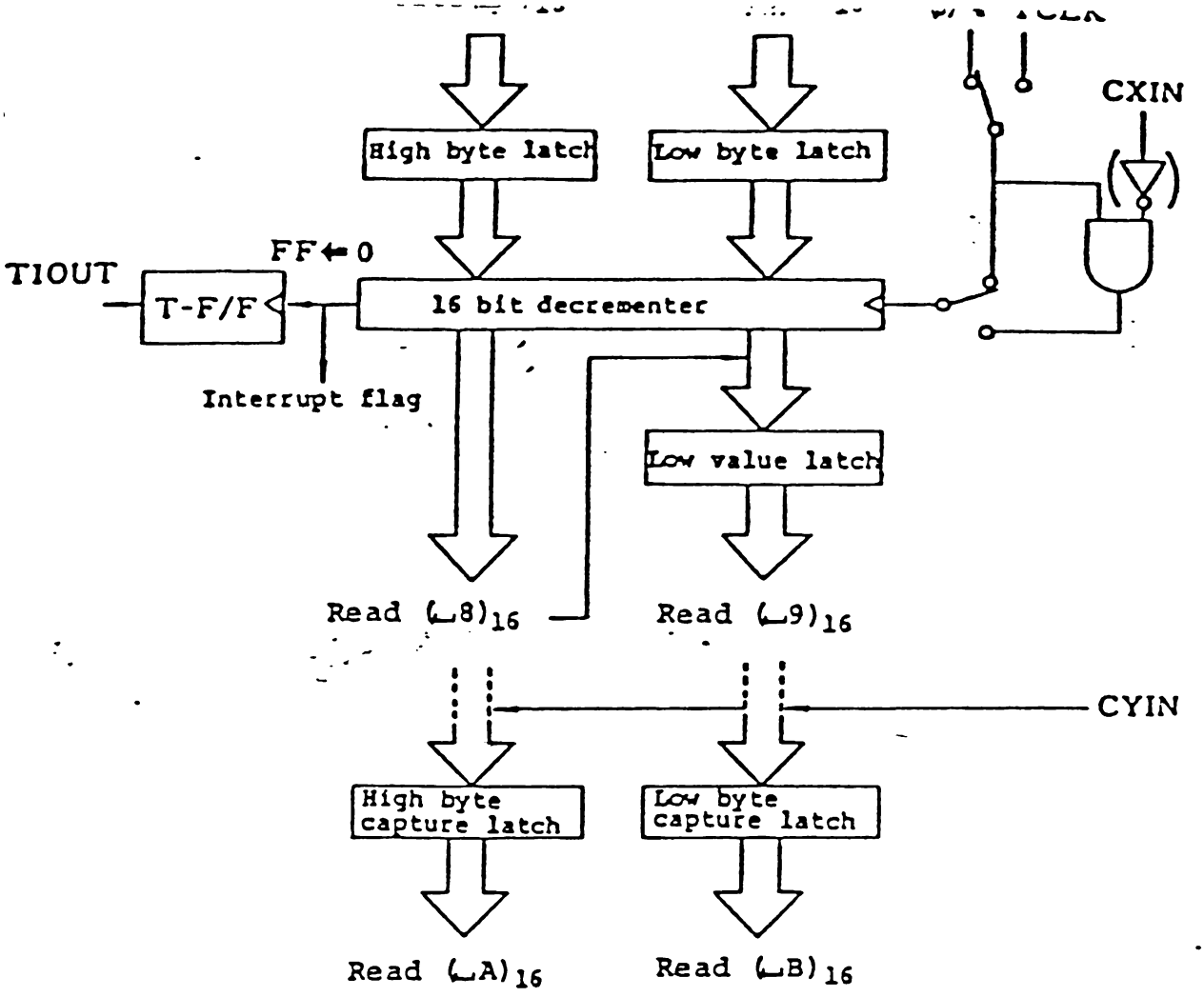


Fig. 4 Configuration of Timer 1

9.1.3 Configuration and Function of Timer 2

① Write the initial value of Timer 2 Latch into the addresss$(C)_{16}$,$(D)_{16}$.

② Identical to the item ② of 9.1.2 except the start bit is bit 3 of Timer Control register.

③ Identical to the item ③ of 9.1.2 except Timer 2 current value is mapped to the address $(\_C)_{16}$, $(\_D)_{16}$.

④ - ⑥ Identical to the item ④ - ⑥ of 9.1.2 except T2OUT is for a timer-output and the Timer 2 interrupt flag is T2FLG of Interrupt Control register.

⑦ Internal Clock ($\phi/4$) or CYIN can be selected as the clock source.

⑧ CXIN usable as an External Trigger by setting T2 External Trigger bit of Timer Control register to a '1'.

⑨ No capture latch function.

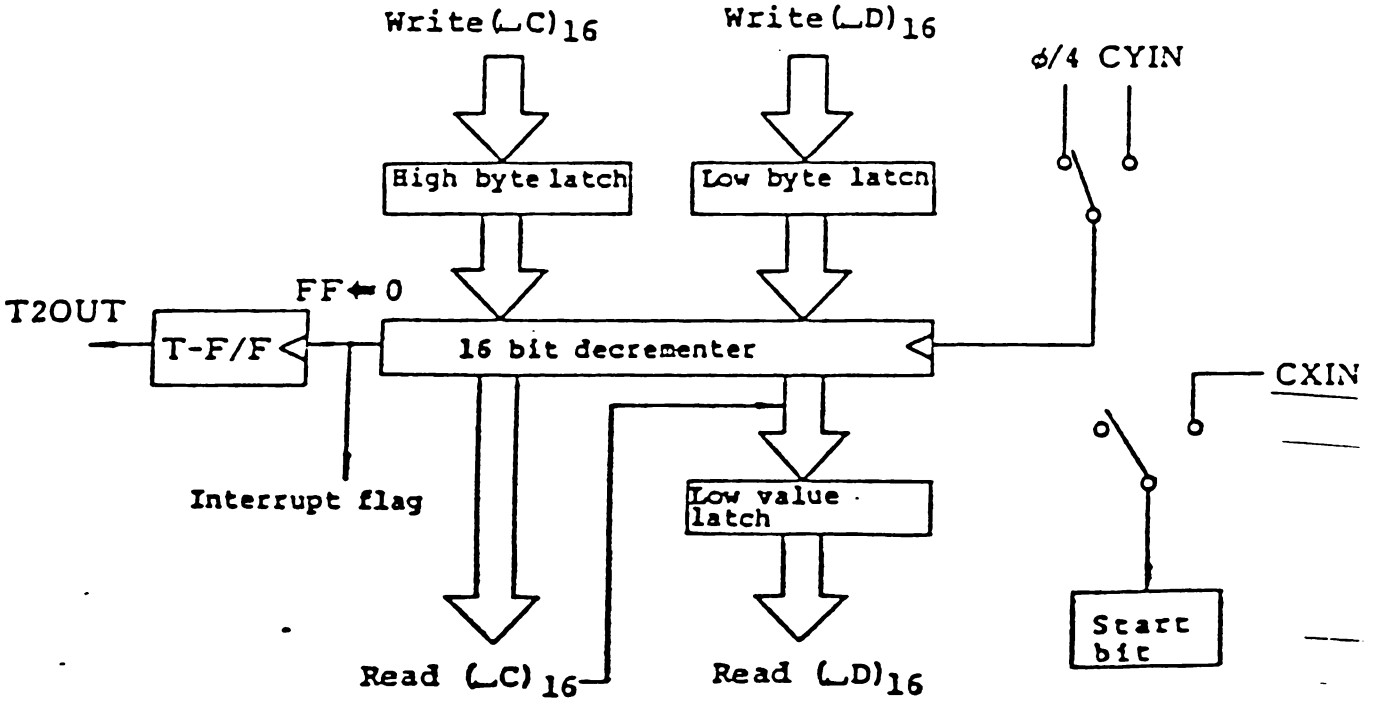


Fig. 5 Configuration of Timer 2

9.2 Timer Operation

There are 2 types of operations, as a timer and as a Counter. It is called a 'Timer' when used for applying Clock Pulses synchronously to the input terminal of the Decrementer Clock, and a 'Counter' when these pulses are applied asynchronously. Timer applications are a time-counter using the internal clock and the measurement of pulse width and so forth. Counter applications are a counting a number of pulses during a defined period, event counting and so forth.

9.2.1 Basic Operating Method of the Timer

The basic method of operating the Timer/Counter is as follows:

① Write the Initial Value into the Timer Latch

The Time Out Period, ~~when the System Clock (internal clock) is used,~~ is expressed through the following equation:

$$tINTn = tCLK \cdot (TL + 1)$$

tINTn : Time Out Period (Interrupt period

unit : second)

tCLK : $4/\phi$ .... (ϕ = CLKIN frequency --- Hz) OR
EXTERNAL SIGNAL PERIOD (SECOND)

TL : Timer latch value (16 bits)

② Write a '1' into the Start Bit of Timer Control Register.

* The initial value is loaded into the Decrementer and the count down begins.

③ A Timer Current value can be obtained by reading Timer Current value register.

* When decremented from $(00)_{16}$ to $(FF)_{16}$, the Timer Interrupt Flag of Interrupt Control Register is set to a '1'.

* In the Free Run Mode, the initial valuie is reloaded automatically after each Time Out and the count down begins.

④ To stop the Counter, write a '0' into the Start Bit of Timer Control Register.

9.2.2 Decrementer Clock Source

2 types of Clock Sources can be selected for both Timer 1 and Timer 2.

1) Timer 1 Clock Source

① The signal divided by 4 CLKIN pulses is used as the internal clock ($\phi/4$).

② Pulses from the TCLK pin (PZ_6) are used for the External Clock.

③ Writing a '0' into the External Enable Bit of Timer Control Register (Bit 4) has no effect on Timer 1 operation.

④ When the External Enable Bit of Timer Control Register is a '1', the count down is stopped if the non-active level is sensed from CXIN pin and the count down is continued if the active level is sensed from CXIN pin.

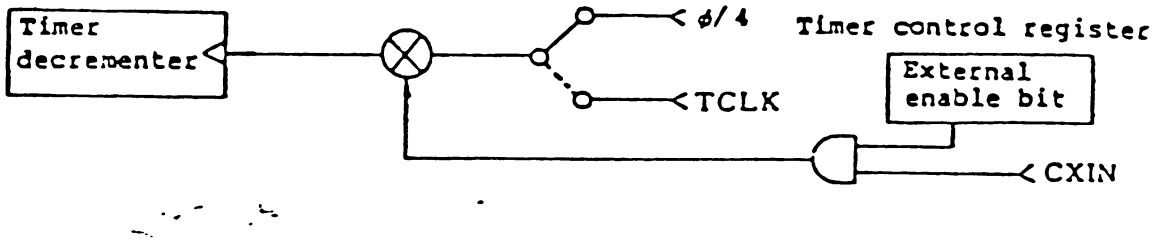


Fig. 6 Timer 1 Block Diagram

2) Timer 2 Clock Source

① The signal divided by 4 CLKIN pulses is used as the internal clock (ϕ/4).

② Pulses from the CYIN (PZ_2) pin are used for the External Clock.

③ Writing a'0'into the External Trigger Bit (bit 0) has no effect on Timer 2 operation.

④ When the External Trigger Bit is a '1' and the active edge is sensed from CXIN pin, a '1' is internally written into the Start Bit of Timer Control Register and the count down begins.

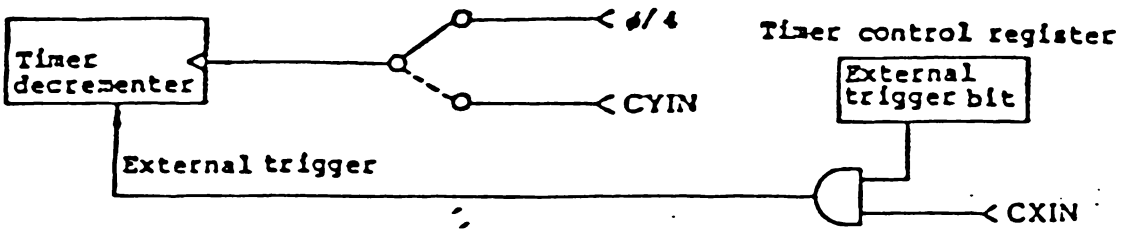


Fig. 7 Timer 2 Block Diagram

9.2.3 Capture Latch

Only Timer 1 is provided with a Capture Latch. The Capture Latch is a register for holding the Timer Value at the time when a defined external signal occurs. The value obtained by reading Timer 1 Curent Value register is not the right timer value you want to know due to a time lag till reading Timer 1 Current Value register. And so the Capture Latch function may be used to get the right timer value.

When the active edge specified by XY Control register is sensed from CYIN pin, the current timer value is latched into Timer 1 Capture Latch register if the CYIN bit of Port Z Control register is a '1'.

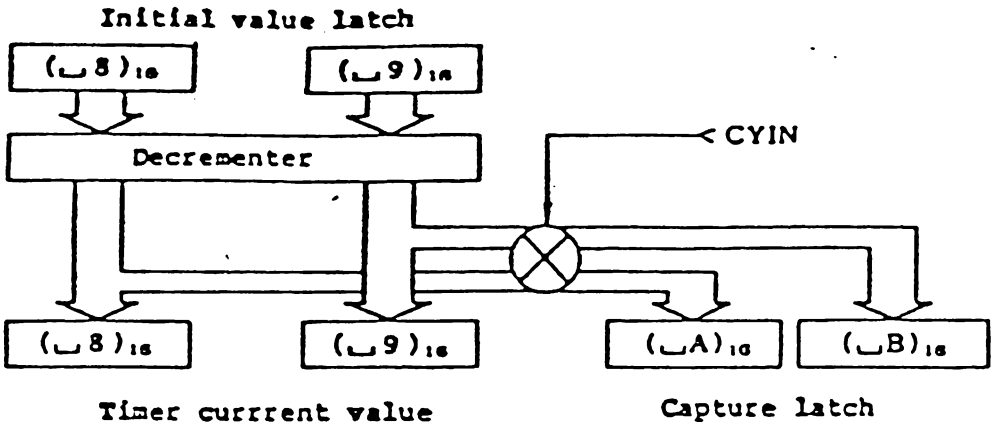
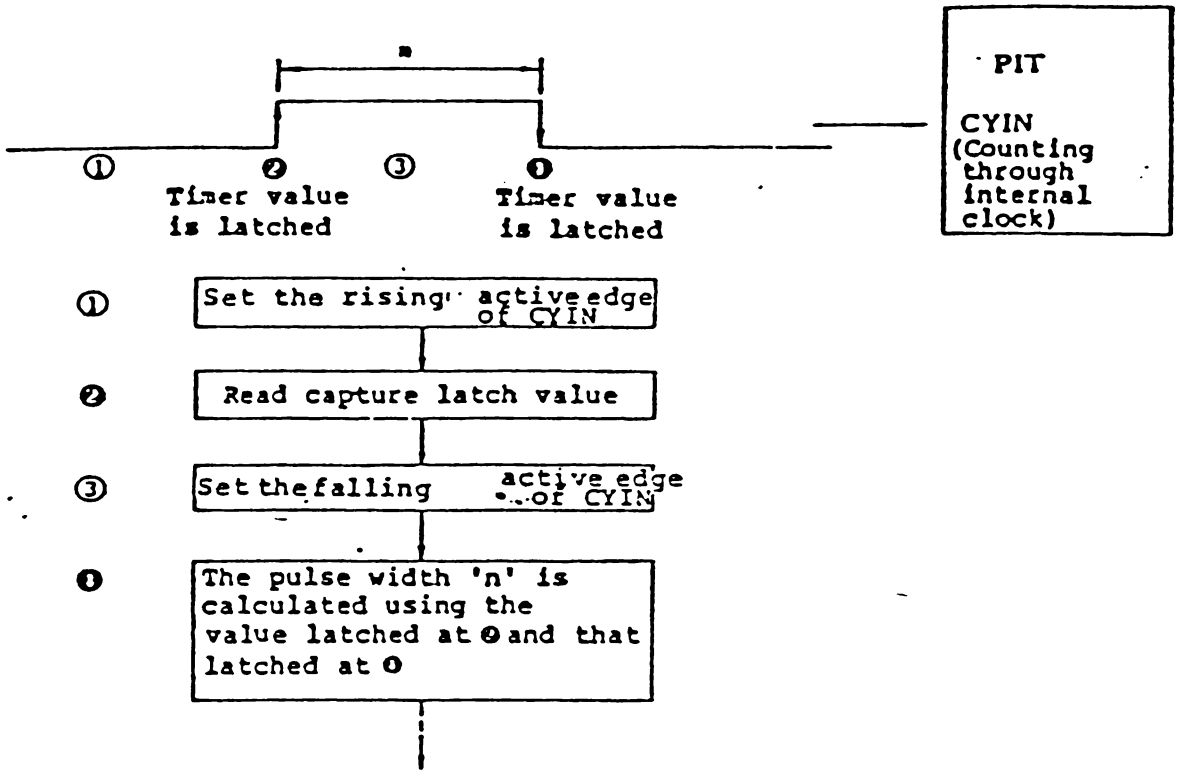


Fig. 8 Capture Latch

(Capture Latch application example)

The following figure shows a Pulse Width measurement example by changing the CYIN active edge from a rising edge to a falling edge.

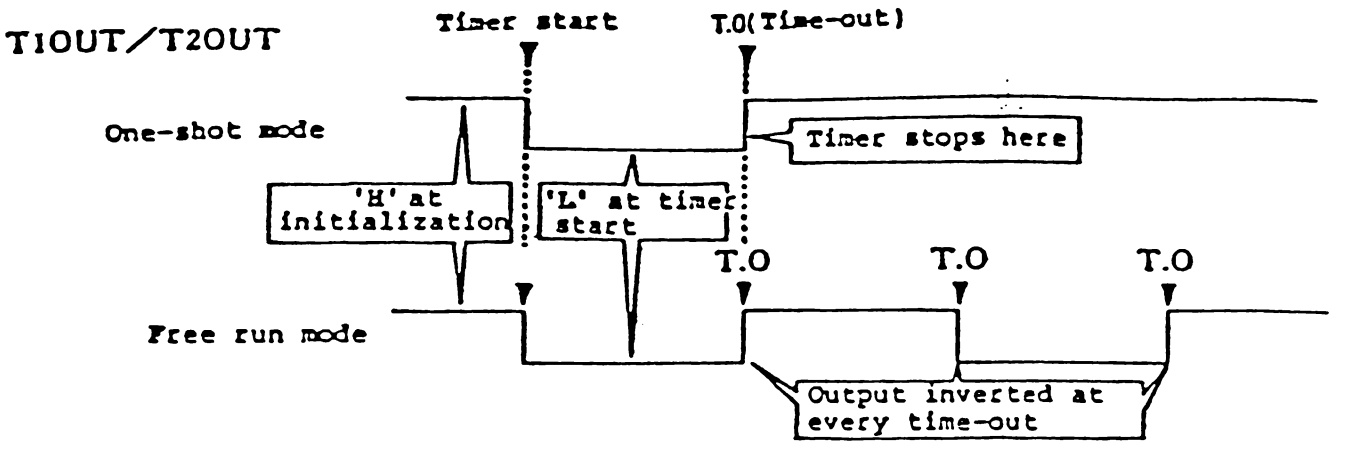


9.2.4 Timer Output

There are 2 types of Timer Outputs, the Time Out Signal (T1OUT, T2OUT) and Timer Interrupt.

1) Time-Out Signal

From T1OUT or T2OUT a square wave will be generated at each Time-Out if the T1OUT bit or T2OUT bit of Port Z Control Register is a '1'.



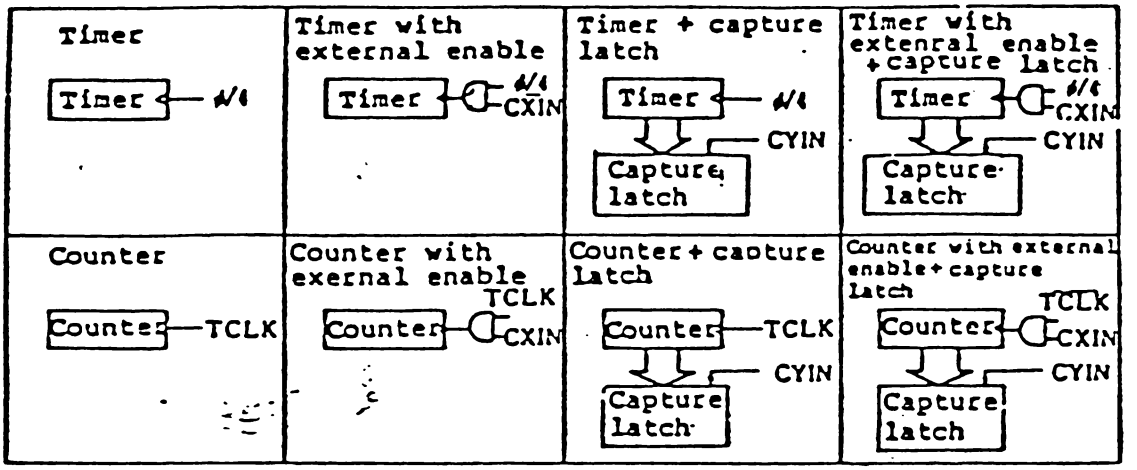
* Under Free Run Mode, the output can be used as a sound source or as an oscillator.

2) Timer Interrupt

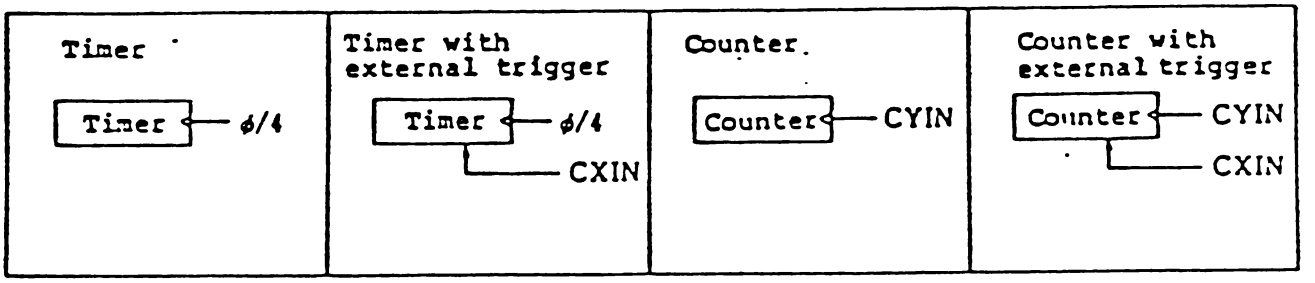
At each time-out the corresponding INTFLG bit of Interrupt Control register is set to a '1' if the corresponding INTEN bit of Interrupt Control register is a '1'. $\overline{\text{INTRQ}}$ pin keeps a 'low' till a logical OR of all $\overline{\text{INTFLGS}}$ is a '0' if the INTRQ bit of Port Z Control register is a '1'. The timer INTFLG (T1INTFLG or T2INTFLG) is cleared by writing a '1' into the corresponding Clear bit of Interrupt Control register. Refer to Section 10 as to Interrupt Control Register.

9.3 Example of Timer Application

Timer 1 (One-Shot or Free-Run mode can be selected)

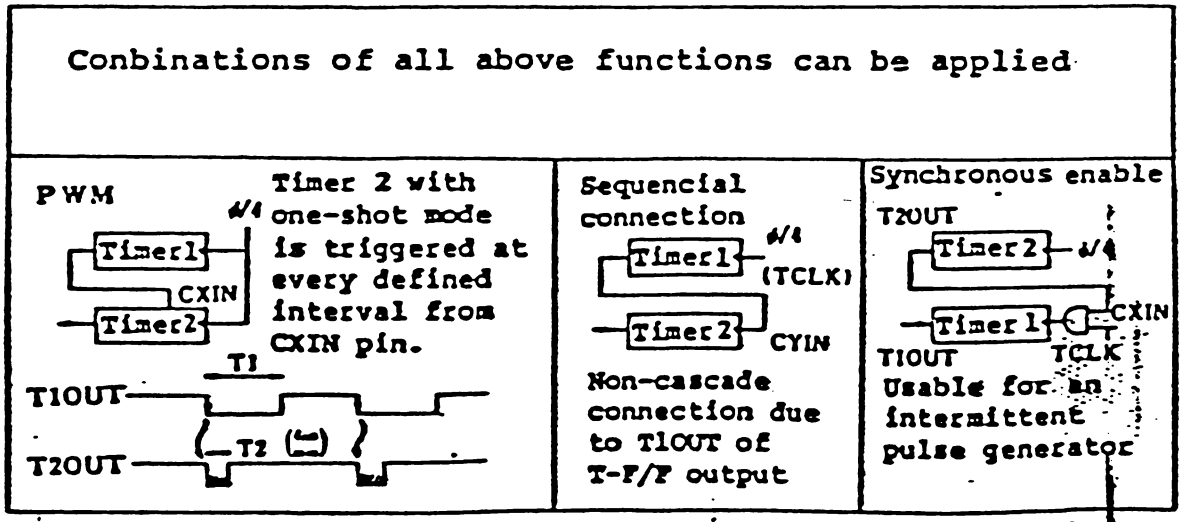


Timer 2 (One-Shot or Free-Run mode can be selected)



Combination of Timer 1, 2

Conbinations of all above functions can be applied



10. Interrupt Control Register

The Interrupt Control Register controls interruptions of Timer 1, Timer 2, Port X H/S and Port Y H/S.
When a '1' is set to Bit 7 of Port Z Control register, the $\overline{\text{INTRQ}}$ pin keeps a 'low' until a logical OR of all INTFLGS of the Enabled Interrupts is a '0'.
CXIN INTFLG or CYIN INTFLG is automatically cleared by Reading or Writing the corresponding Data register. T1 INTFLG or T2 INTFLG must be cleared by the software (by writing a '1 into the corresponding Clear Bit of the Interrupt Control Register).

	Bit 7	6	5	4	3	2	1	0	
F	CXIN Clear	CXIN Enable	CYIN Clear	CYIN Enable	T1 Clear	T1 Enable	T2 Clear	T2 Enable	Write
F	CXIN Flag	CXIN Enable	CYIN Flag	CYIN Enable	T1 Flag	T1 Enable	T2 Flag	T2 Enable	Read

INTEN : CXIN Enable, CYIN Enable, T1 Enable, T2 Enable

INTFLG : CXIN Flag, CYIN Flag, T1 Flag, T2 Flag