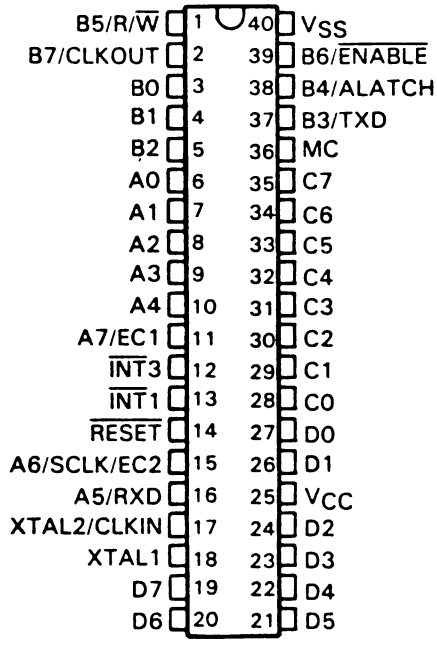
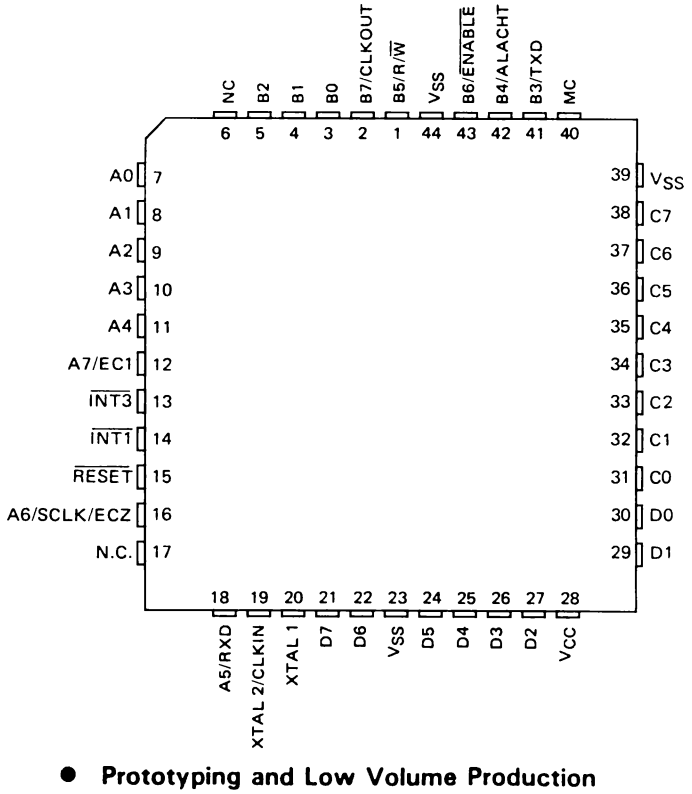
- 8 MHz Maximum Operating Frequency
- TMS7000 Family Compatible
- 4K Byte On-Chip ROM (TMS7042)
- 256 Byte On-Chip RAM Register File
- 32 TTL-Compatible I/O Pins (TMS7042):
  - –22 Bidirectional Pins
  - –8 Output Pins
  - –2 Input Pins
- 32 TTL-Compatible I/O Pins (TMS7002):
  - –20 Pins Used for Addressing and Bus Control
  - –6 Bidirectional Pins
  - –4 Output Pins
  - –2 Input Pins
- Three 8-Bit Timers On-Chip:
  - –Two Timers with 5-Bit Prescale
  - –One Timer with a 2-Bit Prescale
  - –Internal Interrupt with Automatic Timer Reload
  - –Capture Latch
- On-Chip Serial Port:
  - –Asynchronous, Isosynchronous, and Serial Modes
  - –Two Multiprocessor Communication Formats
  - –Error Detection Flags
  - –Fully Software Programmable
  - –Internal or External Baud Rate Generator
  - –Separate Baud Rate Timer Usable as a Third Timer
- Memory-Mapped Ports for Easy Addressing
- Register-to-Register Architecture
- Eight Functional Addressing Formats Including:
  - –Register-to-Register Arithmetic
  - –Indirect Addressing
  - –Indexing and Indirect Branches and Calls
- Memory Expansion to 64K Bytes
- Flexible Interrupt Handling:
  - –Priority Servicing of Simultaneous Interrupts
  - –Software Calls through Interrupt Vectors
  - –Precise Timing of Interrupts through Capture Latch
  - –Software Monitoring of Interrupt Status

N PACKAGE
(TOP VIEW)



PLCC PACKAGE



- Prototyping and Low Volume Production Supported by TMS7742 and SE70P162
- N-Channel Silicon Gate MOS
- 5-Volt Power Supply

TEXAS INSTRUMENTS

description

The TMS7042 is an upward compatible member of the 8-bit TMS7000 family with several performance and feature enhancements. The TMS7042 can operate at 8 MHz, a 60% increase in performance over previous TMS7000 family devices. Other features include 4K bytes of on-chip ROM, 256 bytes of on-chip RAM, three timers, and a flexible serial port (UART), which can operate at a maximum rate of 1M baud when configured in the Isosynchronous mode or at 125K baud when configured in the Asynchronous mode. Also, the TMS7042 features advanced register-to-register architecture that allows direct register arithmetic and logical operations without requiring the use of an accumulator (e.g., ADD R24,R245).

The TMS7002 is the microprocessor version of the TMS7042. It has no on-chip ROM, and uses 20 of the 32 available I/O lines for address and bus control. The TMS7002 can be used in large ROM applications and typical microprocessor applications that take advantage of on-chip features such as the UART, RAM, and timers.

serial port

The serial port of the TMS7042 supports three modes of operation which enable the TMS7042 to communicate with multiple devices using various communication protocol techniques. The TMS7042 is double buffered on both transmit and receive, contains extensive status flag logic that can be used to ensure data integrity, and supports both the Intel and Motorola multiprocessor communications protocols. Also, Timer 3 can be used as an internal baud rate generator. A major enhancement to the serial port is the speed of operation. In the Isosynchronous or Serial I/O mode, the maximum baud rate is one megabit, and in the Asynchronous mode the maximum baud rate is 125 kilobits.

timers

The TMS7042 features three on-chip timers with individual start/stop control bits. Two of these are 8-bit timers with 5-bit programmable prescalers. These timers can be clocked by either the internal oscillator or an external source, and can be cascaded to form a 26-bit timer. Timer 3 is an 8-bit timer with a 2-bit programmable prescaler. This timer can function as a general purpose timer or as a baud rate generator for the serial port. All timers are countdown timers with reload latches. They are automatically reloaded when they count past zero. There is also an 8-bit capture latch which automatically captures the value of Timer 1 when interrupt 3 occurs. This allows very accurate time measurements of external events.

interrupts

There are six prioritized interrupt levels on the TMS7042. Level 0 is the non-maskable reset, levels 1 and 3 are falling edge only external interrupts, level 2 is associated with Timer 1, level 4 is associated with the serial port (receive, transmit, and Timer 3), and level 5 is generated by Timer 2. All interrupts are routed through a user-defined vector to the appropriate service routine; therefore, each service routine can be located anywhere in the TMS7042 address space. There is a global interrupt enable bit in the status register as well as individual interrupt enable bits for interrupts 1 through 5.

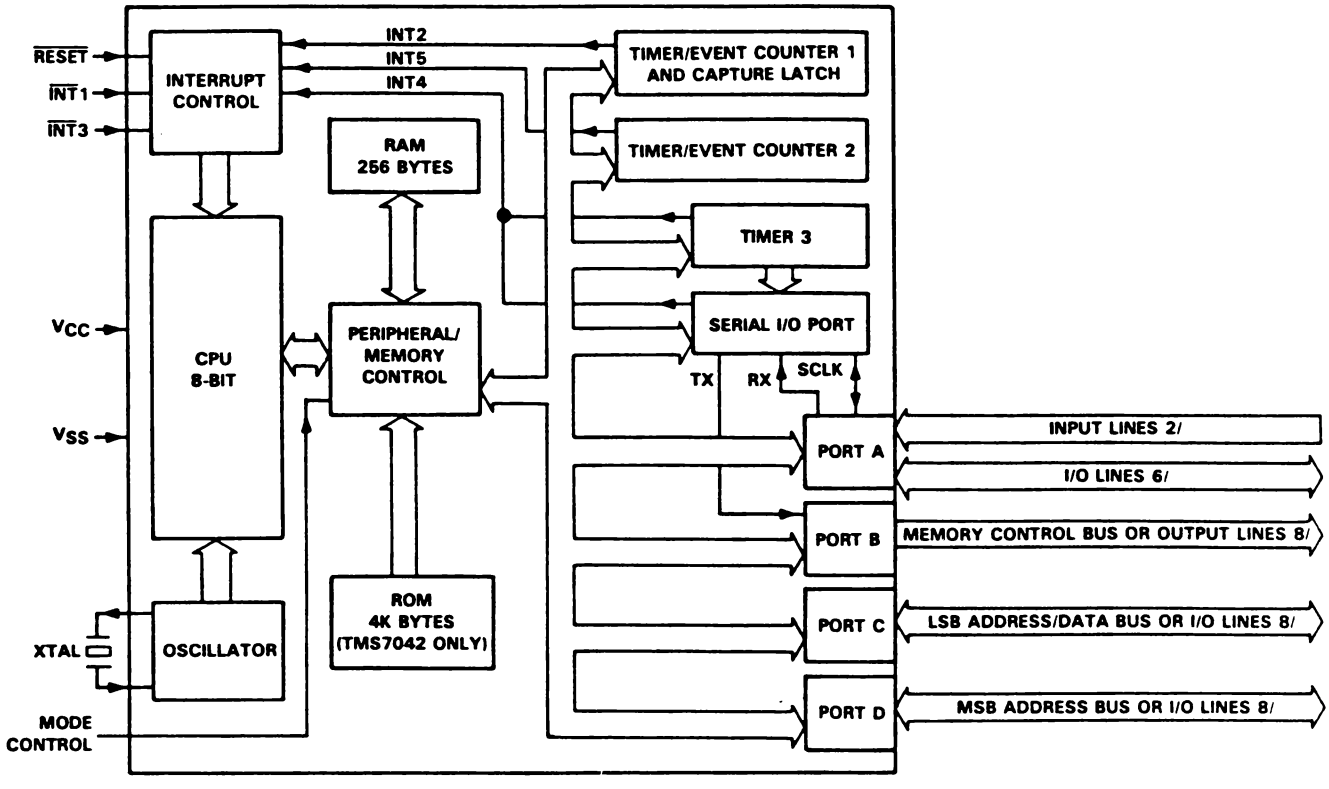
prototyping support

The TMS7742 and SE70P162 prototyping devices provide form factor emulation for the TMS7042.

The TMS7742 is the internally intergrated EPROM version of the TMS7042. The TMS7742 has 4K bytes of on-chip EPROM and can operate at a maximum rate of 5 MHz. The TMS7742 is used for prototyping applications for the TMS7020, TMS7040, TMS7041, and TMS7042, and for applications where program constraints are likely to change periodically.

The SE70P162 is the externally integrated EPROM prototyping device for the TMS7042. The SE70P162 can accommodate up to 16K bytes of EPROM in the piggyback socket and can operate at a maximum rate of 8 MHz. The SE70P162 is designed for prototyping and development and is not recommended for production.

functional block diagram



pin descriptions

PIN NAME	PIN NO DIL	PIN NO PLCC	I/O	DESCRIPTION
A0	6	7	I/O	A0-A4 and A7 are general purpose bidirectional pins; A5 and A6 are input-only data pins.
A1	7	8	I/O	
A2	8	9	I/O	
A3	9	10	I/O	
A4	10	11	I/O	
A5/RXD	16	18	I	Data input/Serial port receiver
A6/SCLK/EC2	15	16	I/O	Data input/Serial port clock/Timer 2 event counter
A7/EC1	11	12	I/O	Data I/O/Timer 1 event counter
B0	3	3	O	B0-B3 are outputs. B4-B7 are outputs in Single-Chip mode and memory interface pins in all other modes
B1	4	4	O	
B2	5	5	O	
B3/TXD	37	41	O	Data output/Serial port transmitter
B4/ALATCH	38	42	O	Data output/Memory interface address latch strobe
B5/R/$\overline{W}$	1	1	O	Data output/Memory interface Read/Write signal
B6/$\overline{ENABLE}$	39	43	O	Data output/Memory interface enable strobe
B7/CLKOUT	2	2	O	Data output/Internal clockout
C0	28	31	I/O	Port C is a bidirectional data port. In Microprocessor mode, Port C is a multiplexed low address and data bus.
C1	29	32	I/O	
C2	30	33	I/O	
C3	31	34	I/O	
C4	32	35	I/O	
C5	33	36	I/O	
C6	34	37	I/O	
C7	35	38	I/O	
D0	27	30	I/O	Port D is a bidirectional data port. In Microprocessor mode, it is the high address bus.
D1	26	29	I/O	
D2	24	27	I/O	
D3	23	26	I/O	
D4	22	25	I/O	
D5	21	24	I/O	
D6	20	22	I/O	
D7	19	21	I/O	
$\overline{INT1}$	13	14	I	Highest priority maskable external interrupt
$\overline{INT3}$	12	13	I	Lowest priority maskable external interrupt
$\overline{RESET}$	14	15	I	Device reset
MC	36	40	I	Mode control pin: V_{CC} for Microprocessor mode (TMS7002)
XTAL2/CLKIN	17	19	I	Crystal input for control of internal oscillator
XTAL1	18	20	O	Crystal output for control of internal oscillator
V_{CC}	25	28		Supply voltage (positive)
V_{SS}	40	23 39 44		Ground reference (All these three pins must be grounded)

mode control

All TMS7000 family members have four different operating modes allowing the optimization of the on-chip versus off-chip memory for each application. These modes are Single-Chip, Peripheral Expansion, Full Expansion, and Microprocessor modes. The table below shows the number of I/O pins and the amount of external address space available in each of the different modes. Note that the TMS7002 normally operates in the Microprocessor mode only.

	SINGLE CHIP	PERIPHERAL EXPANSION	FULL EXPANSION	MICRO-PROCESSOR
Device	TMS7042	TMS7042	TMS7042	TMS7042/TMS7002
I/O Pins:				
Bidirectional	22	14	6	6
Input only	2	2	2	2
Output only	8	4	4	4
Expansion Bus:				
Multiplexed Address/Data lines	0/0	8/8	16/8	16/8
Control lines	0	4	4	4
Memory Space:				
RAM	256	256	256	256
ROM†	4096	4096	4096	0
Peripheral File	18	254	254	254
External Memory	0	0	60,928	65,024

†The first six bytes of ROM (>F000 – >F005) are reserved.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.3 V to 7 V
Input voltage range . . . . . −0.3 V to 20 V
Output voltage range . . . . . −0.3 V to 7 V
Maximum buffer sink current . . . . . 10 mA
Continuous power dissipation . . . . . 1.4 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	CLKIN	2.6			V
		All other inputs	2			V
V_{IL}	Low-level input voltage	CLKIN			0.6	V
		All other inputs			0.8	V
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over full range of operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_I	Input current	A5, MC, $\overline{RESET}$, $\overline{INT1}$, $\overline{INT3}$, XTAL2	V_I = V_{SS} to V_{CC}		±2	±10	μA
		Ports C and D, A0-A4, A6, A7	V_I = 0.4 V to V_{CC}		±10	±100	μA
C_I	Input capacitance				2		pF
V_{OH}	High-level output voltage		I_O = −400 μA	2.4	2.8		V
V_{OL}	Low-level output voltage		I_O = 3.2 mA		0.2	0.4	V
$t_{r(O)}$	Output rise time (see Note 2)		See Figure 2		9	30	ns
$t_{f(O)}$	Output fall time (see Note 2)		See Figure 2		10	35	ns
I_{CC}	Supply current		All outputs open		160	210	mA
$P_{D(av)}$	Average power dissipation				800	1155	mW

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: Rise and fall times are measured between the maximum low level and the minimum high level using the 10% and 90% points (see Figure 2). Outputs have 100-pF loads to V_{SS}.

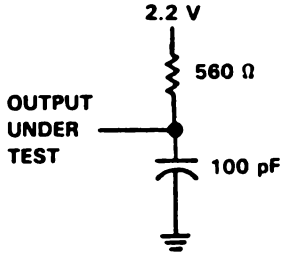


FIGURE 1. TYPICAL OUTPUT LOAD CIRCUIT

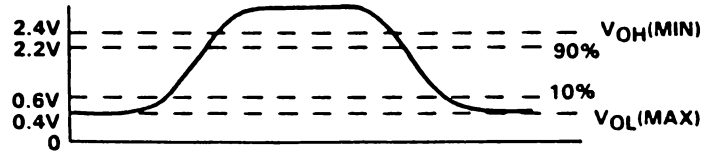


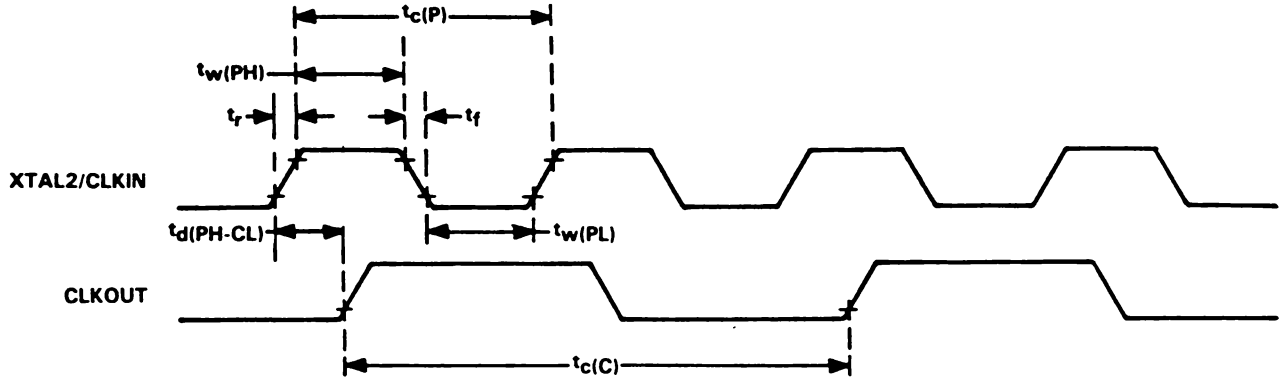
FIGURE 2. MEASUREMENTS POINTS FOR OUTPUT SWITCHING CHARACTERISTICS

recommended crystal operating conditions over full operating range

		MIN	NOM	MAX	UNIT
f_{osc}	Crystal frequency	1		8	MHz
	CLKIN duty cycle		50		%
$t_{c(P)}$	Crystal cycle time	125		1000	ns
$t_{c(C)}$	Internal state cycle time	250		2000	ns
$t_{w(PH)}$	CLKIN pulse duration high	50			ns
$t_{w(PL)}$	CLKIN pulse duration low	50			ns
t_r	CLKIN rise time (see Note 3)			30	ns
t_f	CLKIN fall time (see Note 3)			30	ns
$t_{d(PH-CL)}$	CLKIN rise to CLKOUT rise delay		70	200	ns

NOTE 3: Rise and fall times are measured between the maximum low level and the minimum high level.

clock timing



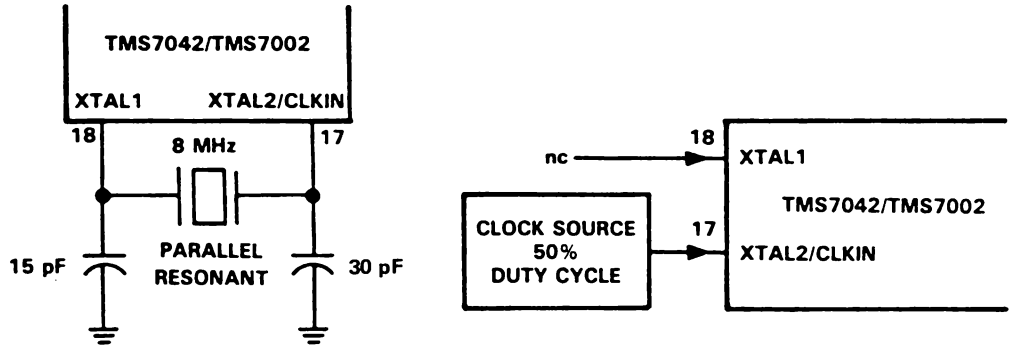


FIGURE 3. RECOMMENDED CLOCK CONNECTIONS

memory interface timing as a function of frequency

In the table below, $t_{c(C)}$ is the period of the internal clock, and $t_{c(C)} = 2/f_{osc}$. At 8 MHz $t_{c(C)}$ would be 250 ns. Minimum and maximum times may be calculated by using the formulas below with the appropriate clock period.

	PARAMETER	MIN	MAX	UNIT
$t_{c(C)}$	CLKOUT cycle time (see Note 4)	250	2000	ns
$t_{w(CH)}$	CLKOUT high pulse duration	$0.5t_{c(C)}-40$	$0.5t_{c(C)}+10$	ns
$t_{w(CL)}$	CLKOUT low pulse duration	$0.5t_{c(C)}-40$	$0.5t_{c(C)}+15$	ns
$t_{d(CH-JL)}$	Delay time, CLKOUT rise to ALATCH fall	$0.5t_{c(C)}-10$	$0.5t_{c(C)}-30$	ns
$t_{w(JH)}$	ALATCH high pulse duration	$0.25t_{c(C)}-15$	$0.25t_{c(C)}-30$	ns
$t_{su(HA-JL)}$	Setup time, high address valid before ALATCH fall	$0.25t_{c(C)}-40$	$0.25t_{c(C)}+45$	ns
$t_{su(LA-JL)}$	Setup time, low address valid before ALATCH fall	$0.25t_{c(C)}-45$	$0.25t_{c(C)}+15$	ns
$t_{h(JL-LA)}$	Hold time, low address valid after ALATCH fall	$0.25t_{c(C)}$	$0.25t_{c(C)}+45$	ns
$t_{su(RW-JL)}$	Setup time, R/$\overline{W}$ valid before ALATCH fall	$0.25t_{c(C)}-35$	$0.25t_{c(C)}+30$	ns
$t_{h(EH-RW)}$	Hold time, R/$\overline{W}$ valid after $\overline{ENABLE}$ rise	$0.5t_{c(C)}-40$	$0.5t_{c(C)}+15$	ns
$t_{h(EH-HA)}$	Hold time, high address valid after $\overline{ENABLE}$ rise	$0.5t_{c(C)}-50$	$0.5t_{c(C)}+35$	ns
$t_{su(Q-EH)}$	Setup time, data output valid before $\overline{ENABLE}$ rise	$0.5t_{c(C)}-45$		ns
$t_{h(EH-Q)}$	Hold time, data output valid after $\overline{ENABLE}$ rise	$0.5t_{c(C)}-45$		ns
$t_{d(LA-EL)}$	Delay time, low address high impedance to $\overline{ENABLE}$ fall	$0.25t_{c(C)}-45$	$0.25t_{c(C)}+15$	ns
$t_{d(EH-A)}$	Delay time, $\overline{ENABLE}$ rise to next address drive	$0.5t_{c(C)}-25$	$0.5t_{c(C)}+80$	ns
$t_{a(EL-D)}$	Access time, data input valid after $\overline{ENABLE}$ fall	$0.75t_{c(C)}-105$		ns
$t_{a(A-D)}$	Access time, address valid to data input valid	$1.5t_{c(C)}-115$		ns
$t_{d(A-EH)}$	Delay time, address valid to $\overline{ENABLE}$ rise	$1.5t_{c(C)}-80$	$1.5t_{c(C)}+30$	ns
$t_{h(EH-D)}$	Hold time, data input valid after $\overline{ENABLE}$ rise	0		ns
$t_{d(EH-JH)}$	Delay time, $\overline{ENABLE}$ rise to ALATCH rise	$0.5t_{c(C)}-25$	$0.5t_{c(C)}+25$	ns
$t_{d(CH-EL)}$	Delay time, CLKOUT rise to $\overline{ENABLE}$ fall	−10	35	ns

NOTE 4: $t_{c(C)}$ is defined to be $2/f_{osc}$ and may be referred to as a machine state or simply a state.

As an example, consider calculating the minimum data out hold time from $\overline{ENABLE}$ rising [$t_{h(EH-Q)}$]. At 8MHz this would give:

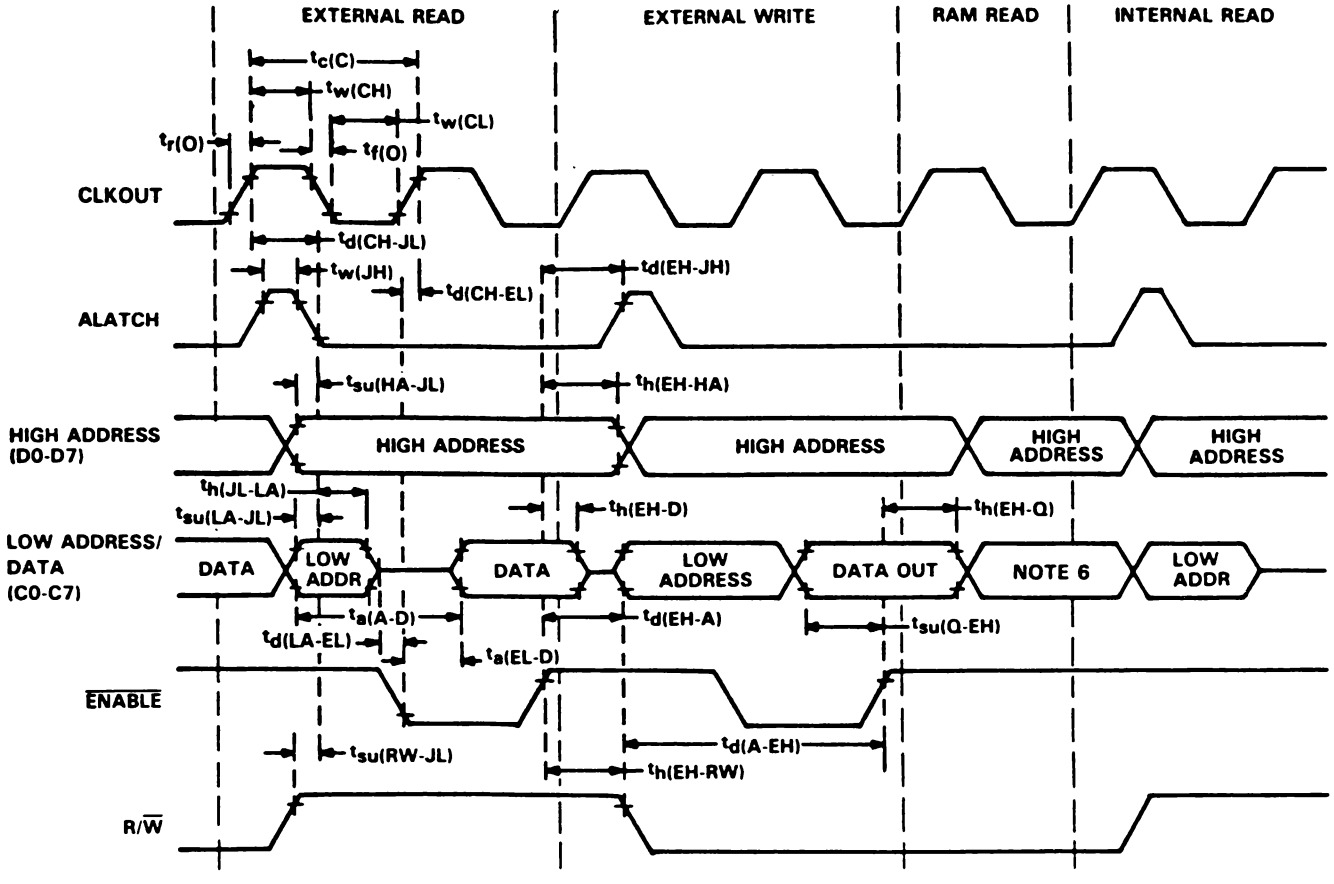
$$t_{h(EH-Q)} = 0.5t_{c(C)} - 45 \text{ ns}$$
$$= 0.5(250 \text{ ns}) - 45 \text{ ns}$$
$$= 125 \text{ ns} - 45 \text{ ns}$$
$$\therefore t_{h(EH-Q)} = 80 \text{ ns}$$

memory interface timing at 8 MHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{c(C)}$	CLKOUT cycle time (see Note 5)	f = 8 MHz, duty cycle = 50%		250		ns
$t_{w(CH)}$	CLKOUT high pulse duration		85	110	135	ns
$t_{w(CL)}$	CLKOUT low pulse duration		85	115	140	ns
$t_{d(CH-JL)}$	Delay time, CLKOUT rise to ALATCH fall		115	135	155	ns
$t_{w(JH)}$	ALATCH high pulse duration		47	70	92	ns
$t_{su(HA-JL)}$	Setup time, high address valid before ALATCH fall		22	65	108	ns
$t_{su(LA-JL)}$	Setup time, low address valid before ALATCH fall		17	50	78	ns
$t_{h(JL-LA)}$	Hold time, low address valid after ALATCH fall		62	90	108	ns
$t_{su(RW-JL)}$	Setup time, R/$\overline{W}$ valid before ALATCH fall		27	60	93	ns
$t_{h(EH-RW)}$	Hold time, R/$\overline{W}$ valid after $\overline{ENABLE}$ rise		85	120	140	ns
$t_{h(EH-HA)}$	Hold time, high address valid after $\overline{ENABLE}$ rise		75	120	160	ns
$t_{su(Q-EH)}$	Setup time, data output valid before $\overline{ENABLE}$ rise		80	120		ns
$t_{h(EH-Q)}$	Hold time, data output valid after $\overline{ENABLE}$ rise		80	115		ns
$t_{d(LA-EL)}$	Delay time, low address high impedance to $\overline{ENABLE}$ fall		17	40	78	ns
$t_{d(EH-A)}$	Delay time, $\overline{ENABLE}$ rise to next address drive		100	150	205	ns
$t_{a(EL-D)}$	Access time, data input valid after $\overline{ENABLE}$ fall		82	120		ns
$t_{a(A-D)}$	Access time, address valid to data input valid		260	300		ns
$t_{d(A-EH)}$	Delay time, address valid to $\overline{ENABLE}$ rise		295	350	405	ns
$t_{h(EH-D)}$	Hold time, data input valid after $\overline{ENABLE}$ rise		0			ns
$t_{d(EH-JH)}$	Delay time, $\overline{ENABLE}$ rise to ALATCH rise		100	105	150	ns
$t_{d(CH-EL)}$	Delay time, CLKOUT rise to $\overline{ENABLE}$ fall		−10	25	35	ns

NOTE 5: $t_{c(C)}$ is defined to be $2/f_{osc}$ and may be referred to as a machine state or simply a state.

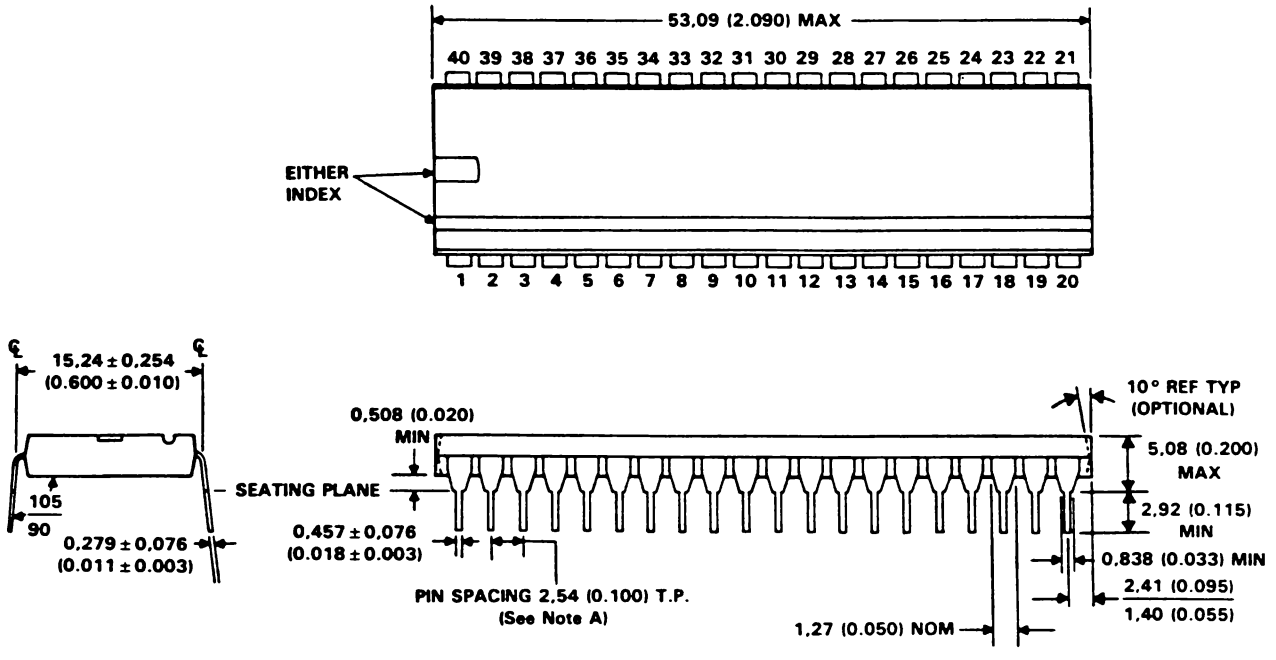
read and write cycle timing



NOTE 6: During an internal RAM access, the CPORT outputs are stable but the data is a "don't care".

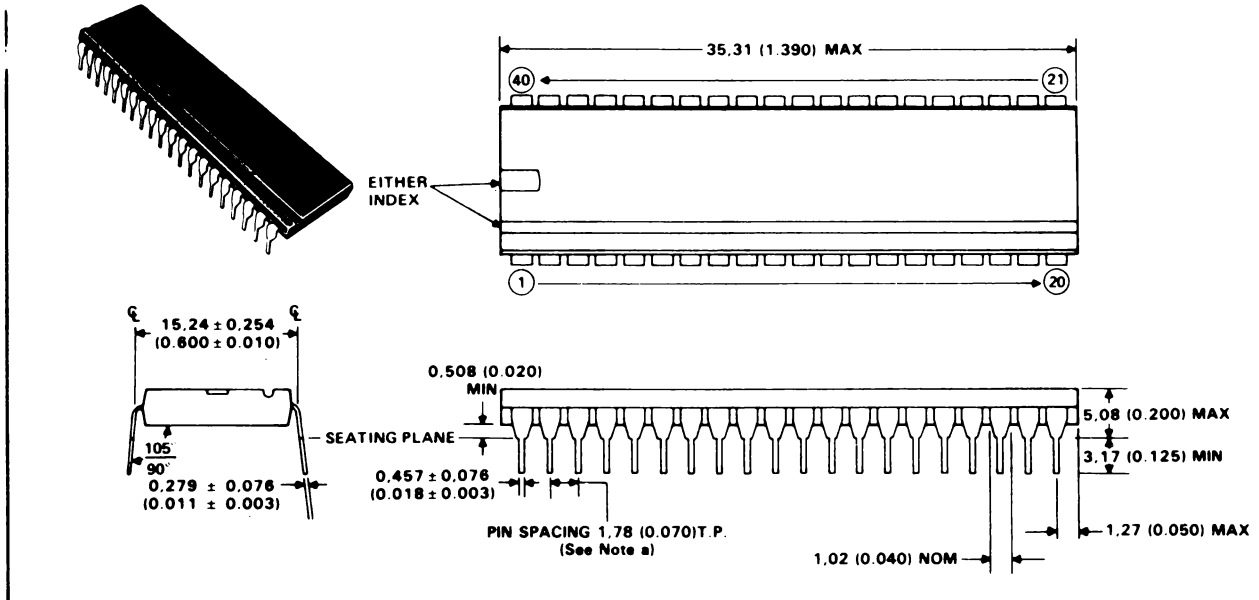
MECHANICAL DATA

40-pin N dual-in-line package (0.100 pin spacing)



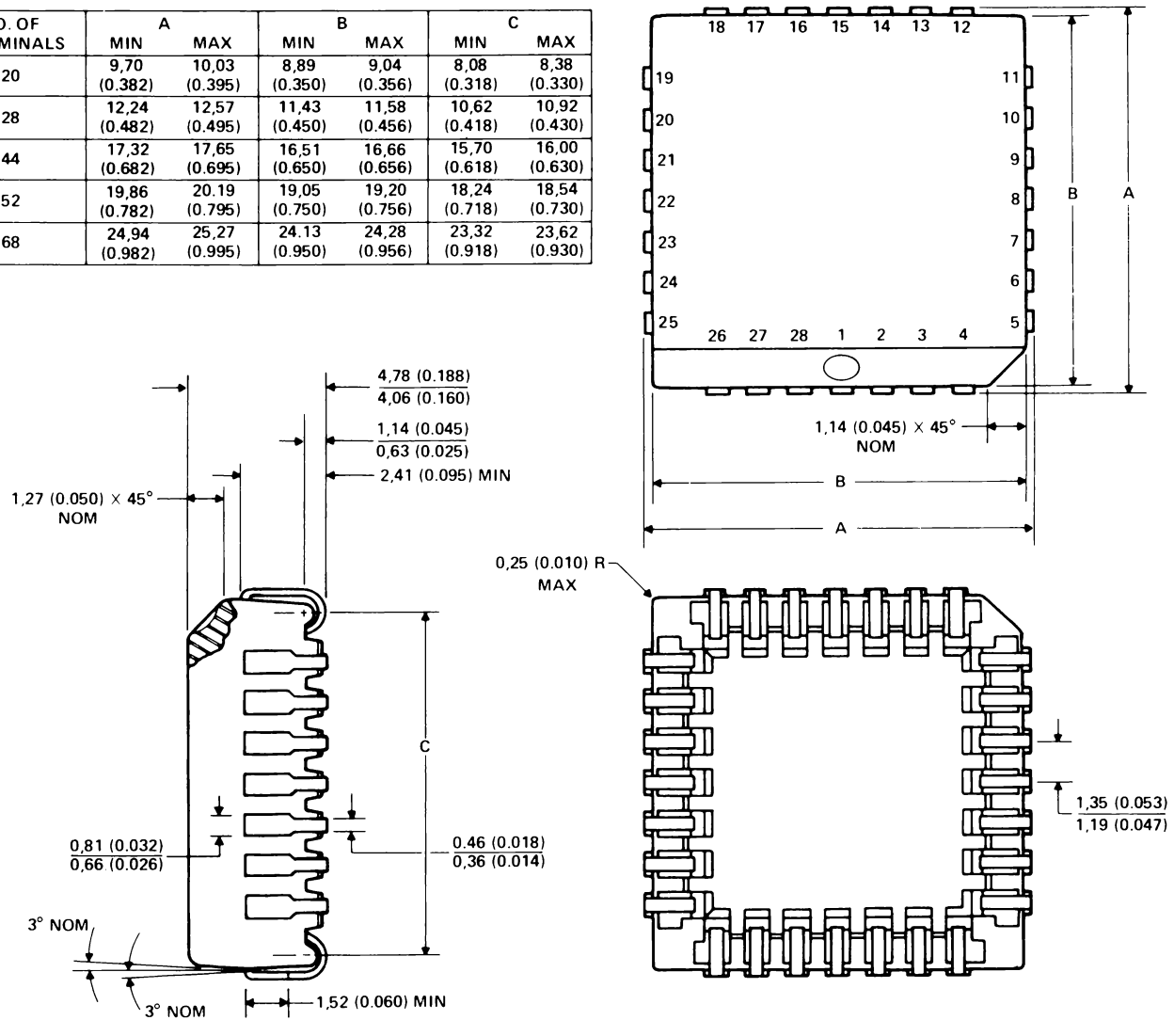
NOTES: a. Each pin centerline is located within 0.254 (0.010) of its true longitudinal position.
b. All linear dimensions are in millimeters and parenthetically in inches.

40-pin plastic package (0.070 pin spacing)



NOTES: a. Each pin centerline is located within 0.254 (0.010) of its true longitudinal position.
b. All linear dimensions are in millimeters and parenthetically in inches.

NO. OF TERMINALS	A		B		C	
	MIN	MAX	MIN	MAX	MIN	MAX
20	9,70 (0.382)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	8,08 (0.318)	8,38 (0.330)
28	12,24 (0.482)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10,62 (0.418)	10,92 (0.430)
44	17,32 (0.682)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	15,70 (0.618)	16,00 (0.630)
52	19,86 (0.782)	20.19 (0.795)	19,05 (0.750)	19,20 (0.756)	18,24 (0.718)	18,54 (0.730)
68	24,94 (0.982)	25,27 (0.995)	24.13 (0.950)	24,28 (0.956)	23,32 (0.918)	23,62 (0.930)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

FN Plastic Chip Carrier Package

Thermal Properties, of Plastic Chip Carriers

NO. OF LEADS	PACKAGE DESIGNATION	θJA (° C/N)	θJC (° C/W)
18	FP	85.4	13.8
20	FN	113.6	37.1
28	FN	76.8	32.2
44	FN	68.0	20.3
68	FN	45.7	11.4

TMS7042 PROTOTYPING SUPPORT

TMS7742 EPROM microcomputer

- TMS7000 Family Compatible
- 4K-Byte On-Chip EPROM
- EPROM Programming Procedure Compatible with TMS2732A
- 256 Byte On-Chip RAM Register File
- 5 MHz Operating Frequency
- 32 TTL-Compatible I/O Pins:
  - —22 Bidirectional Pins
  - —8 Output Pins
  - —2 Input Pins
- Three 8-Bit Timers On-Chip:
  - —Two Timers with 5-Bit Prescale
  - —One Timer with a 2-Bit Prescale
  - —Internal Interrupt with Automatic Timer Reload
  - —Capture Latch
- On-Chip Serial Port:
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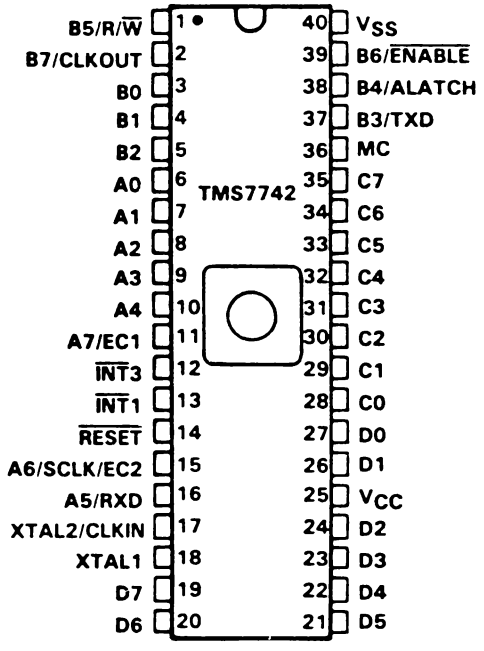
  - —Indexed and Indirect Branches and Calls

(TOP VIEW)



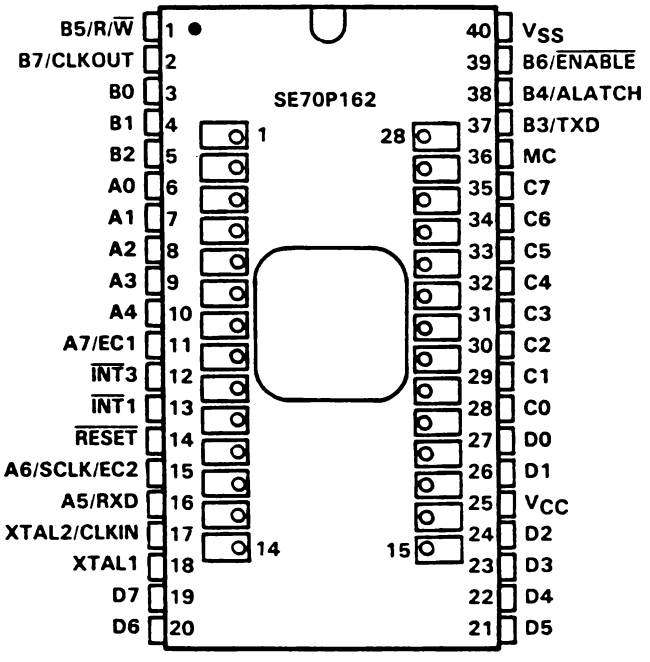
- Flexible Interrupt Handling:
  - —Priority Servicing of Simultaneous Interrupts
  - —Software Calls through Interrupt Vectors
  - —Precise Timing of Interrupts through Capture Latch
  - —Software Monitoring of Interrupt Status
- Supports All TMS7000 Family Expansion Modes
- N-Channel Silicon Gate MOS
- 5-Volt Power Supply (Typical I_{CC} = 180 mA)

The TMS7742 is an EPROM version of the 8-bit TMS7042 microcomputer. The TMS7742 can be used for prototyping applications for the TMS7020, TMS7040, TMS7041, and TMS7042, at a maximum operating frequency of 5 MHz. It can also be used as a low volume alternative to masked ROM parts and for applications where program constraints are likely to change periodically.

SE70P162 piggyback microcomputer

- 8 MHz Operating Frequency
- TMS7000 Family Compatible
- 256 Byte On-Chip RAM Register File
- 32-TTL-Compatible I/O Pins:
  - —22 Bidirectional Pins
  - —8 Output Pins
  - —2 Input Pins
- Three 8-Bit Timers On-Chip:
  - —Two Timers with 5-Bit Prescale
  - —One Timer with a 2-Bit Prescale
  - —Internal Interrupt with Automatic Timer Reload
  - —Capture Latch
- On-Chip Serial Port:
  - —Asynchronous, Isosynchronous, and Serial Modes
  - —Two Multiprocessor Communication Formats
  - —Error Detection Flags
  - —Fully Software Programmable
  - —Internal or External Baud Rate Generator
  - —Separate Baud Rate Timer Usable as a Third Timer
- Memory-Mapped Ports for Easy Addressing
- Register-to-Register Architecture
- Eight Functional Addressing Formats Including:
  - —Register-to-Register Arithmetic
  - —Indirect Addressing
  - —Indexed and Indirect Branches and Calls

(TOP VIEW)†



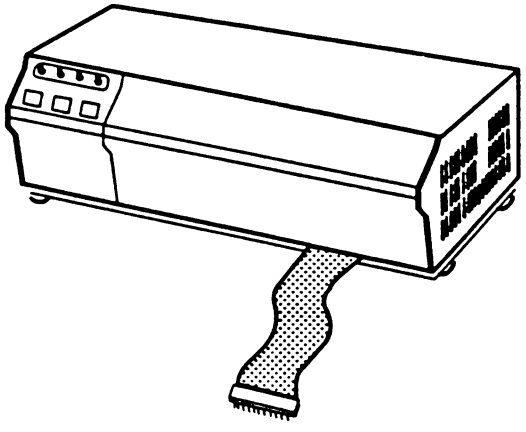
†SE70P162 pin spacing is standard for 40-pin DIP package.

- Flexible Interrupt Handling:
  - —Priority Servicing of Simultaneous Interrupts
  - —Software Calls through Interrupt Vectors
  - —Precise Timing of Interrupts through Capture Latch
  - —Software Monitoring of Interrupt Status
- Supports All TMS7000 Family Expansion Modes
- N-Channel Silicon Gate MOS
- 5-Volt Power Supply

The SE70P162 is a prototyping device for the TMS7042. The SE70P162 is packaged so that a standard TMS2764 or TMS27128 EPROM can be plugged into the socket on top (piggyback). It is designed to be used in the prototyping environment and is tested and supported for that purpose. Texas Instruments does not support or warrant the use of the SE70P162 for production purposes.

TMS7042 DEVELOPMENT SUPPORT

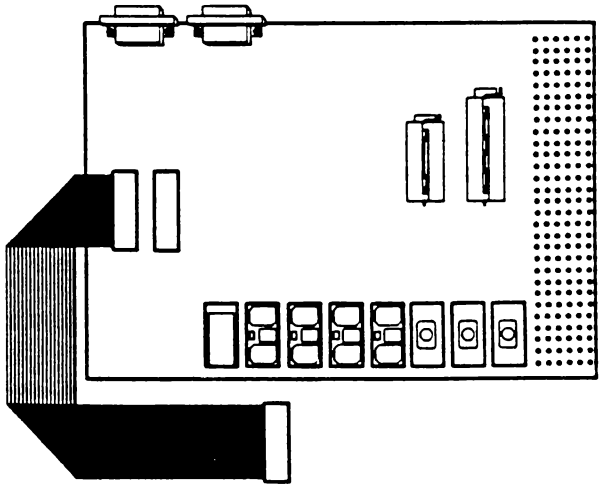
XDS* — extended development system



- Full TMS7000 Family Development System
- Host Independent/RS-232-C Interface
- Full Speed 8 MHz In-Circuit Emulation
- Extensive Breakpoint and Trace Functions
  - —Detailed Timing Analysis
  - —2K-Byte Trace Samples
  - —Breakpoint Sequencing Ability
- Command/Default Storage
- Removable Target Connector
- External Probe for Breakpoint/ Trace Qualifiers
- On-Board Assembler and Reverse Assembler
- Multiprocessing Capabilities

EVM — evaluation module

- TMS7000 Family Low Cost Development System
- Single-Chip Mode Emulation Only
- On-Board Assembler/Line Text Editor
- On-Board Hardware/Software Debugger
- Multiple Breakpoints
- Trace Display Function
- EPROM Programmer Utilities
- NMOS and CMOS versions



assembler/linker packages

Crossware* assembler/linker packages are available through Texas Instruments for the following operating systems:

Operating System	TI Part Number
TI and IBM PC	TMDS7040810-02
DEC VAX VMS	TMDS7040210-08
IBM MVS	TMDS7040310-08
IBM CMS	TMDS7040320-08

*XDS and Crossware are registered trademarks of Texas Instruments Incorporated.

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