SPDU020

XDS TMS7000 Emulator Hardware

XDS Extended Development Support
Installation and Operation Guide

TEXAS INSTRUMENTS

Texas Instruments

The information and/or drawings set forth in this document and all rights in and to inventions disclosed herein and patents which might be granted thereon disclosing or employing the materials, methods, techniques, or apparatus described herein are the exclusive property of Texas Instruments.

No disclosure of information or drawings shall be made to any other person or organization without the prior consent of Texas Instruments.

XDS Group
MS 2186
12501 Research Blvd.
Austin, Texas 78759

IMPORTANT NOTICE

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

Texas Instruments assumes no responsibility for infringement of patents or rights of others based on Texas Instruments applications assistance or product specifications, since TI does not possess full access to data concerning the use or applications of customer's products. TI also assumes no responsibility for customer product designs.

PREFACE

The purpose of this manual is to familiarize the user with the TMS7000 Emulator board, the target connector and the function of the status indicators on the XDS, (Extended Development Support System). This manual also describes installation instructions for the TMS7000 Emulator board, PN 2311080-0001, including the target connector. The user and installer should read this manual before attempting to operate or install any of the TMS7000 Emulator equipment. If the TMS7000 Emulator is removed from the XDS, this manual should be kept with the emulator for reference during future installation.

The following publications are available to support this manual:

Title	Part Number
XDS TMS7000 Emulator User's Guide	1603829-9701
XDS Breakpoint Trace Installation and Operation Guide	1603442-9701
XDS/22 Installation and Operation Guide	1603443-9701

SECTION 1

TMS7000 EMU INSTALLATION

1.1 INTRODUCTION

When the TMS7000 Emulator is delivered with one of the XDS models, the emulator board with the target connector should already be installed. Refer to this section if the board is not installed or if it is to be moved. Also refer to this section if you wish to change the board options.

1.1.1 Board Preparation and Options.

The TMS7000 Emulator board may be configured to support the NMOS version of the TMS7000 family and, with some limitation, the CMOS version. To incorporate this option, you must change the jumper configuration. Also, you can change the frequency of the on-board clock by changing the crystal on the emulator board.

1.1.1.1 Jumper Configuration.

Jumpers E1 through E5 can each be configured in two positions. The first is the jumper plug placed on the lower two of the three stakes which are are the stakes closest to the edge connector of the board. The second position is with the jumper plug placed on the upper two stakes. Before installing the board, make sure that you have installed jumpers E1 through E2 on the lower two stakes and that you have installed E5 on the upper two. The only exception to this configuration is when you desire CMOS emulation. To achieve an edge-only trigger on INT1-, you must install jumper E1 on the upper two stakes. Appendix E of the TMS7000 Emulator User's Guide provides further information on how CMOS emulation is supported.

1.1.1.2 Configuring Clock Frequency.

You can change the frequency of the on-board system clock by replacing crystal Y1 with a parallel resonant crystal of a different value. The factory installes a 5 MHz crystal, which allows you to select internal operating frequencies of 2.5 or 1.25 MHz. If you elect to install a crystal of your own, you must make certain that the resulting operating frequency does not

exceed the maximum specified by the processor's data manual. The emulator will power up with a divide-by-4 option selected. This means that you could install a 10 MHz crystal and the emulator would run at 2.5 MHz internal as long as the divide-by-4 clock option was not altered by the INIT command.

If you are to have access to all 64K of on board memory expansion, the slowest frequency of operation allowed for the TMS7000 emulator is 320 KHz. If you are able to give up half of the available memory expansion, you can run the emulator as slow as 160KHz internal. It is your responsibility to tell the emulator that it will be running slower than 320 KHz by entering the proper response during the INIT command. You should not install a crystal with a value smaller than 640KHz, as the emulator powers up with the divide-by-four option selected.

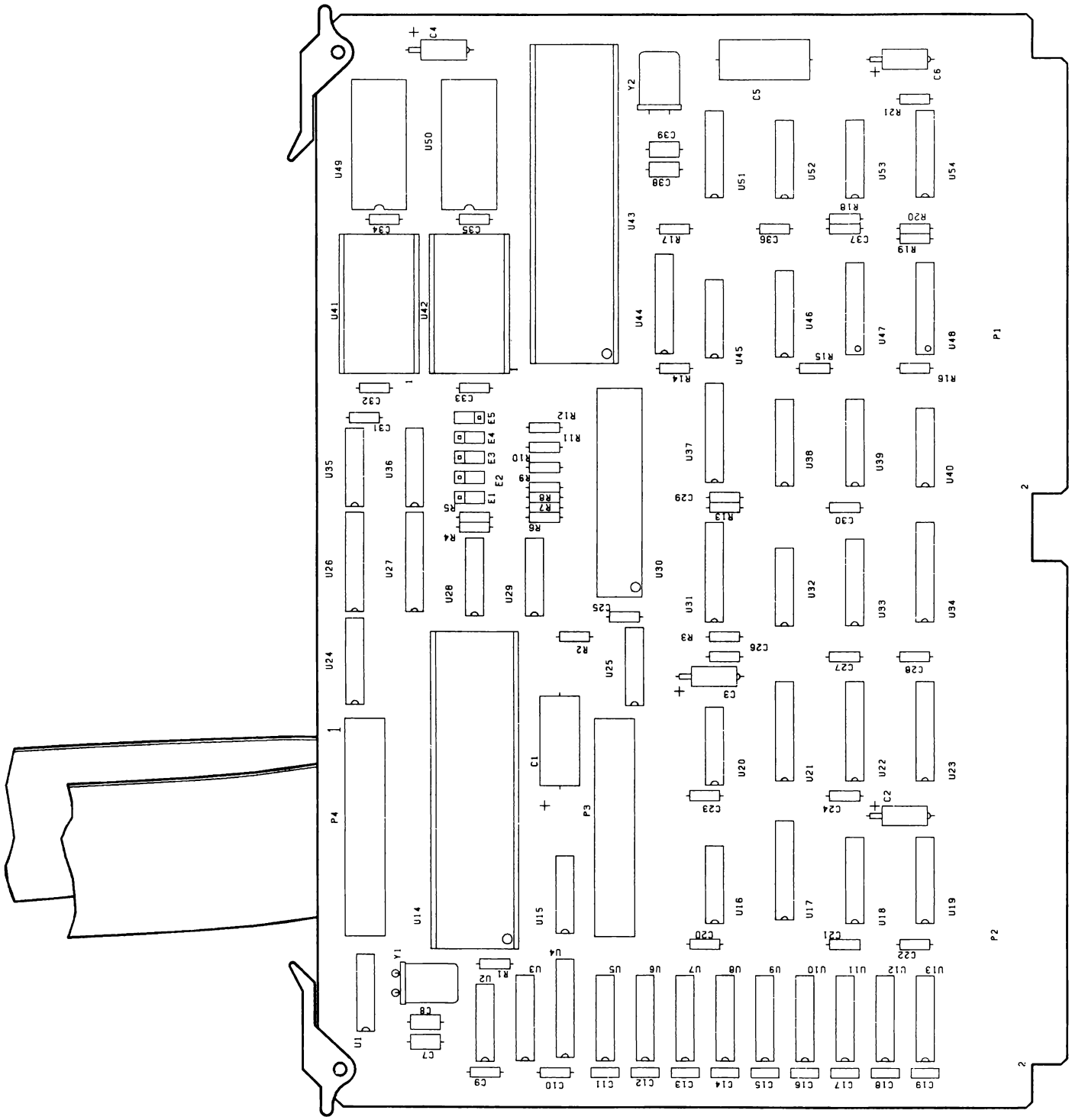


Figure 1-1 TMS7000 Emulator Board -- PN 2311080-0001

1.1.2 Board Installation.

CAUTION

BEFORE INSTALLING OR REMOVING ANY BOARD, TURN OFF THE POWER TO THE XDS UNIT.

The XDS Model XX Installation and Operation Guide describes the procedure for installing or removing boards from the XDS unit. Refer to the manual appropriate for the XDS Model you are using. If an emulator board or board set is currently installed in the XDS, it must be removed before the TMS7000 emulator board can be installed.

Boards removed from the chassis should be stored so that they are protected from static discharge. Erase the board information on the chassis configuration label for each circuit board removed.

For the TMS7000 Emulator board, enter the following information, as given in Table 1-1, on the chassis configuration label.

Table 1-1 Chassis Configuration Label Information

Block Title	Information to be Entered
PWB Description	TMS7000 EMU
Part No	2311080-0001
Rev	ENTER REVISION LETTER FROM TMS7000 EMU BOARD.

Complete the installation according to the instructions in the appropriate XDS installation and operation guide.

CAUTION

DO NOT OPERATE THE XDS UNIT WITH THE FRONT PANEL REMOVED. THE FRONT PANEL IS REQUIRED FOR PROPER AIR CIRCULATION AND COOLING OF THE CIRCUIT BOARDS. THE FRONT PANEL IS ALSO REQUIRED TO PREVENT LEAKAGE OF RFI/EMI RADIATION.

Restore power to the XDS unit. Then wait at least eight seconds before you activate the monitor. Activate the monitor by entering two carriage returns from the terminal keyboard. The screen displays the following:

```
                    TEXAS INSTRUMENTS

                TMS7000   XDS    VERSION 1.0.0

  COMMANDS:
   INIT      IM        DR      RUN       BP      TR      HOST   IMP
   IPC       DM        MR      CRUN      BPM     TRM     IHC    IMD
   IPORT     MM                SS                TRIX    UL     ID
   ICC       FILL              SRR       SIB     SOR     DL     BGND
   RCC       FIND

   RESTART   XA        ARM     DPS       SSB     IT      LOG    GRUN
   BLK       XRA       DISARM  DHS       CSB     DT      SNAP   TRUN
   EXP                 STOP    DTS       DSB             HELP   GHALT
                                       CASB                   THALT
  VARIABLES:
   PC        A         R       C         Z       ROM
   ST        B         P       N         I
   SP
?
```

If the monitor does not respond with the proper display, check the installation of the TMS7000 Emulator board. Refer to the appropriate XDS installation and operation guide to ensure correct connection to the terminal.

1.1.3 Target Connector.

The target connector is permanently connected to the target cables and does not require additional customer installation. The target connector uses an Augat socket to interface to the target system. A spare socket is supplied with the emulator and should be safeguarded for future use. The target connector should be handled with care at all times.

SECTION 2

HARDWARE FEATURES

2.1 INTRODUCTION

The emulator operates primarily with the emulator software that is referenced in the XDS TMS7000 Emulator User's Guide. The XDS Installation and Operation Guide discusses the hardware features and connections. The hardware features are highlighted below:

1. POWER SWITCH: Turns on power to the unit. (Not applicable for the XDS Model 11)

2. POWER LIGHT: Lights when power is applied to the unit.

3. RESET SWITCH: Returns emulator to control mode and regains synchronization with the system clock.

4. STATUS LIGHTS: Indicates emulator status.

The status lights and power requirements are unique for each emulator and are discussed below for the TMS7000 Emulator.

2.2 Status Indicator Lights

The XDS has four status indicator lights controlled by the TMS7000 Emulator. The function of these lights is as follows:

1. Status Indicator #1 -- IDLE -- The idle light comes on when the emulator spins on an idle instruction in your program. The optional breakpoint/trace board must be installed in the XDS for the Idle light, to operate. The Idle indicator resets upon an interrupt or a breakpoint.

2. Status Indicator #2 -- INTERRUPT 1 LINE ACTIVE -- This light comes on when a level 1 interrupt is sensed on the INT1- pin. It will remain lighted only when a low level is present on the INT1- pin.

3. Status Indicator #3 -- INTERRUPT 3 LINE ACTIVE -- This light comes on when a level 3 interrupt is sensed on the INT3- pin. It will remain lighted only when a low level is present on the INT3- pin.

4. Status Indicator #4 -- RUNNING -- This light comes on and remains lighted when the emulator executes user code.

2.3 TARGET CONNECTOR

The target connector is installed in the target system in place of the processor to be emulated. The target system can be any circuit that incorperates one or more processors. The target connector pin assignments are provided in section 3. The target conndectoe does not require VCC from the target system.

2.3.1 Handling the Target Connector.

Because the pins are extreamly delicate, handle the target connector with extream care at all times. Take the following precautions when handling the target connector.

1. To prevent an accidental short when connecting or disconnecting the target connector, you should power down the target system and the XDS unit.

NOTE

The XDS may not operate correctly when the target connector is connected to a system that is not powered up.

2. When the target connector is not in use, the pins must be protected to prevent physical damage to the pins and the XDS unit resulting from electrical short circuits. You can protect the pins by using either the gray plastic pin cover supplied with the unit or non-conductive foam. Conductive material should never be used to protect the target connector pins, as this may cause operation problems with the emulator.

2.3.2 Target Connector Features.

The target connector incorporates the following features to simplify your task of working with the target connector and the emulator system.

1. The yellow dot on the target connector, references the location of pin 1. Figure 2-1 shows the location of the yellow dot with respect to pin 1.

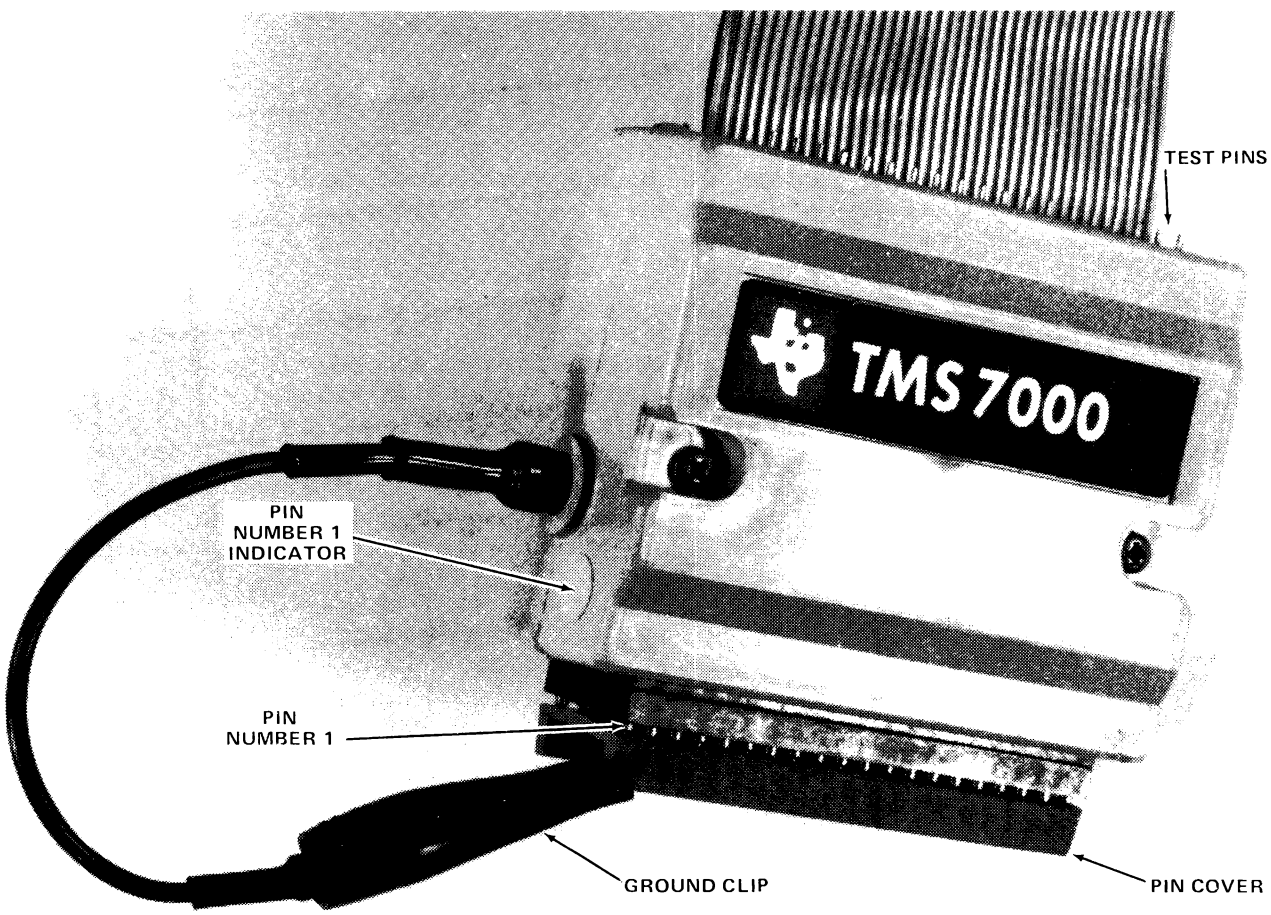


Figure 2-1 Target Connector With Pin Cover in Place

2. Test pins are located on the top of the target connector and correspond one-to-one to the pins that plug into the target system. The exception to this one-to-one configuration is pins 17, 18, and 25 which are open. You should use push-on test probes rather than clips or hooks.

3. A ground connection is provided at each end of the target connector. These connections mate with the ground cable provided with the emulator. This cable is screwed into the target connector and should be clipped to a ground post on the target system.

NOTE

To ensure a good ground of the target system to target connector, you must properly install the target connector grounding cable. This precaution is particulary important when the system is operating at high frequencies.

4. The target connector pin interface to the target system is a 40-pin socket. This socket can be removed from the target connector and replaced if a pin is broken. One extra socket is included with the emulator and should be safeguarded for this use. If you need more replacement sockets, you should use Auget #540-AG10D.

2.4 POWER REQUIREMENTS

Table 2-1 shows The DC power requirements for the TMS7000 Emulator board. You can use this information to calculate the total DC power requirements of the XDS system. When adding new boards to the system you should make this DC Power calculation to ensure that the power supply will not be overloaded. Refer to the appropriate XDS installation and operation guide for the power supply rating information. You can obtain the power requirements for the other circuit boards from their appropriate reference manuals.

Table 2-1 TMS7000 Emulator DC Power Requirements

+ 5 Volts (Amps)	+ 12 Volts (Amps)	- 12 Volts (Amps)
1.5	0.0	0.0

SECTION 3

EMULATOR SPECIFICATIONS

3.1 INTRODUCTION

This secton describes the following for the TMS7000 family:

1. Capacitor values for crystal inputs
2. Pin Assignments
3. Theory of Operation

3.2 Tank Capacitor Values for a Target Crystal

When using external crystals for clock inputs, you must install a capacitor from pin 17 or pin 18 to ground. Although the processor data book for the TMS7000 series processors recommends the use of 15pF tank capacitors on pins 17 and 18, this is not the case for the XDS. When using the XDS TMS7000 Emulator system, you should use the following capacitor values in your target system:

1. Pin 17 to Ground, 39pF
2. Pin 18 to Ground, 10pF

3.3 TMS7000 Family Pin Assignments

Table 3-1 shows the target connector pin assignments for the TMS7000.

Table 3-1 TMS7000 Target Connector Pin Assignments

PIN SIGNATURE	PIN NUMBER	I/O	DESCRIPTION
A0 (LSB)	6	IN	I/O Port A: General Purpose
A1	7	IN	Bidirectional Lines
A2	8	IN	
A3	9	IN	
A4	10	IN	
A5/RXD	16	IN	
A6/SCLK	15	IN	
B0 (LSB)	3	OUT	I/O Port B: General Purpose
B1	4	OUT	Output Lines
B2	5	OUT	
B3/TXD	37	OUT	
B4/ALATCH	38	OUT	
B5/RW-	1	OUT	
B6/ENABLE-	39	OUT	
B7/CLOCK OUT	2	OUT	
C0 (LSB)	28	I/O	I/O Port C: General Purpose
C1	29	I/O	Bidirectional Lines
C2	30	I/O	
C3	31	I/O	
C4	32	I/O	
C5	33	I/O	
C6	34	I/O	
C7 (MSB)	35	I/O	
D0 (LSB)	27	I/O	I/O Port D: kGeneral Purpose
D1	26	I/O	Bidirectional Lines
D2	24	I/O	
D3	23	I/O	
D4	22	I/O	
D5	21	I/O	
D6	20	I/O	
D7 (MSB)	19	I/O	

Table 3-1 TMS7000 Tkarget Connector Pin Assignments Continued

PIN SIGNATURE	PIN NUMBER	I/O	DESCRIPTION
INT1-	13	IN	Maskable Interrupt
INT3-	12	IN	Maskable Interrupt
RESET-	14	IN	RESET-
MC	36	IN	Memory Control
XTAL2/CLKIN	17	IN	Crystal input for control of internal OSC; input pin for external OSC or LRC networks
XTAL1	18	IN	Crystal input for control of internal OSC; leave open for external OSC.
VCC	25		No connection
VSS	40	IN	Ground reference

3.4 Theory of Operation of the TMS7000 Emulaotr

The purpose of this section will be to convey to an engineer or technician the general theory behind the emulator in order to fascilitate debug and repair of XDS 7000 emulators. In order to gain a full understanding of the discussion in this manual, the reader should obtain a copy of the TMS7000 emulator logic diagrams, P/N 2311082-9901.

3.4.1 OVERVIEW. The block diagram for the emulator is shown in figure 1. The TMS9996 microprocessor on the left hand side serves as the emulator's master controller. It communicates with the user at his terminal via one of the TMS9902's, and with the host computer (if there is one) via the other 9902. It stops and starts the TMS7041SE (system emulator chip) and tells it what information to fetch. It programs and retrieves information from the Breakpoint/Trace board via the system bus, P1 and P2. The 9996 runs out of the control program stored in the 27128 eproms, U41 and U42. The 4K X 8 rams, U49 and U50 serve as temporary data storage for the control program.

The TMS7041SE device on the right hand side of the diagram provides the run-time processor emulation seen by the user at the target connector. It is a special device with all of the normal pins found on a TMS7041 plus an additional address, data and control bus for emulator functions.

The 9996 can stop and start the 7041SE by means of the freeze logic. When the 7041SE is not running (frozen), the 9996 can request that the SE read from or write to areas in user memory or on-chip registers such as the PC, ST and SP. Communication between the SE and the 96 is performed via the LS299 serial to parallel shift register, U29. The 96 talks to the SE with its CRU instructions, and the SE sends and receives data via the SEDATA bus.

In order for the SE to know what the 96 wants it to do, a special group of 8-bit "tags" was developed which give the SE special instructions such as "read your pc and load it on to the sedata bus" or "store the following byte at address >7000". These tags are sent to the SE via the LS299 shift register, U21. When the SE is not running, its "freeze-" line is used as a data strobe to transfer data in and out of the SE. When the 96 wants the SE to start executing user code again, it will send out an "end of freeze" tag. Exact timing relationships and more detail on 7041SE operation can be found in Appendix A.

When the emulator is in "RUN" mode, i.e. the 7041SE is running user code and emulating the device, the Breakpoint/Trace card monitors what is on the 7041's internal address and data bus via the SEADDRESS and SEDATA bus. Because these busses are seperate from the user's address and data bus, complete transparancy is achieved with no additional loading. Even accesses to internal memory locations are sent out on the SEADDRESS and SEDATA bus to allow the B/T card to breakpoint and trace on these locations.

The emulator comes with 64K of D-RAM on board which serves two functions. The 7041SE has no rom on-chip, so rom is simulated in D-RAM. Also, the user is allowed to map in the D-RAM as memory expansion to take the place of target system memory. The parity logic flags the 96 whenever the SE gets parity errors on D-RAM accesses. A parity error will cause the SE to stop running and an error message to be relayed to the user at his terminal.

A special section of logic was added to allow the breakpoint/trace card to be stopped and examined even while the SE is running user code. This is referred to as the ARM/DISARM logic on the block diagram. This feature was added to aid users designing real timer controllers where it may cause problems to stop the processor in mid stream.

The 64K X 1 D-RAM at U13 allows a user to program so-called software breakpointswhich do not require that a breakpoint/trace card be installed. The ram monitorsthe SEADDRESS bus and can be programmed to breakpoint on any address, although monitor firmware only allows a user to program up to 10 breakpoints by this method.

The clock logic allows a user to select either the clock generated by the on-board oscillator chip (U1) or to select the target system clock. It also allows the selection of a divide-by-two or divide-by-four input. The 96 programs the selector, U24, to provide the input desired by the user.

The Run-On-Reset logic, (ROR), was designed to hold the SE in a frozen state until a reset was sensed at the target reset-line. At that point, the emulator would begin executing user code at the address in its PC. Due to code space limitations however, this feature is not presently being implimented.

The interrupt logic allows selection of either edge-only or both edge and level interrupt triggers for INT1- and INT3-. The jumpers at E1 and E2 are used to select which mode is desired. For NMOS parts, both edge and level triggers are specified, so the jumpers should go between pins 1 and 2. For CMOS emulation,

jumper E1 should go between pins 2 and 3 so that INT1- will be edge-only.

3.4.2 EMULATOR OPERATIONAL FLOW. There is a general sequence of events which occur during any emulator session. The flow goes something like this:

1. On power up, the 9996 initializes all cru-accessable locations, resets and freezes the 7041SE, and clears out control ram and 7041SE D-RAM. It then displays the power-up banner to the user's terminal and awaits the first command input. The emulator is now in the "control mode" state, because the 7041SE is halted and the 96 is running the show.

2. The user will then issue a variety of commands, the first of which is usually INIT. This command defines what type of processor the 7041SE will emulate, which clock is selected, how many external breakpoint bits will be used, and whether or not the clock is to be slower that 320KHZ. After the user inputs his parameters, the 9996 goes off and initializes the SE, B/T card and random logic to conform to the init selections. Other commands might be entered by the user to map in expansion ram, assemble code in ram, download code from a host, or many other functions. The 9996 responds to each command by performing the correct cru and memory operations to accomplish the goal of the command. Eventually, the user will get to the point where he is ready to put the emulator in run mode and execute his program. He may define locations at which the emulator is to halt by using the breakpoint commands , or he may tell the B/T card to trace certain memory accesses. Again, the 96 must tell the breakpoint or trace logic on which conditions it is to monitor or stop the SE.

3. When the RUN command is issued, the 96 has to go out and initialize the 7041SE to the proper state and then send the end of freeze tag. The SE will then begin executing user code, either out of target memory or on-board memory, and continue running until either a breakpoint is encountered or the user hits the key board. When the SE is executing user code, the emulator is said to be in "RUN" mode.

4. Once the processor stops, the user will enter emulator commands to find out what the flow of his program looks like or where a breakpoint occurred. He may then

change his program and try running it again.

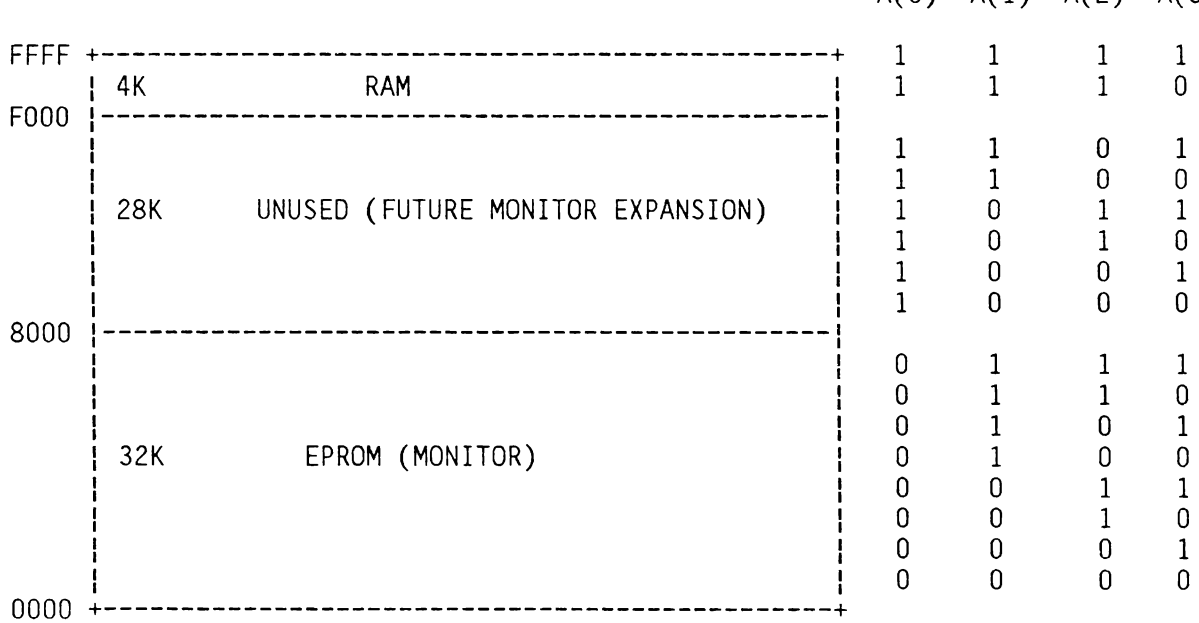
5. The rest of the emulator session will continue to consist of this alternation between RUN mode and CONTROL mode.

3.4.3 DESIGN ANALYSIS.

This following will go into in-depth analyses of each major block of logic in order to give the reader a more thorough understanding of the emulator's operation. References will be made to pages of the logic diagram, P/N 2311082-9901.

3.4.3.1 MEMORY MAP.

The 9996 control processor, (U43), executes the control code stored in the 27128 16K X 8 eproms (U41 and U42). It uses the 4K X 8 static rams at U49 and U50 for temporary data storage. The chip select lines to the ram and rom are decoded by the pal at U44. Below is a memory map of the 9996 memory space.



The eproms and ram chip select signals are decoded by the pal, U44, according to the following logic equations:

1. CS1 = MEMEN*(A(0)- + A(1)- + A(2)- + A(3)-).

2. CS3 = (A(15) + W/B-)*MEMEN*A(0)*A(1)*A(2)*A(3)

3. CS4 = (A(15)- + W/B-)*MEMEN*A(0)*A(1)*A(2)*A(3)

Memory cycles are qualified by MEMEN- going low before DBIN- or WE- go low.

3.4.3.2 CRU ADDRESS MAP.

The 9996 uses its serial I/O port, otherwise known as CRU, to set control bits which affect various blocks of logic on the emulator. CRU bits are addressed by the same address bus as memory locations, so there is a mechanism wy which the two types of accesses are identified. CRU cycles are differentiated from memory cycles by MEMEN- staying high while DBIN- or WE96- are low. CRU cycles also require that D(0) and D(1) be low. The CRU bit address map is given below for all signals found on the emulator board. Bits which address internal 9901 or 9902 bits are not included, since these can be found in the device data manuals. Also, bit addresses of com board and B/T board bits are not included unless they are brought directly to the emulator board via the backplane connectors. Address bits A(1) through A(5) are don't care bits in all cases.

9996 CRU ADDRESS BIT MAP

CRUBASE OR BIT	SIGNAL NAME	A(0)	A(6)	A(7)	A(8)	A(9)	A(10)	A(11)	A(12)	A(13)	A(14)	TYP
>0000	CRUIN9901	X	X	0	0	0	X	X	X	X	X	R
>0000	EN9901-	X	X	0	0	0	X	X	X	X	X	EN-
BIT 1	INT9902A-	X	X	0	0	0	0	0	0	0	1	R/W
BIT 2	INT9902B-	X	X	0	0	0	0	0	0	1	0	R/W
BIT 3	SEFRZQ-	X	X	0	0	0	0	0	0	1	1	R/W
BIT 4	RUNQ	X	X	0	0	0	0	0	1	0	0	R/W
BIT 5	PERRQ-	X	X	0	0	0	0	0	1	0	1	R/W
BIT 6	LNGBPQ	X	X	0	0	0	0	0	1	1	0	R/W
BIT 16	96PARCLR-	X	X	0	0	0	1	0	0	0	0	R/W
BIT 17	SBPR/W-	X	X	0	0	0	1	0	0	0	1	R/W
BIT 18	96CRUEN-	X	X	0	0	0	1	0	0	1	0	R/W
BIT 19	96FRZ	X	X	0	0	0	1	0	0	1	1	R/W
BIT 20	96ERST	X	X	0	0	0	1	0	1	0	0	R/W
BIT 21	96ROR	X	X	0	0	0	1	0	1	0	1	R/W
BIT 22	SFTHLD	X	X	0	0	0	1	0	1	1	0	R/W
BIT 23	962XCLK	X	X	0	0	0	1	0	1	1	1	R/W
BIT 24	96SECLK	X	X	0	0	0	1	1	0	0	0	R/W
BIT 25	SSTPQ	X	X	0	0	0	1	1	0	0	1	R/W
BIT 26	ROROK	X	X	0	0	0	1	1	0	1	0	R/W
BIT 27	SOFTBP	X	X	0	0	0	1	1	0	1	1	R/W
BIT 28	MC	X	X	0	0	0	1	1	1	0	0	R/W
BIT 29	LD299	X	X	0	0	0	1	1	1	0	1	R/W
BIT 30	LSTEVT-	X	X	0	0	0	1	1	1	1	0	R/W
BIT 31	-------	X	X	0	0	0	1	1	1	1	1	R/W
>0040	CRUIN9902A	X	X	0	0	1	X	X	X	X	X	R
>0040	EN9902A-	X	X	0	0	1	X	X	X	X	X	EN
>0080	CRUIN9902B	X	X	0	1	0	X	X	X	X	X	R
>0080	EN9902B-	X	X	0	1	0	X	X	X	X	X	EN
>00B0	BPREG	X	X	0	1	1	X	X	X	X	X	R
>00B0	LLDEC-	X	X	0	1	1	X	X	X	X	X	EN
>0100	TMA09	X	X	1	0	0	X	X	X	X	X	R
>0100	LLDTC-	X	X	1	0	0	X	X	X	X	X	EN
>0140	EXPMEMI-	X	X	1	0	1	X	X	X	X	X	R
>0140	EXPMEMO-	X	X	1	0	1	X	X	X	X	X	EN
>0180	FLGS-	X	X	1	1	0	X	X	X	X	X	EN
>0180	LOCHLT	0	X	1	1	0	X	X	X	X	X	R
>0180	TR/WCTL-	X	0	1	1	0	0	0	X	X	X	EN
>01B0	TBDIN	X	X	1	1	1	X	X	X	X	X	R
>0190	BITSL-	X	0	1	1	0	0	1	X	X	X	EN
>01A0	EXPCRU-	X	0	1	1	0	1	0	X	X	X	EN
>01B0	ALTCNTRL-	X	0	1	1	0	1	1	X	X	X	EN
>0380	TDBITS-	X	1	1	1	0	0	0	X	X	X	EN
>8180	COMREG	1	X	1	1	0	X	X	X	X	X	EN
>8180	REGIN	1	X	1	1	0	X	X	X	X	X	R

3.4.3.3 SIGNAL DEFINITION.

Below is a list of important signals used by the 9996. Brief definitions are given for each.

CRUIN When the 9996 performs a TB or STCR instruction, the input CRU bit is selected and demultiplexed onto this line, which is fed back directly to the 96.

INTREQ- When an interrupt is detected by the 9901 systems interface, it signals the 96 by pulling this line low.

IC096 - IC396 These lines tell the 96 what level interrupt is pulling INTREQ- low.

D0 - D15 This is the 9996 data bus.

XTAL1, XTAL2 These are the inputs for the crystal which activates the clock on board the 9996.

POR- This signal resets the 9996 and could be pulled by a power-on reset, the front-panel reset button, or an Ampl reset.

MEMEN- This signal preceeds DBIN- and 96WE- going low to identify memory accesses.

A0 TO A15 This is the 96 address bus, used for both memory and cru accesses. On CRU output cycles, A15 is used as the data bit. An SBO instruction causes A15 to go hi and an SBZ forces it low.

CLKOUT1, CLKOUT2 Two phases of the 96 system clock used to generate a 3 MHZ clock for the 9902's.

CRUCLK A low to hi transition on this line strobes in valid CRU data on a read operation, and a hi to low transition strobes out valid write data.

W/B- If the 96 wants to access both rams, then this signal will be high during the cycle. If only one, then this signal is held low and A(15) decides which ram is accessed.

DBIN- Used by the 96 to enable the rams on to the data bus during a read cycle.

WE96- Used by the 96 to tell the rams when data is valid on

the bus during a write cycle.

3.4.4 9902 ASYNCHRONOUS COMMUNICATION CONTROLLERS - U47, U48.

The TMS9902s at U47 and U48 are used by the 9996 to communicate with EIA ports A and B respectively on the back of the XDS chassis. The enable lines to the 9902s are decoded by LS138 at U38. Specific bits inside the devices are then addressed by address lines A10 - A14 on cru cycles. Specific information concerning the RS-232 protocal and 9902 operation can be found in the 9902 data manual.

3.4.5 9901 PSI - U30.

The TMS9901 at U30 is used by the 9996 to multiplex cru bits and decode 9902 interrupts. Address lines A10 through A14 are used to address each port on the 9901 during cru cycles. Some of the ports on the 9901 are used as input only and others are used as I/O. The enable line to the 9901 is selected by the LS138 at U38.

3.4.6 CRU INPUT DEMULTIPLEXER - U39.

This LS251 selects one of 8 cru input bits to be multiplexed on to the CRUIN line to the 9996. Address lines A7 through A9 decide which bit is selected. CRUIN9901, CRUIN9902A and CRUIN9902B are the read input bits from the 9901 and 9902s, while BPREG, TMA09, EXPMEMI-, and TBDIN are read bits from the B/T and Comm boards. CRUMUX is a comes from the pal at U44 and is either LOCHLT if A0 is low or REGIN if A0 is hi. LOCHLT is a cru bit which comes from the memory expansion card and REGIN is the output bit of the LS299 shift register at U21. REGIN is the bit used by the 96 to read back data from the 7041SE.

3.4.7 ENABLE SELECTOR LOGIC - U38, U33.

The LS138 selectors at U33 and U38 are used to enable various cru devices both on the emulator and on the B/T and Comm boards. EN9901-, EN9902A-, and EN9902B- are self explanatory. All other enable bits perform functions on the B/T and comm boards which are not in the scope of this document.

3.4.8 ADDRESS DECODE PAL - U44.

The pal at U44 serves to generate chip select signals to the control ram and rom and also funnel the input from the com register, U21 back to the 96. CS1- , CS3- and CS4- have previously been defined as chip select signals for the control ram and rom. CRU96 is a shift clock to the LS299 and is defined by the logic equation: CRU96 = (DBIN + CRUCLK)*MEMEN-. COMREG enables CRU96 and is defined as COMREG = FLGS*A0. CRUMUX was defined earlier as a multiplexed input bit which is either LOCHLT from the comm board or REGIN, the output bit of the LS299.

3.4.9 LS299 COMMUNICATION SHIFT REGISTER - U21.

This parallel to serial shift register serves as the comm link between the 9996 and the 7041SE. When the SE has been frozen, the 96 will shift in tags and data to the LS299 by cru operations. The signal LD299 is a cru bit from the 9901 and is used to load the register from the data bus. When LD299 is low, the register will shift right each time a COMCLK is received, thus allowing the register to be loaded and unloaded via cru. SEBOE- is an enable signal from the 7041SE which tells the register when to get on and off the bus. This prevents the D-RAMs and Comreg from being on the bus at the same time.

3.4.10 TMS4164 D-RAM BANK U6 - U13.

The 64K X 1 d-rams serve as the memory expansion and simulated rom area for the 7041SE. The SE has no rom on chip, so this is simulated in d-ram. Also, if a user maps in memory expansion, the d-rams are accessed instead of target memory. The Ras- and Cas- signals to the rams are generated internally by the 7041SE. RASSTP is a cru bit set by the 96 to temporarily shut off ras and cas to the rams when the clock source for the SE is being switched. This prevents data from being lost in ram. SEDOE- enables the ALS573 driver latch at U17 on and off the bus. This is another signal generated by the SE which prevents the Comreg and d-rams from being on the data bus at the same time.

3.4.11 PARITY LOGIC U5,U17,U16,U20,U25.

During every write access to the 7041SE's D-RAM bank, a bit is stored in the parity ram at U5 which is dependent on how many ones are in the data byte being written. The signal BADPAR which is input to the I bit of the 74S280 at U16 will force the output of the parity generator to be the opposite of that expected. For example, if a data byte of >01 is written, PAREVEN will go high because the number of ones in the data byte is ODD. PARODD is the opposite of PAREVEN and is the bit which is stored in the

parity ram. Therefore, we would have stored a 0 in U5 on this occasion. When the data is read back, BADPAR will go to the opposite value of that which was stored in the parity ram, in this case it will go to a 1. With BADPAR being a one and the data byte being read back as >01, the PAREVEN line will go high since the number of ones input to the S280 is even. If PAREVEN is a one on the read cycle, no parity error will result as can seen by looking at U25. PERR goes high when a parity error is found, and this will not happen unless PAREVEN is a 0. Because PAREVEN went high when we read back >01, no parity error occured. If we had incorrectly read back a value of >00, PAREVEN would have gone low and caused a parity error. PERR is latched at U28 and fed back to the 9901 as a cru bit for the 9996 to read. 96PARBAD is a signal used only in diagnostics to force parity errors and is always a low in normal operation. 96PARCLR- is a cru bit set by the 9996 to clear a previously sensed parity error.

3.4.12 SOFTWARE BREAKPOINT LOGIC U2,U3,U4,U15,U45.

The D-RAM at U3 is used by the 9996 to force breakpoints based on SE address bus conditions. The signals SBPDIN and SBPR/W- are both cru bits from the 9901 which the 96 uses to program the ram. If the 96 wants to cause a breakpoint to occur at a particular address, it sets SBPR/W- low, does a SBZ at SBPDIN, and then does an access (a read or write) at the address in question. This will store a zero in U3 at the desired address. SBPR/W- is then set back high. When the SE accesses this address again while running the user's program, the zero will be read out onto LNGBP-, causing LSTEVT- to go low after a certain timing delay. LSTEVT- is an open collector signal shared by the software breakpoint logic and the B/T card to cause the SE to stop. LNGCAS- is an artificially generated CAS- to the D-RAM. It was necessary to use a signal other than SECAS- because the SE shuts off SECAS- when doing target or on-chip accesses. This would have kept us from setting breakpoints when the user had mapped in his target system memory or when the breakpoint was set on a register file location. LNGCAS- is clocked on H2 which allows LSTEVT- to be enabled on the right clock edge. AFRZ- serves to "freeze" the cas address at the output of U4 to allow U3 enough time to cause the breakpoint to be recognized. The discussion of how LSTEVT- causes the SE to stop and B/T card to suspend will be given in the section on the RUN/HALT logic.

3.4.13 RUN/HALT LOGIC U51-U54.

The purpose of the run/halt logic is to synchronize the stopping and starting of the breakpoint/trace card as well as

signalling the SE when a breakpoint has been detected. STOP is a signal which is generated to cause both the SE and the B/T card to stop. The logic equation is STOP=PERRQ + SOFTBP-*LSTEVT. This means that parity errors will stop both the SE and the B/T card anytime, whereas if SOFTBP is a one, LSTEVT- will be masked off and not cause the SE to stop. SOFTBP is used by the 9996 to stop the B/T card without stopping the SE. This is used in the ARM and DISARM commands which allow a user to inspect his trace buffer and set breakpoint conditions without causing the SE to cease executing the user's program.

In the normal case where both the SE and B/T will be stopping at the same time, LSTEVT- goes low causing STOP to go high. STOP is fed back to the freeze logic which then halts the SE. When the SE stops running, the RUN line goes low. RUN is funneled back to U51 as RUNQ which causes STOPBTQ- and SUSPEND- to go low, thus stopping the B/T card. The B/T card is started up again when the SE starts running. RUN goes high, causing RUNQX- to go low, causing STOPBT and IGATE to go low, causing SUSPEND- and STOPBTQ- to go high which starts up the B/T card.

In the alternate run mode, also known as ARM, SOFTBP is turned on, thus preventing LSTEVT- from causing STOP to go high. Instead, LSTEVT- will cause SFTBP- to go low, causing SHALT- to go low. SSTP will then go high, causing STOPBT and IGATE to go high causing STOPBTQ- and SUSPEND- to go low, thus stopping the B/T card. The SE continues running since STOP never went high forcing a freeze. After the B/T card has been stopped, the 96 gains control over it by setting SFTHLD high which breaks the SSTPQ feedback path from U54 to U52, but keeps IGATE high through U53. This will hold SUSPEND- low until the 96 sets SFTHLD low, thus restarting the B/T card.

3.4.14 FREEZE LOGIC U26,U27,U35.

The purpose of the freeze logic is to define the conditions under which the SE will be halted, and synchronize the starting and stopping with other events. When the SE is running and a breakpoint or parity error occurs, STOP will go high. After the RUN line has been high for at least 2 clock cycles, SEFRZ- will go low, causing the SE to stop. The 9996 will then use the SEFRZ- line as a data strobe by toggling 96FRZQ-. (See the section on the operation of the 7041SE.) Until the 96 pulls 96FRZQ- hi, the term on pins 1,11,12 and 13 holds SEFRZ- low. The term basically says that we have been frozen for at least one clock state and 96FRZ has not yet been set by the 96. Once the 96 pulls 96FRZ high, the term on pins 1,11,12,and 13 will never pull SEFRZ- low again until after the SE starts running. The term on pins 2 and 3 , ROROK*TRESETBQ-, is used to allow the SE

to remain frozen until a target reset is received. This logic is not used by the XDS monitor firmware at present due to a lack of code space. Otherwise there would be an RTR(Run on target Reset) command which would set the ROROK bit and set 96FRZ low. SEFRZ- would then wait until a target reset was sensed before going high and strobing in the end of freeze tag.

3.4.15 RUN ON RESET LOGIC U36,U35.

96ROR is a cru bit set by the 96 which will cause the output of the flip-flop at U36 to toggle. The output bit, ROROK, is used as an input to the freeze logic. Once this bit is set high, the SE will not enter run mode until a target reset is sensed. At present, this logic is not emplimented in the XDS monitor due to a lack of code space. IGATE is used to clear ROROK as soon as the SE starts running. Once the target reset is issued, TRESETBQ- goes low allowing SEFRZ- to go high and strobe in the end of freeze tag. Just before the SE goes into run mode, RESET- will go low and then release after the target reset is released.

3.4.16 SE RESET LOGIC U20,U25.

The 74S51 at U20 decides when to issue a reset to the 7041SE. 96ERST is a cru bit which the 9996 can set to force an SE reset at any time. TRESET comes from the target and is enabled by TRESETEN. The logic equation is TRESETEN = (ROROK + RUNQ)*SEFRZQ-. This says that once the processor has been running and not frozen for at least one clock state, or if the run on reset bit is set and the processor is ready to enter run mode, then target resets will be enabled.

3.4.17 INTERRUPT EDGE/LEVEL LOGIC U31,U45,U46,U37.

The purpose of this logic is to let the user select between edge only or edge and level triggered interrupts. When the target interrupt lines are routed directly to the 7041SE, both edge and level interrupts will be recognized. The purpose of the additional logic is to allow interrupts to the SE only when a high to low transition on one of the external interrupt lines occurs. Once the interrupt is passed on to the SE, it is cleared until another low going edge is detected. Jumpers E1 and E2 are used to select between the two types of interrupts. PINT1- and PINT3- are the edge only interrupt signals, while TINT1- and TINT3- are the straight through interrupt lines.

3.5 CLOCK LOGIC U1,U24,U28

U1 is an NMOS clock oscillator chip whose frequency of oscillation is controlled by the crystal at Y1. The tank capacitors C7 and C8 help the oscillator to come up oscillating at the crystals fundamental frequency. 96SECLK is a crubit which selects the on-board oscillator when it is a one, and the target oscillator when it is a zero. 962XCLK selects a divide by 4 clock when it is one, and a divide by 2 clock when it is zero.. The flip flop at U28 does the actual "clock division". U24 serves as the selector between the 4 types of clocks available, i.e. on-board/2, on-board/4, target/2, and target/4.

3.5.1 BREAKPOINT/TRACE INTERFACE U18,U19U22,U23,U34.

The SEADDRESS bus is driven out on to the motherboard by latches U23 and U34. The MSbyte is latched first by U18 and U19 on the low going edge of H1, and then both LSbyte and MSbyte are clocked out to the motherboard on the hi going edge of H1.

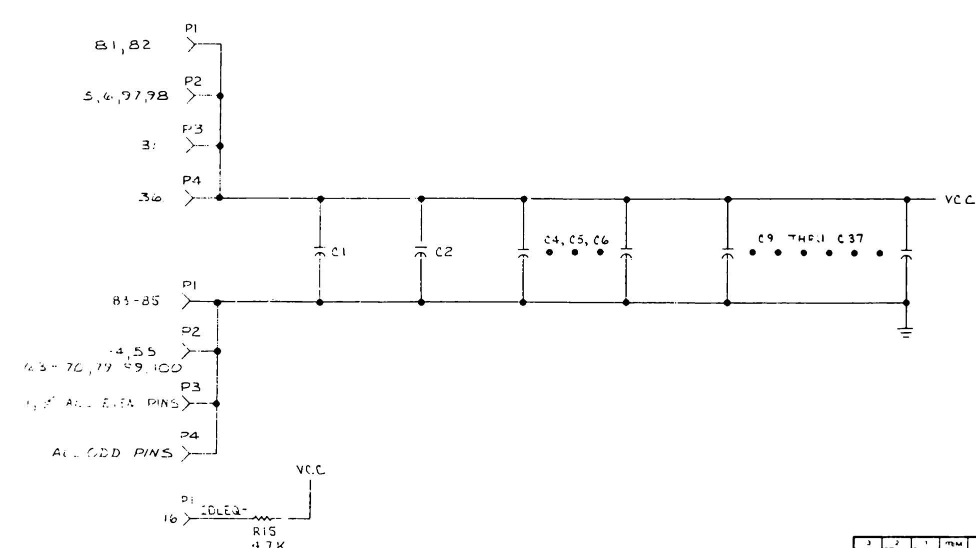
APPENDIX A

TMS7000 Emulator Schematics

NOTES UNLESS OTHERWISE SPECIFIED
1. ALL DEVICE TYPES ARE PREFIXED WITH SN74.
2. VCC IS APPLIED TO PIN 8 OF ALL 8-PIN IC'S, PIN 14 OF ALL 14-PIN IC'S, PIN 16 OF ALL 16-PIN IC'S, PIN 20 OF ALL 20-PIN IC'S, ETC.
3. GROUND IS APPLIED TO PIN 4 OF ALL 8-PIN IC'S, PIN 7 OF ALL 14-PIN IC'S, PIN 8 OF ALL 16-PIN IC'S, PIN 10 OF ALL 20-PIN IC'S, ETC.
4. DEVICE TYPE, PIN NUMBERS, AND REFERENCE DESIGNATOR OF IC IS SHOWN AS FOLLOWS:

LS00 AND LS04 = DEVICE TYPE
1, 2, AND 3 = PIN NUMBERS
U2 AND U14 = REFERENCE DESIGNATOR

5. RESISTANCE VALUES ARE IN OHMS.
6. RESISTORS ARE 1/4 WATT, 5%.
7. CAPACITANCE VALUES ARE IN MICROFARADS.



REV	DESCRIPTION	DATE	APPROVED
A	REVISED PER ENGR CHANGES		

FORMAL RELEASE

DWG NO 2311082 SH 1

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A
	SH	1	2	3	4	5	6	7	8	9	10

PARTS LIST

NEXT ASSY	USED ON
2311080	7119

APPLICATION

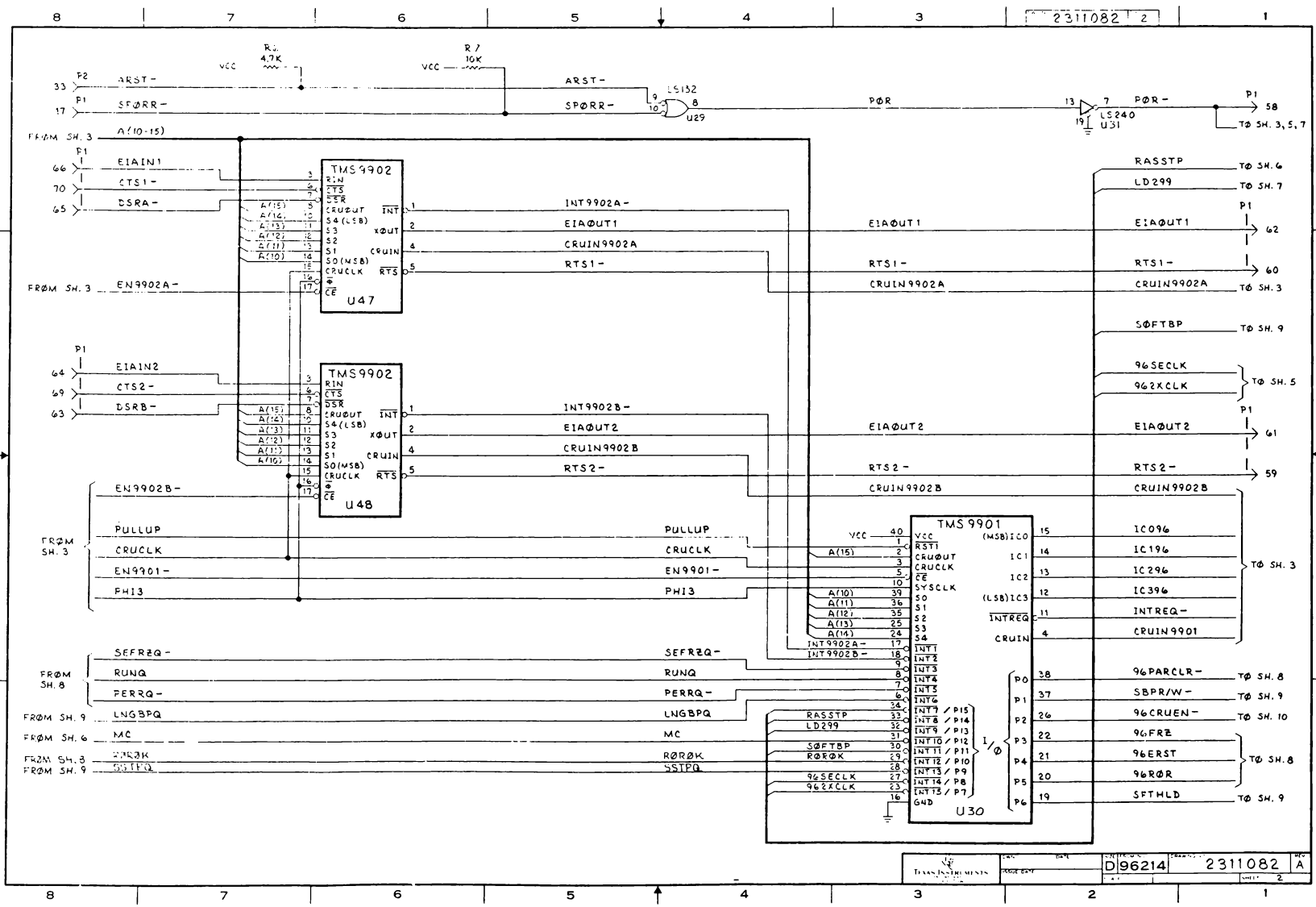
DWN C. KEELER 7-6-83
CHK A. KELLER

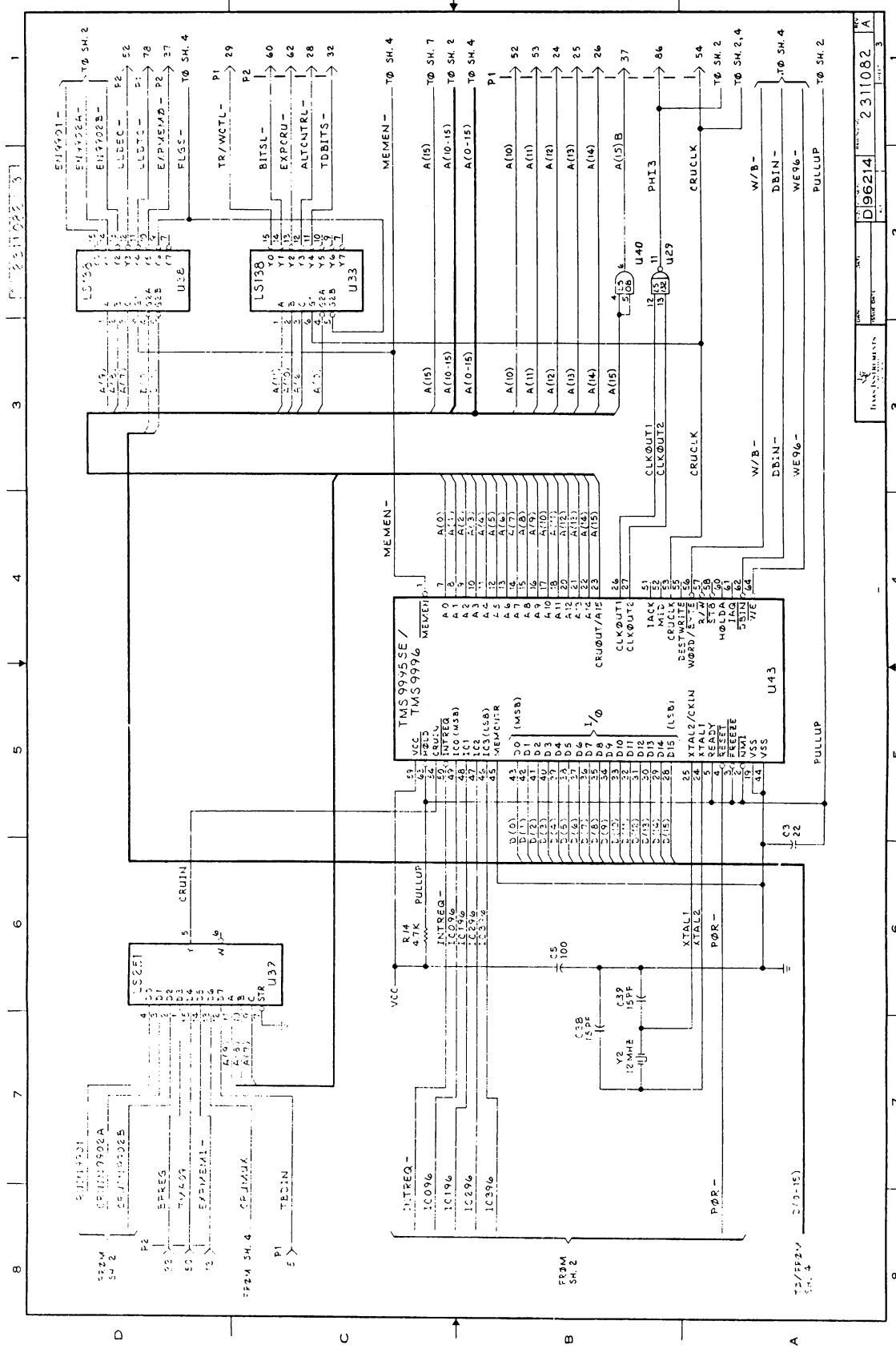
TEXAS INSTRUMENTS
SI-METRIC

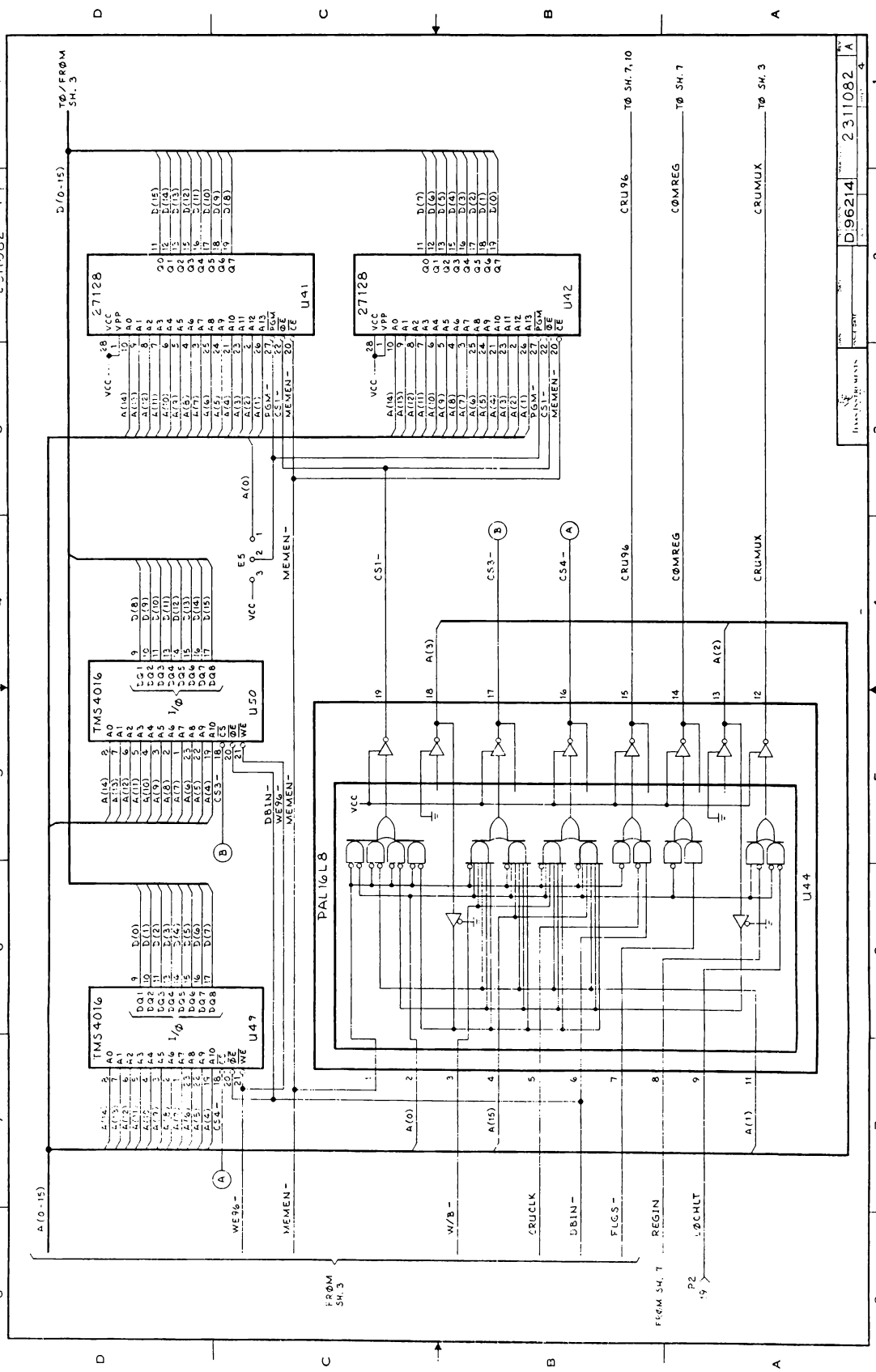
LOGIC DIAGRAM, TMS7000 EMULATOR

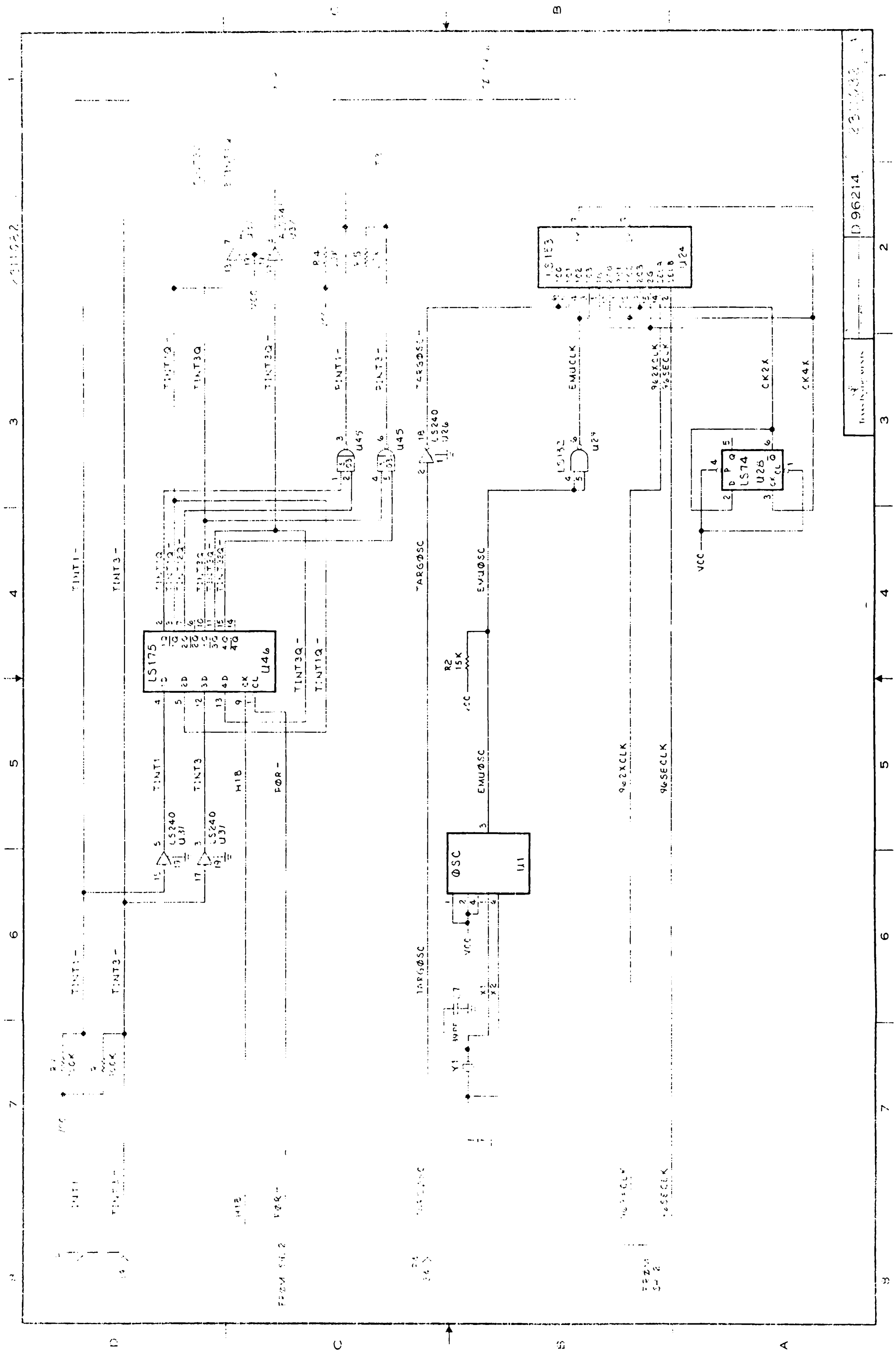
SIZE D FSCM NO 06668 DRAWING NO 2311082

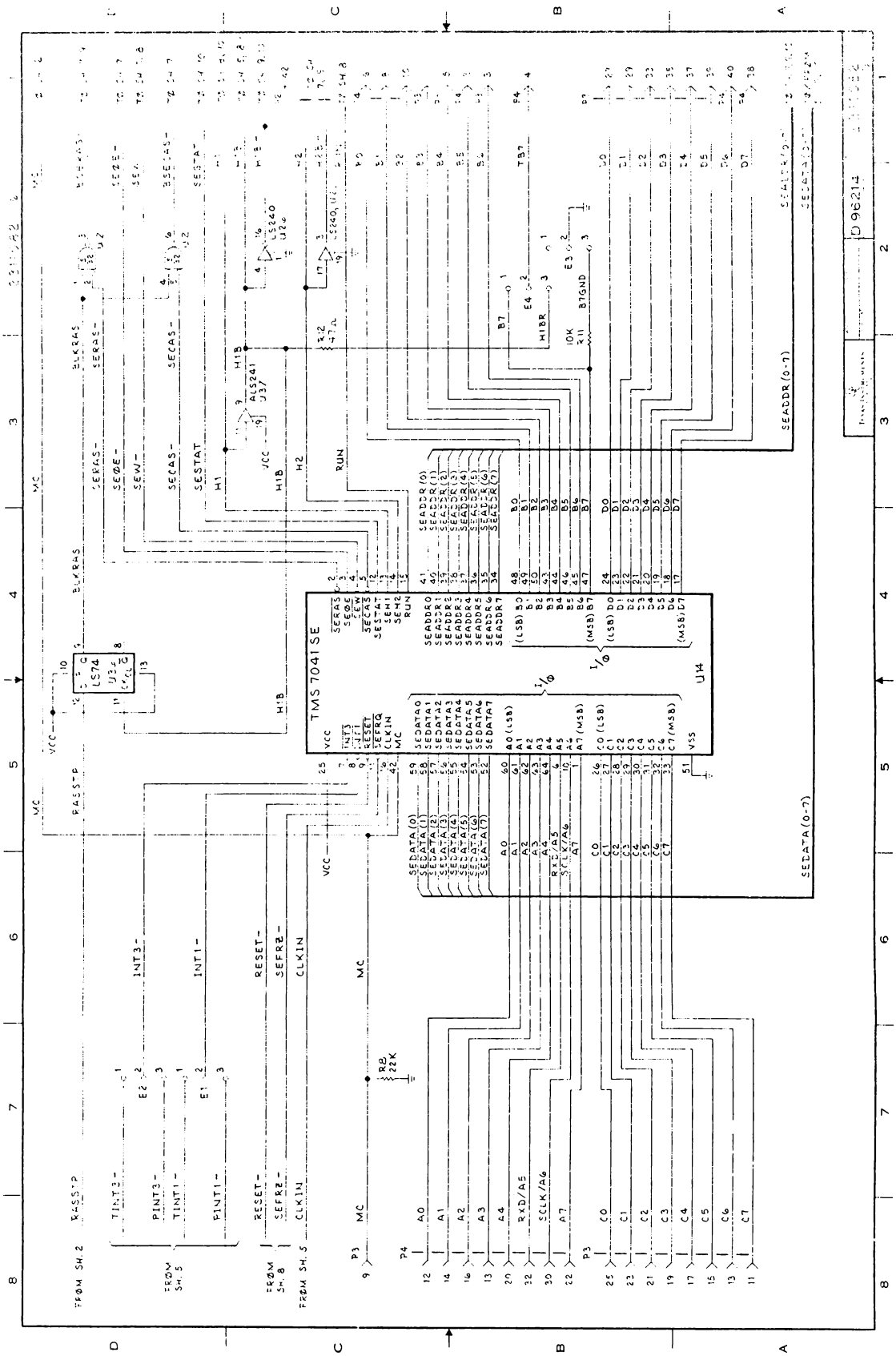
SHEET 1 OF 10

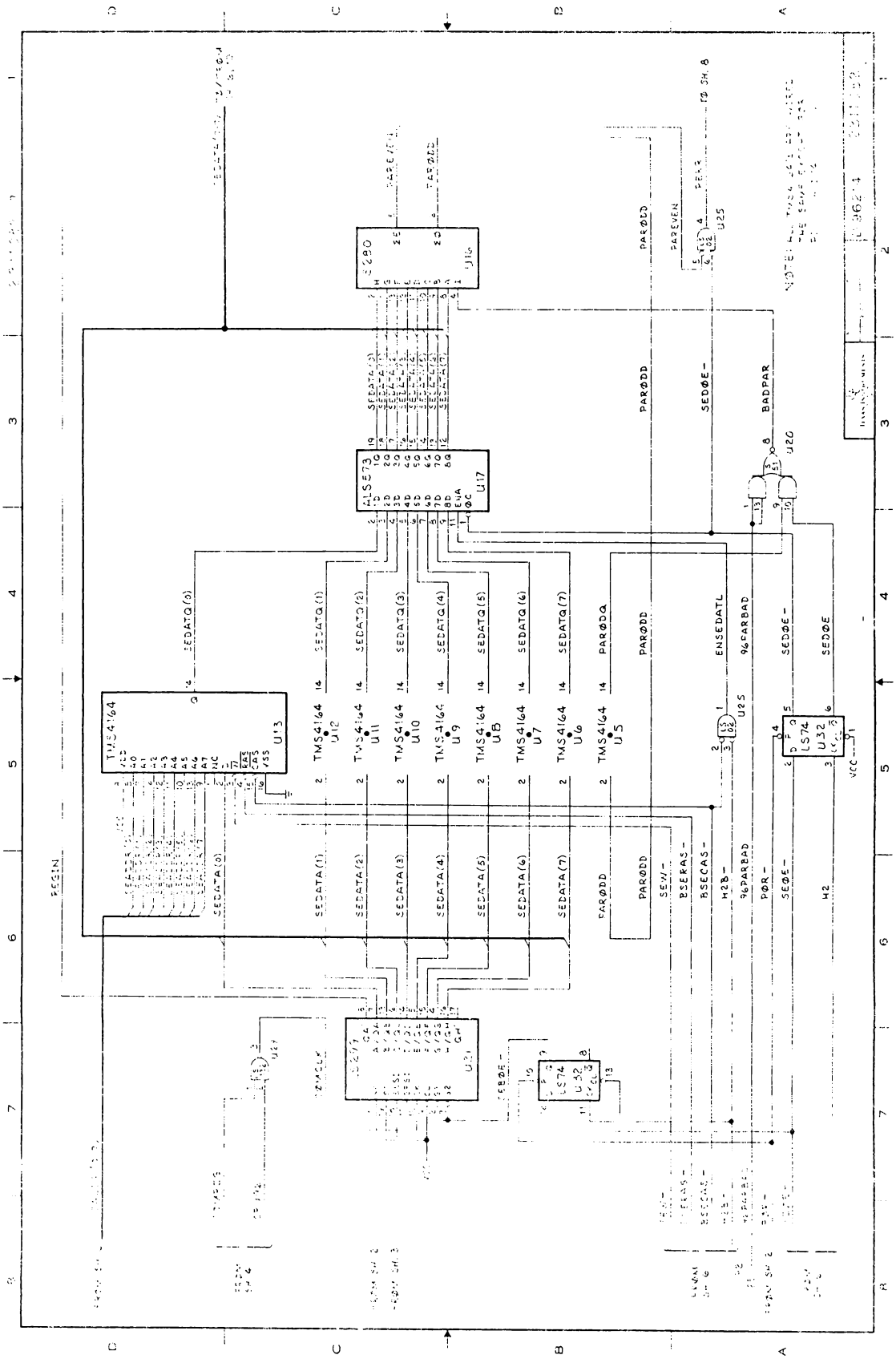

2311082 2
R6 4.7K
R7 10K
VCC
P2 33 ARST-
P1 17 SPØRR-
ARST-
SPØRR-
LS132 U29
PØR
LS240 U31
PØR-
P1 58
TØ SH. 3, 5, 7
FRØM SH. 3 A(10-15)
TMS9902 U47
P1 66 EIAIN1
70 CTS1-
65 DSRA-
INT9902A-
EIAØUT1
CRUIN9902A
RTS1-
FRØM SH. 3 EN9902A-
TMS9902 U48
P1 64 EIAIN2
69 CTS2-
63 DSRB-
INT9902B-
EIAØUT2
CRUIN9902B
RTS2-
EN9902B-
PULLUP
CRUCLK
EN9901-
PHI3
FRØM SH. 3
TMS9901 U30
SEFRZQ-
RUNQ
PERRQ-
LNGBPQ
MC
RØRØK
SSTPQ
FRØM SH. 8
FRØM SH. 9
FRØM SH. 6
RASSTP
LD299
SØFTBP
96SECLK
962XCLK
RASSTP TØ SH. 6
LD299 TØ SH. 7
EIAØUT1 P1 62
RTS1- 60
CRUIN9902A TØ SH. 3
SØFTBP TØ SH. 9
96SECLK
962XCLK
TØ SH. 5
EIAØUT2 P1 61
RTS2- 59
CRUIN9902B
IC096
IC196
IC296
IC396
INTREQ-
CRUIN9901
TØ SH. 3
96PARCLR- TØ SH. 8
SBPR/W- TØ SH. 9
96CRUEN- TØ SH. 10
96FRZ
96ERST
96RØR
TØ SH. 8
SFTHLD TØ SH. 9
TEXAS INSTRUMENTS
D96214
2311082 A
SHEET 2

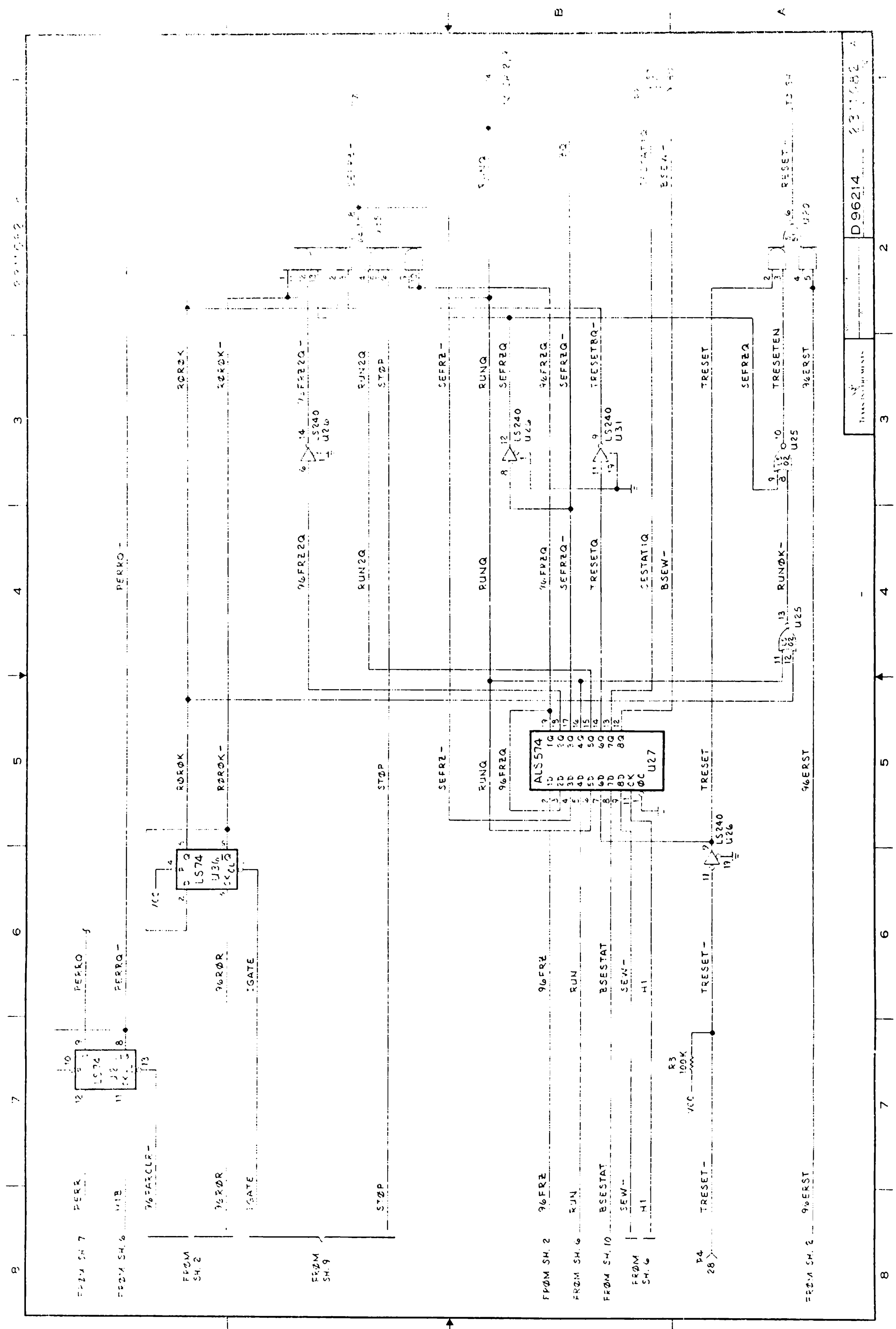


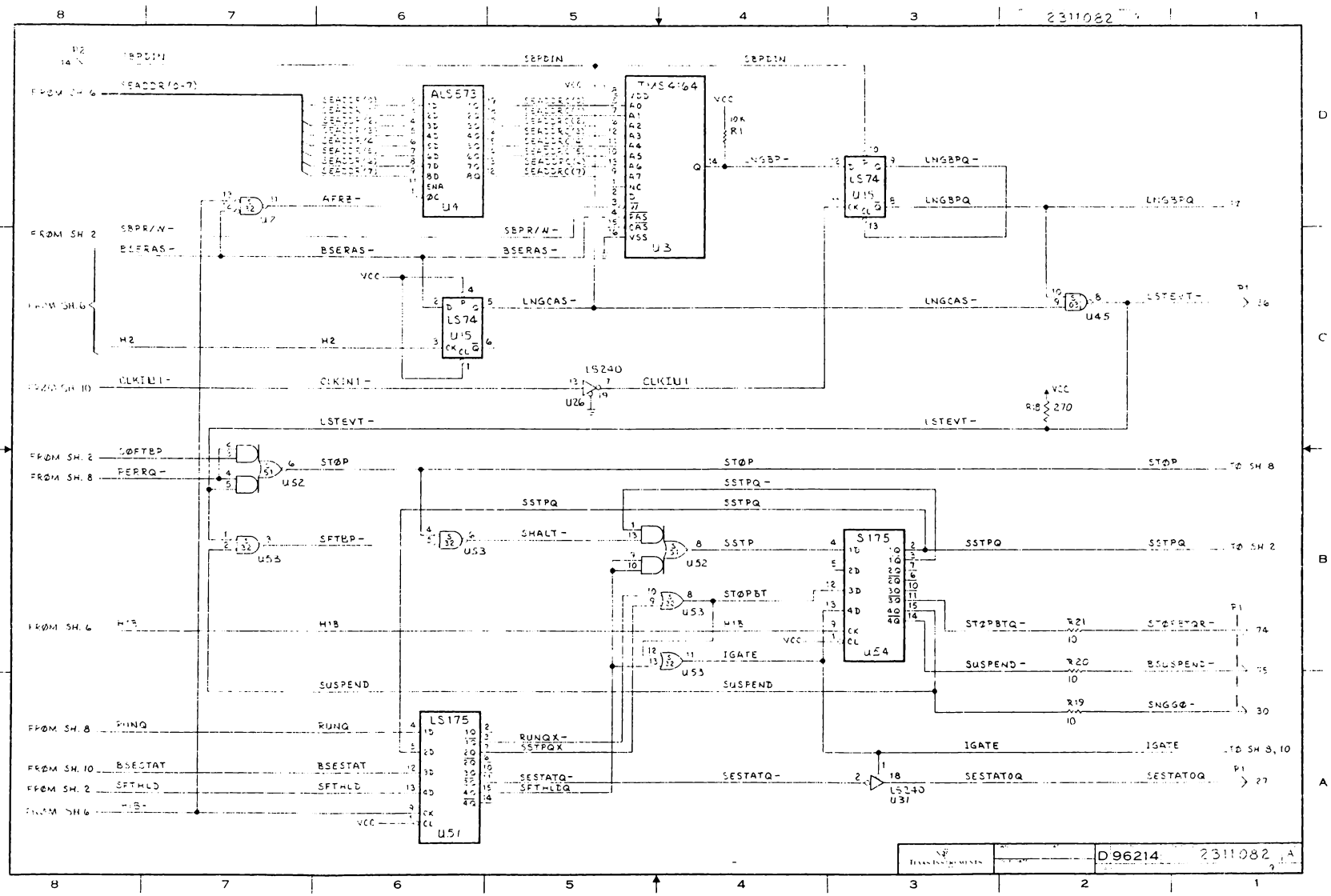

2311082 4
TØ/FRØM SH. 3
D/0-15)
27128
U41
U42
TMS4016
U47
U50
PAL16L8
U44
E5
MEMEN-
CS1-
CS3-
CS4-
DBIN-
WE9b-
A(0)
A(1)
A(2)
A(3)
A(15)
CRU96
COMREG
CRUMUX
TØ SH. 7,10
TØ SH. 7
TØ SH. 3
A(0-15)
WE9b-
MEMEN-
FROM SH. 3
WB-
CRUCLK
DBIN-
FLGS-
REGIN
FROM SH. 7
P2
LØCHLT
D96214
2311082
A

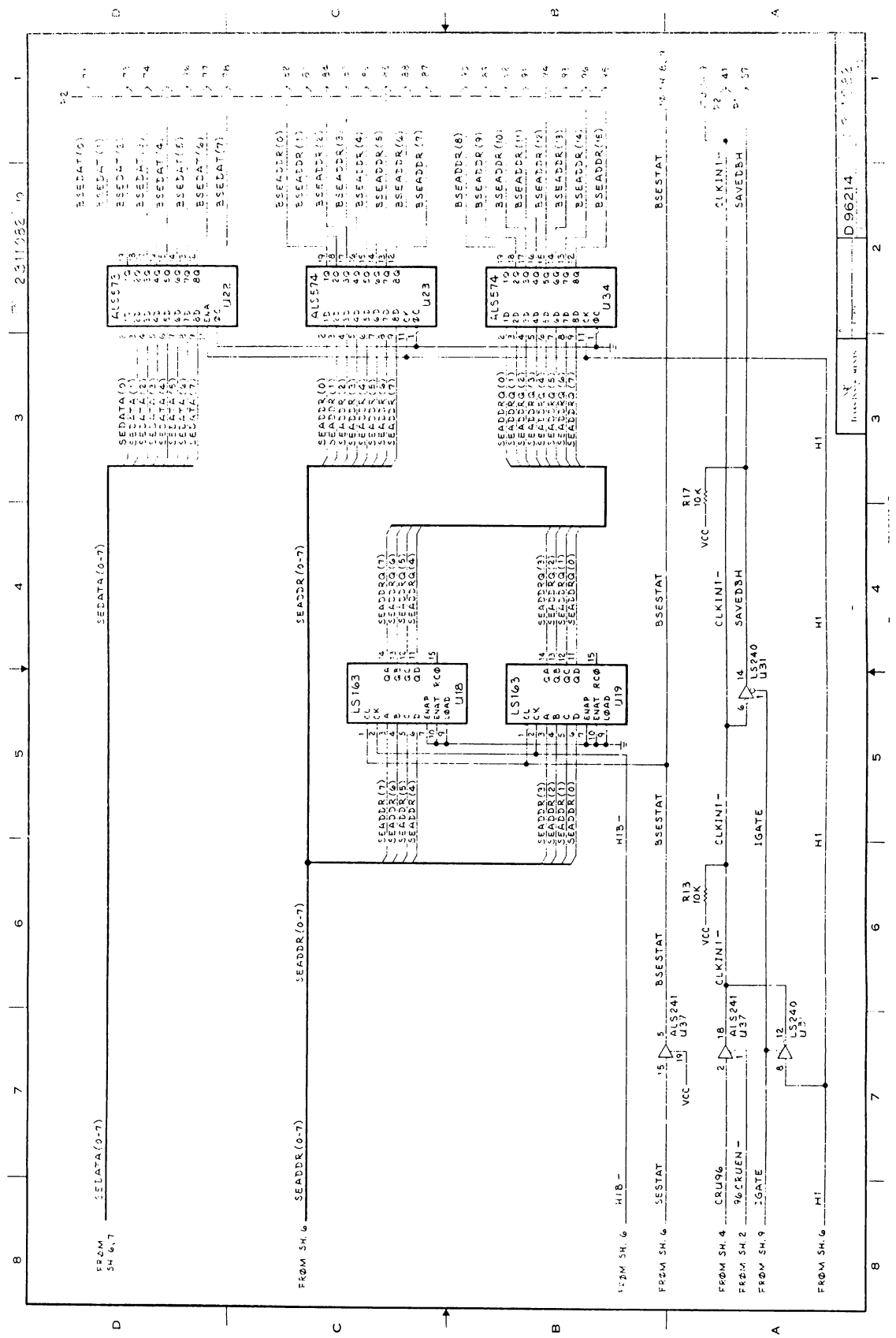

LS175
U46
LS240
U31
ØSC
U1
LS153
U24
LS74
U28
LS240
U26
LS132
U29
U45
EMUØSC
EMUCLK
TARGØSC
CK2X
CK4X
962XCLK
96SECLK
TINT1
TINT3
TINT1-
TINT3-
TINT1Q
TINT3Q
TINT1Q-
TINT3Q-
H1B
PØR-
R2
15K
VCC
Y1
D96214


TMS7041SE
U14
SEDATA(0-7)
SEADDR(0-7)
D96214
RESET-
SEFR2-
CLKIN
INT3-
INT1-
MC
RESSTP
H1B
H2
RUN
SERAS-
SECAS-
SEOE-
SEWE-
SESTAT
BLKRAS
BLKCAS
LS74
LS240
LS241
R8 22K
R12 47Ω
10K R11
B7GND
H1BR
FROM SH.2
FROM SH.5
FROM SH.8




D 96214
ALS574
U27
LS74
LS240
96FRZ
RUN
BSESTAT
SEW-
H1
TRESET-
96ERST
STØP
IGATE
96RØR
PERR
PERRQ-
RUNQ
SEFRZQ
SEFRZ-
RUN2Q
96FRZQ
TRESETQ
BSEW-
RUNØK-
TRESETEN
RØRØK
RØRØK-
R3
100K
VCC
FRØM SH. 2
FRØM SH. 6
FRØM SH. 10
FRØM SH. 9


2311082
SBRDIN
FROM SH 6
SEADDR(0-7)
ALS573
U4
TMS4464
U3
VCC
10K
R1
LNGBP-
LS74
U15
LNGBPQ-
LNGBPQ
FROM SH 2
SBPR/W-
BSERAS-
AFRZ-
U12
LNGCAS-
U45
LSTEVT-
TO SH 6
FROM SH 6
H2
CLKIN1-
CLKIN1
LS240
U26
CLKIU1
R18 270
FROM SH 2
SOFTBP-
FROM SH 8
FERRQ-
U52
STOP
TO SH 8
SSTPQ
SSTPQ-
U53
SHALT-
SSTP
TO SH 2
STOPBT
STOPBTQ-
R21
FROM SH 6
H1B
S175
U54
IGATE
SUSPEND-
R20
BSUSPEND-
SUSPEND
R19
SNGGO-
TO SH 8, 10
FROM SH 8
RUNQ
RUNQX-
SSTPQX
LS175
U51
FROM SH 10
BSESTAT
FROM SH 2
SFTHLD
SESTATQ-
SFTHLDQ
SESTATOQ
U31
D96214
2311082
A



TEXAS INSTRUMENTS

Creating useful products
and services for you.

March 1984
Revision *
1603838-9701
Printed in U.S.A.