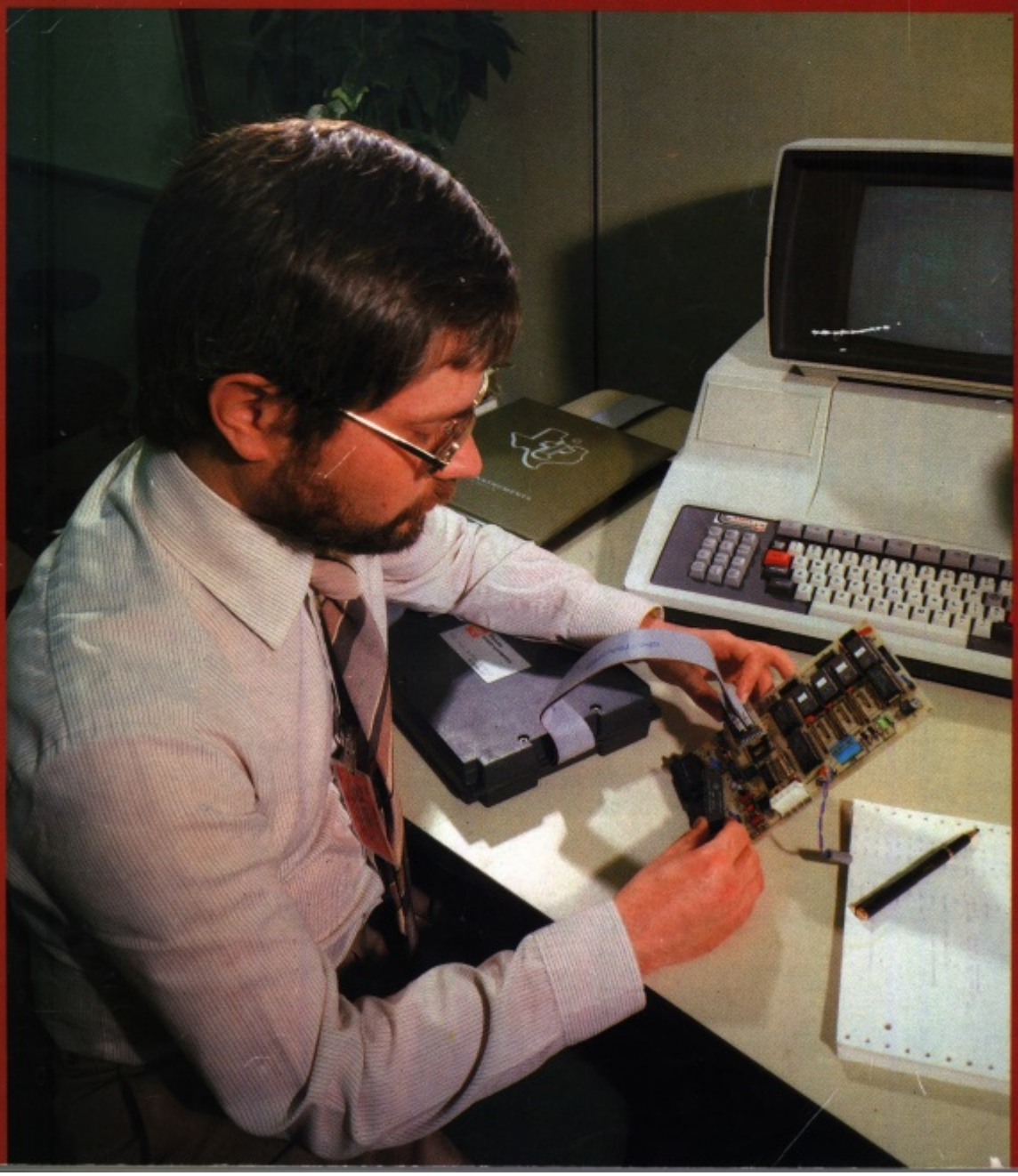
TEXAS INSTRUMENTS 8-BIT MICROCOMPUTERS

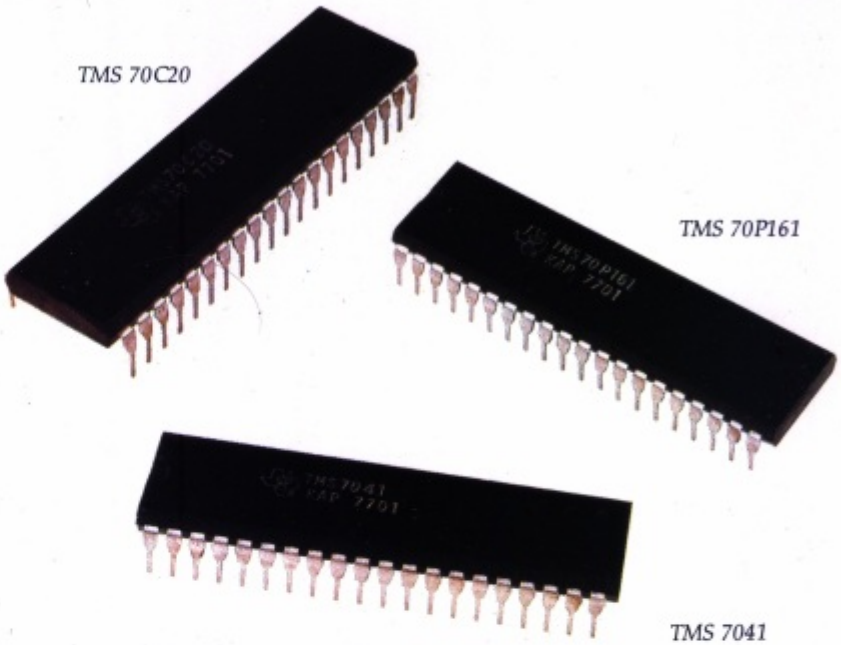
TMS 7000: The cost-effective high performance micro



The world's best price/ performance 8-bit microcomputer family

Texas Instruments are a major supplier of single chip microcomputers. We recently shipped our 80 millionth TMS 1000 4-bit microcomputer, the world's best selling single chip microcomputer. This level of experience gives us unrivalled understanding of the needs of the single chip microcomputer market.

The TMS 7000 family is the new, advanced range of high performance NMOS and CMOS 8-bit microcomputers from Texas Instruments. This second generation family of devices is more than just a new series of microcomputers, it is a new concept in design.



Microprogramming

Just a brief examination of the TMS 7000 shows it's potential.

It's the world's first microprogrammable microcomputer. That means the standard instruction set can be changed to suit the needs of a particular application. For example, to provide faster execution for time critical applications, to compress a long program to fit in the ROM of a single chip microcomputer, or for extra algorithm security. Texas Instruments provides all the development aids to allow a user to develop his own microcoded instruction set.

Powerful Instruction Set

The TMS 7000 architecture and standard instruction set are common to all the processors in the family. So if you need to change to a new processor during development (to provide more memory or reduce power consumption, for example) then this may be achieved with a minimum of software alterations.

The architecture has been optimised for fast real time applications and is very powerful. It offers a memory mapped register file, stack operations, 64K byte address space, direct, indexed and indirect addressing, hardware multiply and up to 4 different memory expansion modes.

Microprocessor versions of all the TMS 7000 family members are available.

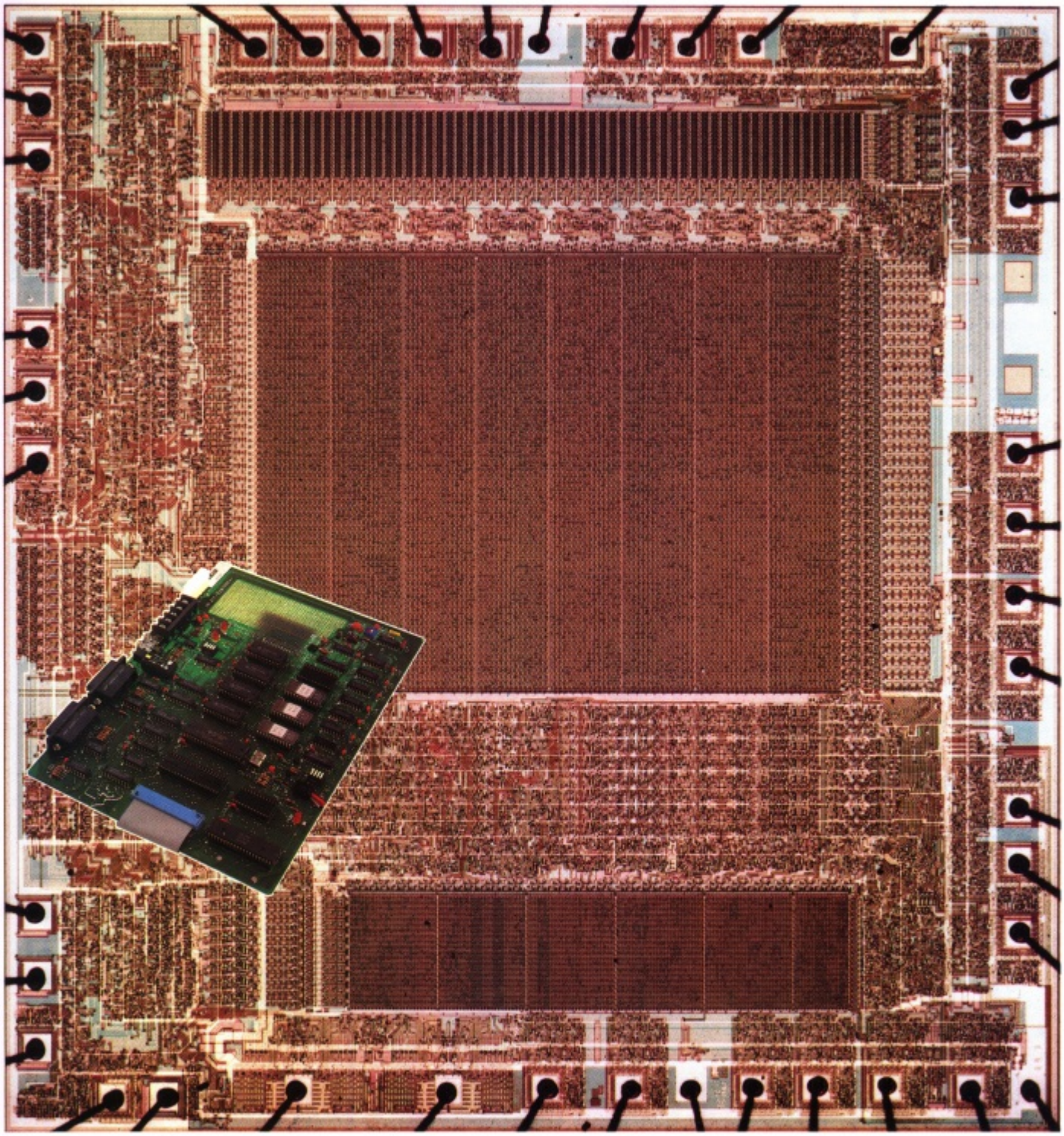
Revolutionary SCAT Layout

Tomorrow's 8-bit, high volume applications will demand more performance and more capability. The key to providing the most cost-effective solution for a range of parts is SCAT (Strip Chip Architecture Topology) VLSI layout shown here (see photo). All TMS 7000 family processors are designed with this technique, which abandons traditional random logic techniques for a completely new approach. Chip size is reduced by a factor of 25% or more over other microcomputers with similar features.

A Complete Range of Development Aids

TMS 7000 is fully supported by development aids which range from very capable low cost evaluation boards to multiuser hard disc systems. TI has technical support people to assist during all stages of development to enable you to get your product to market as fast as possible.

ON OTHER PAGES: ..... Components ..... pages 4/5: Microprogramming, Future Developments, and SCAT .... pages 10/11: Standalone



TMS 7041 Bar

Components

Choosing the Right Processor for the Application

Whenever you decide to use an 8-bit single chip microcomputer in a new design, a number of different criteria must be met. Certainly for large quantity production it is necessary to use a device which will have the required capability combined with the lowest total system cost, yet will not have excessive or wasteful capabilities which are not needed. This normally means finding the right combination of speed, memory size (ROM & RAM), I/O, power consumption and sometimes even physical size.

Texas Instruments designed the TMS 7000 family as a second generation 8-bit microcomputer to meet the demanding needs of the 1980's.

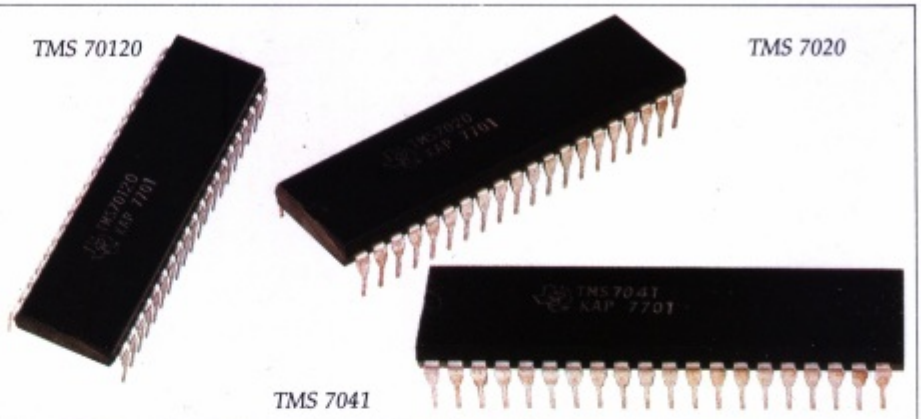
So far over 10 different variants of the basic architecture are available or nearing completion. We focus here on four different TMS 7000 family members, each of which is intended for use in a particular application area.

TMS 7020/7040

Features:

- 8-BIT CPU
- 2/4K BYTE ROM
- 128 BYTES RAM
- MICROPROGRAMMABLE
- 64K BYTE ADDRESS RANGE
- 32 I/O LINES
- 4 MEMORY EXPANSION MODES
- 8-BIT TIMER/EVENT COUNTER WITH 5-BIT PRESCALER
- 5 VOLT OPERATION
- 2 EXTERNAL INTERRUPTS
- 400mW TYPICAL POWER DISSIPATION
- 40 OR 28 PIN PACKAGE

The TMS 7020 and the TMS 7040 are the basic NMOS single chip microcomputers in the TMS 7000 range. They feature the very flexible second generation architecture of the TMS 7000 family, and have exceptional price performance. The 10MHz NMOS parts are available in a choice of 40 pin package, or 28 pin package for extra cost saving.



TMS 7041

Features:

- 8-BIT CPU
- 4K BYTE ROM
- 128 BYTES RAM
- MICROPROGRAMMABLE
- 64K BYTE ADDRESS RANGE
- 32 I/O LINES (29 IF UART IS IN USE)
- 2 8-BIT TIMERS WITH 5-BIT PRESCALERS
- 2 EXTERNAL INTERRUPTS
- MULTI-MODE OPERATION UART
  - — Asynchronous, Isosynchronous, Multiprocessor and Serial I/O expansion
  - — Dedicated baud rate timer
- 5 VOLT OPERATION
- 600mW TYPICAL POWER DISSIPATION
- 40 PIN PACKAGE

The TMS 7041 is currently the highest performance processor in the TMS 7000 range. The on-chip UART offers programmable 5-8 data bits, 1-2 stop bits, even or odd parity and baud rate. The multiprocessor mode of operation (in both asynchronous and isosynchronous modes) makes the TMS 7041 well suited to meet the increasing trend in applications towards distributed processing. The Master/Slave protocol is partly implemented in hardware minimising the software to be written by the user, and allowing efficient programming. When the UART is not in use, its 8-bit timer is available for general use. All the three on-chip timers have their own dedicated interrupts.

Typical Applications

Remote terminals, Printers and Peripherals, Multiprocessor applications, Intelligent sensors.

TMS 70C20/TMS70C40

Features:

- 8-BIT CPU
- 2/4K BYTE ROM
- 128 BYTES RAM
- MICROPROGRAMMABLE
- 64K BYTE ADDRESS RANGE
- 32 I/O LINES
- 4 MEMORY EXPANSION MODES
- 8-BIT TIMER/EVENT COUNTER WITH 5-BIT PRESCALER
- 3 TO 6 VOLT OPERATING VOLTAGE
- 2 POWER DOWN MODES
  - — WAKEUP
  - — HALT

  (both activated in software)
- 50mW TYPICAL POWER
  4mW WAKEUP MODE
  25μW HALT MODE

These silicon-gate CMOS microcomputers combine very low power consumption with the high performance of the advanced TMS 7000 architecture. All the features of the NMOS devices are retained; in

TMS 7000 Range

fact CMOS TMS 70C20/70C40 are software and pin-for-pin compatible with their NMOS counterparts. In addition they provide 2 power saving modes the WAKEUP & the HALT mode. In WAKEUP mode, both the on-board RAM and the timer are powered up; in HALT mode, only the RAM memory is powered up. The power down modes are entered through software and released by interrupts.

Typical Applications

Portable Instruments, Pocket Computers, Remote sensors, Domestic Appliances.

TMS 70120

Features:

- 8-BIT CPU
- 12K BYTE ROM
- 128 BYTES RAM
- MICROPROGRAMMABLE
- 64K BYTE ADDRESS RANGE
- 32 I/O LINES
- 4 MEMORY EXPANSION MODES
- 8-BIT TIMER/EVENT COUNTER WITH 5-BIT PRESCALER
- 2 EXTERNAL INTERRUPTS
- 500mW TYPICAL POWER DISSIPATION
- 5 VOLT OPERATION
- 40 PIN PACKAGE

The very large ROM capacity of this device (12K bytes) is suitable in applications which would normally require external memory expansion; for example complex applications requiring high level languages or extensive data tables. Despite its large memory size the TMS 70120 is very cost-effective because of the bar-saving SCAT design techniques which minimise the extra silicon bar space required. ●

Typical Applications

Video system controllers (pre-programmed display pages), Non-linear systems (look-up tables), Data storage, High level languages.

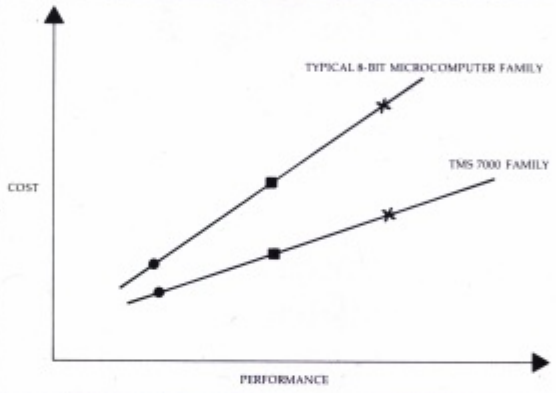


Figure 1
The Cost v Performance Curve. The advanced 'SCAT' layout technique allow more functionality to be put on a given area of silicon, hence improving the cost/performance ratio.

TMS7000 Family Device Summary

	7000	7001	7020	7040	70120	7041	70C00	70C20	70C40	70P161
ROM (KBytes)	0	0	2	4	12	4	0	2	4	16●
RAM (Bytes)	128	128	128	128	128	128	128	128	128	128
I/O Bits	32	32	32	32	32	32	32	32	32	32
Serial Port	NO	YES	NO	NO	NO	YES	NO	NO	NO	YES
No. of Mem Exp'n Modes	1	1	4	4	4	4	1	4	4	4
No. of Interrupts	3	5	3	3	3	5	3	3	3	5
8-Bit Timer/ Event Counter	YES	YES (2)	YES	YES	YES	YES (2)	YES	YES	YES	YES (2)
Internal Clk (MHz)	2.5	2.5	2.5	2.5	2.5	2.5	1.5	1.5	2.5	
Ext. Crystal(MHz)	10	10	10	10	10	10	3	3	3	5
Op. Voltage	5	5	5	5	5	5	3/6	3/6	3/6	5
Curr. Drain (ma at max op freq)	80	120	80	100	100	120	5	5	5	250
Pwr Dwn Curr.(μA)*	—	—	—	—	—	—	400/5	400/5	500/5	—
Technology	NMOS	NMOS	NMOS	NMOS	NMOS	NMOS	CMOS	CMOS	CMOS	NMOS
DIL Pkg	40	40	28/ 40+	28/ 40+	40	40	40	28/ 40+	28/ 40+	40

\+ — 28 pin package offers reduced input/output
● — EPROM "piggy-back"
* — "Wakeup Mode/Halt Mode"

Notes:

1. All devices are available for –40°C to + 85°C operating temperature range at additional cost.
2. A 2k EEPROM version of the TMS 7000 with 256 bytes static RAM will be available in 1984, equivalent to the SEEQ 72720 device.
3. For the NMOS devices a divide-by-2 option exists for the external crystal e.g. 5MHz instead of 10MHz.
4. The non-maskable reset interrupt is not included in number of interrupts line.

Architecture

Figure 2 — TMS 7000 Block Diagram

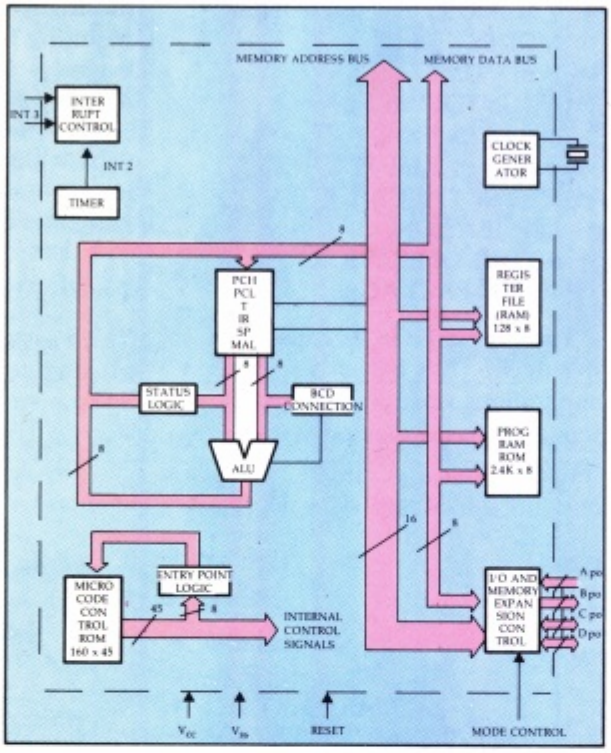
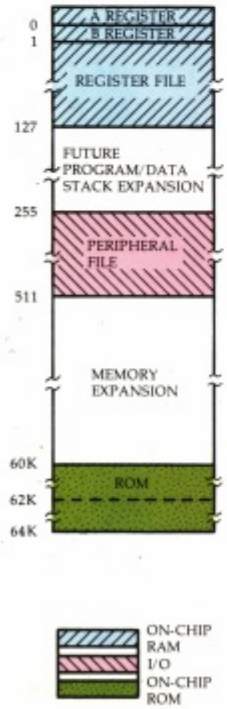


Figure 3 — Memory Map



TMS 7000 Architecture

Description

The TMS 7000 family of single chip microcomputers uses a modular architecture to simplify the development of new family members and to make the most efficient use of the available chip size. The SCAT layout and microprogrammable CPU are a fundamental part of the design (see pages 10, 11), representing an innovative solution to the on-chip interconnection problem of very complex VLSI devices. Each TMS 7000 is based around a microprogammable Central Processor Unit (CPU), which, interfaces to a combination of on-chip RAM, ROM and I/O circuitry (see block diagram). The TMS 7000 CPU implements a 64K byte logical address space and interfaces with I/O registers, timer circuit controls, and other useful on-chip functions by referencing certain addresses within the memory map.

Memory

TMS 7000 stores data and instructions in the same area of memory i.e. unified memory structure. The first 128 bytes of memory are on-chip RAM which can be used as a Register File. The first two positions in the memory-mapped array can be used as the dedicated accumulator (A), and index register or second accumulator (B). To allow development of future TMS 7000 family members with larger RAM an additional 128 bytes of memory space has been reserved.

Above this RAM area in the memory space is 256 bytes of peripheral memory which includes all the control registers for timer, interrupts, I/O ports, etc on the chip. When a memory reference is made to a port not existing on-chip (approx 240 bytes in the Peripheral File) the 7000 performs an external memory reference, permitting an 8-bit peripheral chip to respond. This may be used to handle memory-mapped I/O devices very efficiently.

The mask ROM is implemented at the high end of memory. The rest of the 64K user memory area is accessible externally to the TMS 7000 in full expansion or microprocessor mode. A trap vector table is implemented at the highest addresses in memory to provide software interrupts using the TRAP instruction. (See Instruction set summary.)

I/O Flexibility

The TMS 7000 Series provides 32 I/O pins configured as four 8-bit input/output ports. They can be configured through the use of four expansion modes. These modes give the TMS 7000 Series the flexibility to trade-off pins of dedicated I/O for off-chip peripheral and memory expansion.

Access to the I/O pins is gained by reading or writing to certain 8-bit "ports" in the Peripheral File. For example, the "A" port is implemented as Peripheral File register four (or "P4").

Six instructions are dedicated to I/O port data manipulation, providing the bit and byte I/O

Architecture

manipulation required for control applications. Additionally, the I/O ports can be accessed with general extended memory addressing instructions.

Interrupts

Four prioritised interrupts are provided (6 on the TMS 7001/TMS 7041/SE 70P161).The system reset interrupt is nonmaskable (and has top priority), but each of the other three hardware interrupts is enabled separately by bits in the I/O control register (in the Peripheral File) and together by a bit in the status register. Two of these interrupts are externally triggered by either a pulse or level at the appropriate interrupt request pin. The remaining interrupt is generated internally.

Timer/Event Counter

The on-chip 8-bit timer with the 5-bit prescaler can be driven by either the internal clock or by an external source (via one of A port inputs) for event counting. The 5-bit programmable prescaler allows a pre-divide of one to thirty-two to be selected for optimum resolution in specific applications. When the 8-bit timer itself decrements through zero an interrupt request is issued.

The capture latch is another attractive feature of the on-chip timer. The occurrence of an external level 3 interrupt loads the capture latch to record the contents of the timer. Thus, a precise measurement of the time the interrupt occurred is available. This capability is especially valuable when the external event occurs while the processor is servicing a higher-priority interrupt. Tasks such as pulse-width measurements may be carried out with a minimum of external circuitry by use of this capture latch.

Expansion Modes

The four memory expansion modes give the TMS 7000 Series outstanding flexibility for handling a wide range of different applications.

The TMS 7020, TMS 7040, and TMS 7041 can operate as stand-alone microcomputers when in the Single-Chip Mode. The user has the option of selecting either external peripheral or external memory expansion for more complex applications by placing the TMS 7020, TMS 7040 or TMS 7041 in the Peripheral Expansion Mode or Memory Expansion Mode respectively. The TMS 7020, TMS 7040 or TMS 7041 can be configured to operate as a ROM-less microcomputer when placed in the Microprocessor mode.

Figure 4 — Timer

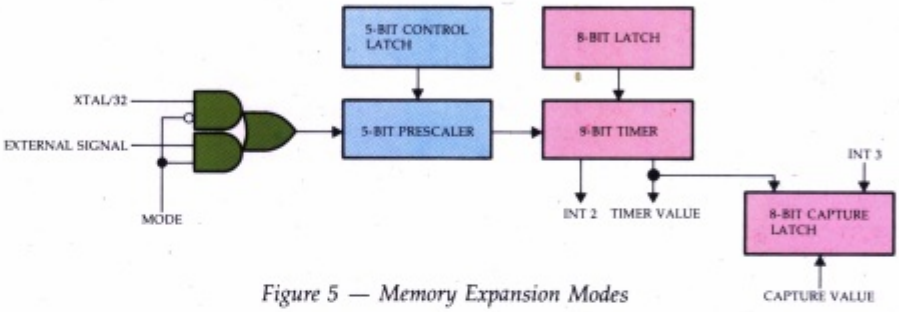
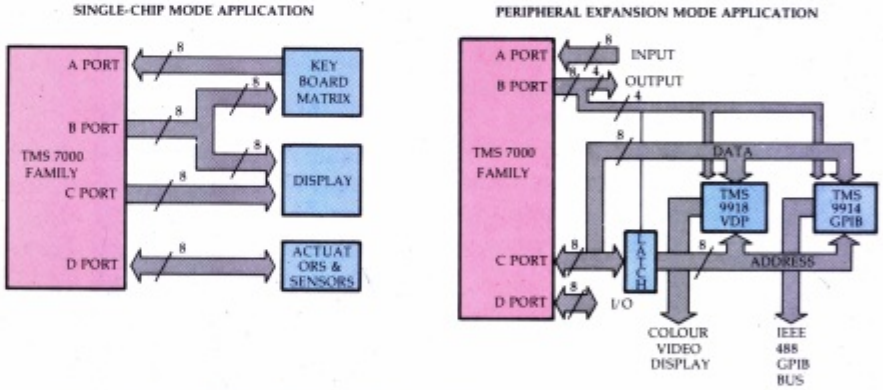
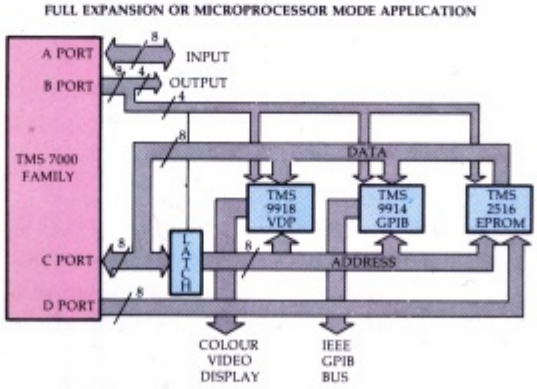


Figure 5 — Memory Expansion Modes





EXPANSION MODES SUMMARY
(Table 2)

EXPANSION MODE	ON-CHIP RAM BYTES	ON-CHIP ROM BYTES	ON-CHIP I/O LINES	OFF-CHIP MEMORY BYTES
MICROCOMPUTER	128	2048/4096	32	0
PERIPH EXP'N	128	2048/4096	20	246
FULL EXPANSION	128	2048/4096	12	63224/61176
MICROPROCESSOR	128	0	12	65272

Instruction set

TMS 7000 Instruction Set

The TMS 7000 instruction set is unique amongst 8-bit single-chip microcomputers available today and it is well worth spending some time assessing the advantages this offers the application. The set provides a powerful combination of instruction opcodes and addressing modes which at the same time are easy to learn and apply.

A key feature of the TMS 7000 architecture is the ability for the programmer to regard the on-chip RAM memory as a 128 GENERAL PURPOSE REGISTER FILE (R0-R127). This can be seen in the instruction set where the majority of operations possible are contained within the RAM area. This concept will be expanded to 256 bytes of on-chip RAM in future 7000 series microcomputers.

This memory resident arrangement of registers means dual operand instructions can operate on any RAM location for the source and any RAM location for the destination avoiding the data bottleneck found on many traditional accumulator-based microcomputers.

However, the fastest execution speeds and minimum memory requirements are achieved if RO (also referred to as the A-register) and R1 (B-register) are specified giving the usual advantages of hardware accumulators. The use of A and B registers are implied as the operands in all single byte instructions e.g. CLR A, ADD B,A. Addition of another byte means any one of 128 RAM locations can be accessed e.g. CLR R32, ADD R32,A.

Data table organisation, arithmetic operations and minimal imposed stacking discipline in responding to interrupts are all made easier by the flexible 128 byte Register File at the heart of the 7000.

As well as the more common opcodes found in the instruction set there are several worth highlighting here:

- **Decimal Arithmetic**
  - — performed on two packed BCD bytes using DAC (Decimal Add with Carry) and DSB (Decimal Subtract with Borrow). These are very useful for point of sale, financial, scientific or "real world counting" applications.
- **Multiply**
  - — 8 x 8 unsigned multiply which is 17.2 μs for 10MHz version. Very few single chip 8-bit microcomputers make available a hardware multiply.
- **Combination Test**
  - — where one instruction incorporates both the testing of a register and a conditional jump operation. See examples DJNZ and BTJO/BTJZ in the table opposite.
- **Software Interrupts (or Traps)**
  - — up to 20 Traps are available for the user to specify. These one-byte subroutine calls use the 16-bit address previously stored in the appropriate 2-byte vector location at the top of memory. In this way the practice of modular programming and memory code efficiency are easily obtained.

In order to support the capability of the TMS 7000 series microcomputers to address 64K bytes of memory the following are provided:

1. Instructions such as MOVD (Move Double) and DECD (Decrement Double) to allow manipulation of 16-bit values within the Register File.
2. Extended addressing modes such as:

   Register Indirect — address of operand contained in two contigious registers

   Direct — 16 bit address is made up from the 2 bytes following the opcode

   Indexed — where the address of the operand is derived from the sum of the direct address and the 8-bit offset contained in the B register (facilities searching of 256 byte blocks)

The on-chip RAM lies in the unified memory map and can therefore be accessed using normal 16-bit addressing. This allows the RAM to be partitioned to perform not only as a Register File as described previously, but as a scratchpad data area and as programme memory. Applications where there are time critical paths or routines that need to be dynamically altered will find this flexibility very useful.

There are six dedicated PERIPHERAL FILE instructions to manipulate on-chip control registers or input/output ports that fall in the 256 byte address range >0100 to >01FF. These allow the programmer to set (ORP), clear (ANDP), complement (XORP) and test (BTJOP/BTJZP) one or more bits in addition to reading and writing (MOVP) a byte.

With the added, and very unique, dimension to the instruction set of MICROCODE PROGRAMMABILITY AT USER LEVEL (ie. the AMPL emulator allows the user to create his own instructions), the 7000 makes an extremely comforting choice in tackling a difficult application, and achieving a single chip microcomputer solution.

It has only been possible to give a brief appreciation of the 7000 instruction set. For further reading the 7000 Data Manual and the 7000 Assembly Language Programmer's Guide are recommended while practical evaluation can be carried out with the TMAM 6100A Standalone Development Board.

Instruction set

7000 Instruction Examples

NOTE:
Brackets represent "byte count/system clock cycles"

DATA MOVEMENT

— MOV R8, R32 (3/10)
Move contents of register 8 to register 32
— MOV B, R58 (2/7)
Move contents of B register to register 58
— MOV B, A (1/6)
Move contents of B register to A register

COMBINATIONAL TEST

— DJNZ R30, LOOP (3/9)
Decrement contents of register 30 and if not equal to zero jump (relative) to LOOP
— BTJO >11, R12, TEST (4/11)
Test bits 0 & 4 in register 12 and if either is set to one jump (relative) to test

DECIMAL (BCD)

— If R15 = >15, B = >36 and Carry Bit = 0 the instruction will perform an addition resulting in >51 being stored in B

MULTIPLY

— MPY R5, R87 (3/48)
Multiply register 5 by register 87 and store 16-bit result in A and B registers with the most significant byte in A register

HANDLING 16-BIT VALUES

— MOVD % >FO48, R52 (3/10)
Load the immediate value >FO48 into register 52 and 51
— DECD R108 (2/11)
Decrement register 108 and 107 as a 16-bit number

PERIPHERAL FILE

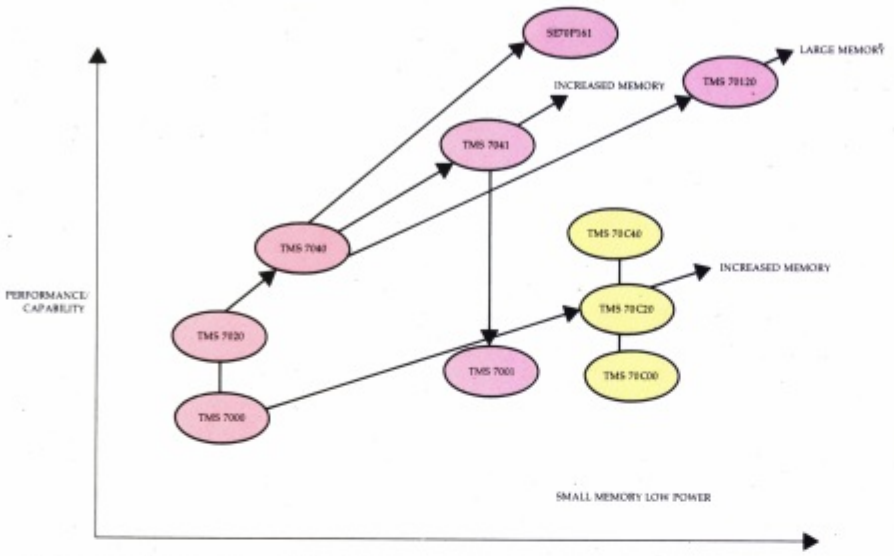
— ORP B, P10 (2/9)
If B contains >03 then the bits 0 and 1 of port 10 will be set

EXTENDED ADDRESSING

— CMPA *R78 (2/11)
Assuming R78 contains >E2 and R77 contains >FO this instruction will compare the contents of address >FOE2 with the A-register and set the appropriate bits in the status register.

Microcoding — Future products

Figure 6 — Development of the TMS 7000 Range



Microcoding, SCAT, Custom Devices — The Future of TMS 7000

1. A New Design Concept

The recently introduced TMS 7000 is much more advanced than many earlier 8-bit microcomputers. Texas Instruments believes that there will be a growing requirement for more powerful 8-bit microcomputers in the next few years. In order to meet this demand, a flexible architecture and chip layout has been developed which will allow new devices to be added to the family quickly and simply. Examples of future possible devices are large ROMS (up to 16K bytes), larger RAM (up to 256 bytes), additional on-chip I/O, like A/D converters, LCD drive etc.

With the TMS 7000 TI has taken a new look at the traditional implementation of microcomputer design. Two significant innovations, SCAT and MICROPROGRAMMING, allows TMS 7000 to provide a powerful instruction set and still maintain an extremely small bar size.

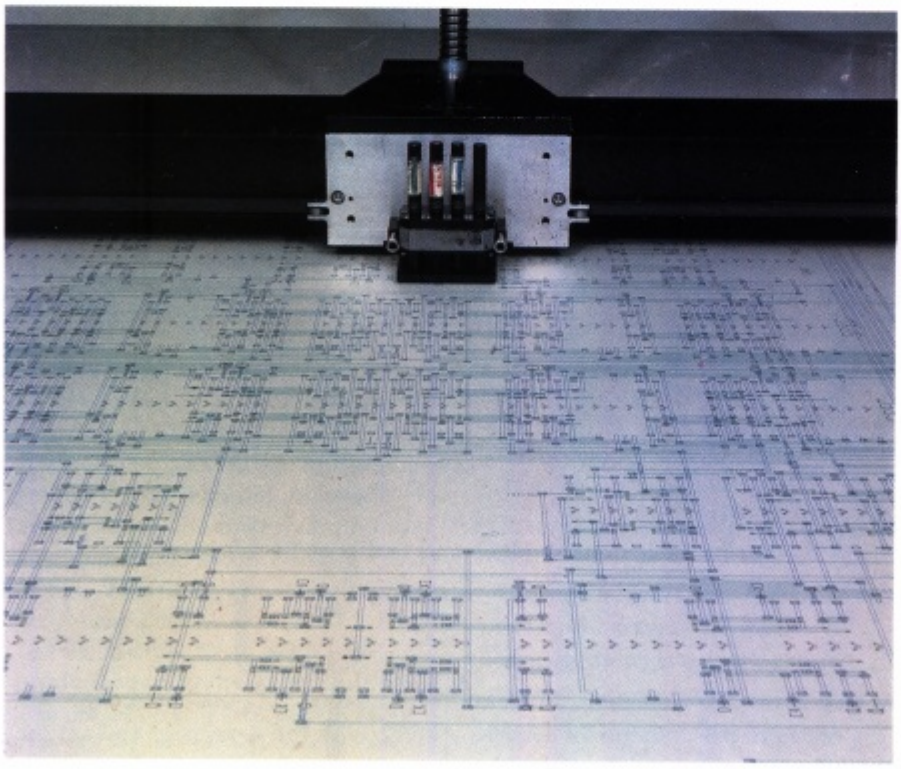
2. Microprogramming

The TMS 7000 family is the first fully microprogrammable 8-bit microcomputer range in the world.

A control ROM replaces random logic for defining the instruction execution sequence. This has two main advantages over normal methods.

Firstly it reduces bar area, thereby reducing cost. Secondly it gives a potential user the ability to define his own instruction set. This may be used to provide increased speed by reducing the number of instructions in a time critical routine, to make more efficient use of a limited amount of program memory or to provide increased security of software — in effect producing your own microcomputer. This would reduce the possibility of duplication by a competitor. Up to 25% of the standard instruction set may be modified.

Microcoding will normally only be cost effective for applications using 50,000 or more units per year, since most applications will find the standard instructions adequate. But there will be some applications where microcoding will provide a unique advantage. Full support is available on TI's AMPL systems for developing microcode, including microcode assemblers and a hardware emulator, together with all the necessary documentation. Training courses (3 days) are also available. Alternatively it may be possible for TI to develop new instructions if requested by the user.



Layout Plotter

3. SCAT — The Advantages

The Strip Chip Architecture Topology is TI's term for the design philosophy which incorporates the non-memory elements of a microcomputer architecture i.e. the registers, ALU + control logic in a strip of vertical bricks in the logic design. The diagram shows the layout of the TMS 7020, the 2K ROM version of the TMS 7000 family. Most of the interconnection between the blocks (in the form of data and address busses) is implemented on a layer of metal over the silicon. As a result, valuable (and expensive) bar area is not wasted in interconnecting the logic elements as in a traditional random logic design. The result is a high performance chip, with a significantly lower cost than its competitors.

An example of the strip chip architectural flexibility — TI created the TMS 7040 4K ROM version from the TMS 7020 2K ROM version without redesigning the chip. The bar design was separated at the memory border and the additional 2K of memory simply inserted alongside the original 2K of memory by the design computer. Likewise, additional features such as more ROM, RAM, or different I/O structures can be added with a minimum of design, resources and time. (see photo) TI plans to take advantage of the flexibility of the strip architecture by adding many new devices to the TMS 7000 Series in the future to offer a broad spectrum of TMS 7000 microcomputer devices to meet a wide range of different user requirements.

4. Special Customisations

For high volume users of the TMS 7000, that is, those intending to use more than 100,000 units/annum, there is one more option available. That is, to specify the design of a 'semi-custom' TMS 7000. This means defining a unique TMS 7000 family member for either a particular application or range of applications. This may be done in conjunction with TI. Because of the unique SCAT layout of the TMS 7000, such new devices may be very quickly implemented, perhaps in a matter of months if the additions are simple. It could be a matter of adding more memory — or less if cost is important — extra serial I/O, high current outputs, etc, and of course where high volume production is concerned the savings produced by such a custom solution can be very significant.

It is beyond the scope of this brochure to discuss this possibility in detail, so if you are interested, please contact Texas Instruments directly.

Figure 7 — 'SCAT' Design Layout

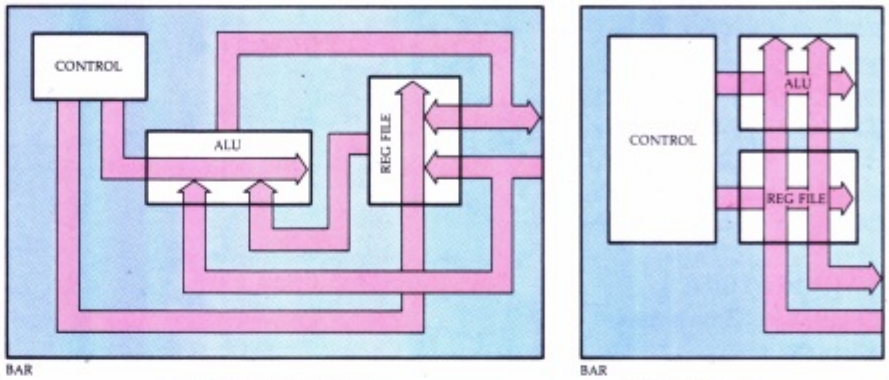
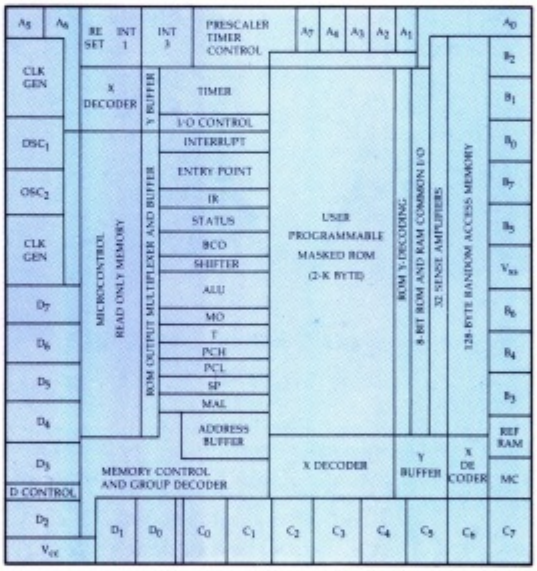
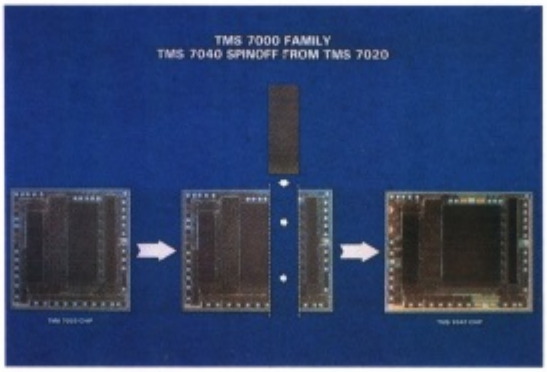


Figure 8 — 'SCAT' Bar Layout



$A_0 - A_7$ = A PORTS
ALU = ARITHMETIC AND LOGIC UNIT
$B_0 - B_7$ = B PORTS
BCD = BINARY-CODED DECIMAL CHECKER
$C_0 - C_7$ = C PORTS
CLK GEN = CLOCK GENERATORS
$D_0 - D_7$ = D PORTS
I/O = INPUT-OUTPUT
INT = INTERRUPT INPUT
IR = INSTRUCTION REGISTER
MAL = MEMORY ADDRESS LOW BYTE
MC = MEMORY CONTROL
MD = MEMORY DATA GATES
OSC_1-OSC_2 = OSCILLATOR CRYSTAL INPUTS
PCH = PROGRAM COUNTER HIGH BYTE
PCL = PROGRAM COUNTER LOW BYTE
REF = REFERENCE
SP = STACK POINTER
T = TEMPORARY REGISTER



TMS 7040 Spinoff from TMS 7020

Development systems

Development Support for the TMS 7000

TEXAS INSTRUMENTS DEVELOPMENT SYSTEM APPROACH — TI offers a whole range of development aids from single board systems, to fully packaged multiuser systems.

TMAM 6100A

Standalone Development Board

Features:

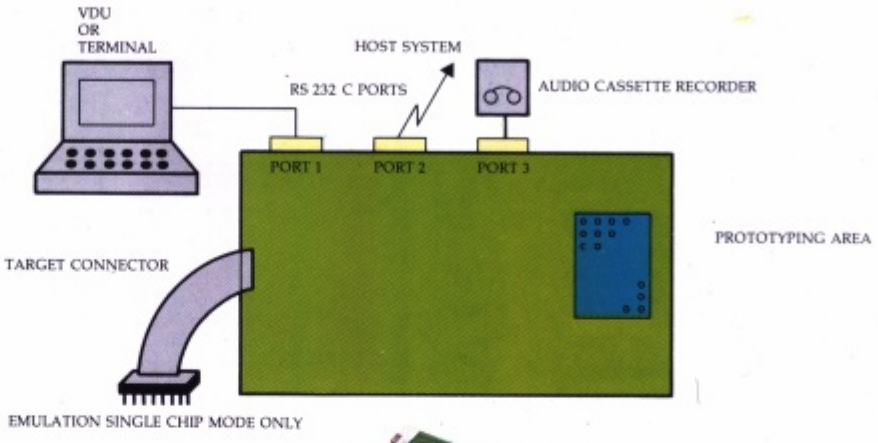
- Firmware utilities include text editor, full feature assembler and debug monitor.
- Low cost audio cassette storage (filename and file search supported).
- On board EPROM programmer for TMS 2532.
- Supports link to host system for source and object (TMS 7000 or Tektronix format) files.
- In-circuit emulation for TMS 7020, TMS 7040 and TMS 7041.
- Supplied with comprehensive USER'S GUIDE.
- Prototyping area served by address, data and control lines for custom application circuits.
- Execute target code in RAM or in EPROM.
- User accessible utility calls to on-board firmware.

The TMS 7000 Standalone Development Board enables a user to evaluate the capability of the TMS 7000, or to develop software for a TMS 7000 application from conception right through to its final implementation in EPROM (TMS 2532). This final ROM code is then supplied to Texas Instruments for production of masked devices. All this very low cost board requires to complete a capable development system is an EIA RS 232C terminal, power supply and audio cassette recorder.

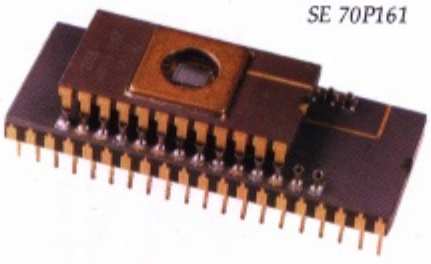
Alternatively the TMAM 6100A may be used with a host computer running TMS 7000 cross support software. In this case editing and assembly of 7000 programs is done on the host which then, downloads the target object code to the TMAM 6100A board via its second RS 232C port. Control then switches over to the board for real-time emulation. The host may be a TI computer, or a non-TI host. A number of third party software packages for the TMS 7000 are beginning to appear, such as CP/M*, and TI has cross-support for IBM and DEC computers.

For more information on the TMAM 6100A, a separate product brief is available.

Figure 9 — TMAM 6100A System Configuration



TMAM 6100A



SE 70P161

* CP/M is a trademark of Digital Research Incorporated

SE 70P161

Prototyping Chip

Features:

- 40 pin ceramic DIL package with 28 pin DIL 'PIGGYBACK' socket (for TMS 2764 or TMS 27128 EPROM).
- 8 bit CPU.
- Expandable to 16K bytes EPROM
- 128 bytes RAM.
- 32 I/O lines.
- 2 8-bit timers with 5-bit prescalers.
- On-board UART.
- NMOS technology.
- 5 volt operating voltage.
- 0—50° C operating temperature range.

Description

This device provides in-circuit emulation for the whole range of TMS 7000 single chip micro-computers, with the exception of the power down modes of the 70C00 series. EPROMS may be programmed

Development systems

using any standard EPROM PROGRAMMER. The SE 70P161 is available in small development quantities only.

AMPL* — Advanced Microprocessor Prototyping Laboratory

The most powerful development system for TMS 7000 is AMPL (Advanced Microprocessor Prototyping Laboratory). Either single user floppy disc systems, or multiuser hard disc systems are available. The system shown here is the TMAM 9001 single user system, together with the TMAM 6059 AMPL station and TMS 7000 in-circuit emulator buffer module.

This system provides full real-time in-circuit emulation and has a set of progamme development utilities, editor, and cross assembler to assemble the standard TMS 7000 code, link editor, and utilities to control the in-circuit emulator. AMPL includes a video terminal with an easy-to-use screen based editor, and twin double-sided double-density 8" floppy disc drives. Additional equipment such as printers, EPROM programmer and additional buffer module may be added. The TMAM 9001 system supports all of TI's microcomputer and microprocessor families; TMS 1000, 9900, and TMS 7000/9995/99000/320, with the addition of the appropriate XDS system.

AMPL with buffer module

AMPL Systems

DESCRIPTION	TMAM 9001	TMAM 9021	TMAM 9041
Main Memory Bytes	64K	256K	320K
Mass Storage	DSDD Floppy	Hard Disc	Hard Disc
Total Disc Storage (formatted bytes)	2.2M	32M	96M
No. of Disc Drives	1 Dual	1	
Fixed Storage	None	1 × 16M	1 × 80M
Removable Storage	2 × 1.1M	1 × 16M	1 × 16M
No. of Terminals Inc.	1	2	2
No. of Users with Extra Terminals	—	4	8+

TMS 7000 AMPL Station Packages and Software Utilities

PART NO.	DESCRIPTION
TMAM 4016-21	Assembler, linker and PROM format conversion s/w
TMAM 4017-21	AMPL Emulator control utilities
TMAM6059	TMS 7000 AMPL station. Includes TMAM 6099, TMAM 6011, TMAM 6012
TMAM 6099	TMS 7000 Emulator, Buffer Module, Target Connector
TMAM 6011	AMPL Station 6-slot chassis, Host data link, Power Supply, Enclosure
TMAM 6012	Trace Module, Data Probe and Accessory Kit

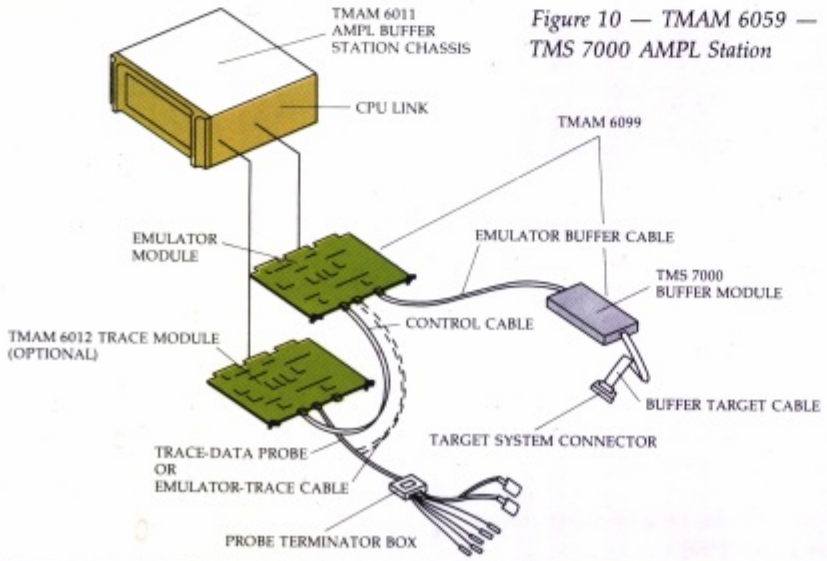


Figure 10 — TMAM 6059 — TMS 7000 AMPL Station

TI also has multi-user hard disc AMPL development systems which can support from 2 to 12 users if required and these will also support TMS 7000 program development.

(Full support is also provided for owners of existing FS 990/4 development systems.)

For more information on TI's AMPL development system series please consult the TI Microsystems Designers Handbook, available from your local TI Distributor.

** AMPL is a trademark of Texas Instruments*

Development systems

The TM990 Amplus Software Development System

Texas Instruments has produced a very low cost development system from standard microcomputer boards. The capabilities of this development system may be extended by adding more boards from the TM 990 range (see TI's Microsystems Designers Handbook for more details). A single diskette, TMAM 4011-21, the AMPLUS Software Development Diskette (SDD) provides a complete software development environment.

In addition to the diskette and boards, a floppy disc drive (8") and an RS 232C compatible terminal are required. We call this a "consumable" development system, since the boards may be used in a final application.

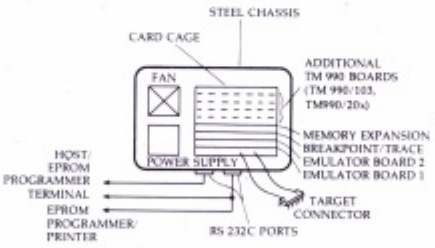
TM 990/601
System Hardware Kit
Features:

- User configurable consumable development system
- Runs SDD development system software
- Pre-configured and tested for operation with
  - SA 800/801, CDC 9404B and Qume DT/8 drives
  - EIA terminal: ADM-3 or equiv.
- Includes the following:
  - TM 990/101MA CPU module with 2 asynchronous ports
  - TM 990/203-23 64K DRAM
  - TM 990/303A Floppy Disc Drive Controller
  - TM 990/510 — 4 slot card case
  - TM 990/527 — Cable for connecting two standard disc drives to controller.

TMAM 4011-21
Software
Development Diskette
Features:

- Full file management capability (directory and files)
- Screen based text editor
- Text formatter for producing documentation
- PROM programming facility (using optional EIA-linked PROM programmer)
- 9900 Assembler and Linker as standard
- 'MENU' driven with self-prompting displays

Figure 11 — XDS-22 Exploded View



In addition to TMAM 4011-21 and TM 990/601, the TMAM 4016-21 software package with TMS 7000 assembler and linker will be required, to provide TMS 7000 program development capabilities. For in-circuit emulation with this system, the TMAM 6100A or TMS 7000 XDS system is recommended.

XDS System

12500 F per unit

The XDS Range of Emulators

LEVEL	FEATURES DESCRIPTION	PART NUMBERS NMOS	CMOS
XDS-11	Basic lowest cost system. Runs target program in real-time and gives complete control of target environment. Target debug (2 letter (XX) Primitive commands). 2 EIA RS 232C ports for user terminal, and host computer/PROM programmer. Target connector (0.5m). Assembled object can be downloaded to emulator from host computer. Power supply not included.	TMDS 7061110	TMDS 7061120
XDS-22	True fully capable emulator system. Contains all features of XDS-11 plus; Hardware breakpoint and trace boards, emulator memory expansion boards, triple RS 232C port to allow connection of printer. Self contained housing includes fan and power supply. The system is directly upwards expandable, with space available for additional boards.	TMDS 7062210	TMDS 7062220
XDS-33	All features of XDS-22 plus high level debus language to allow programmed debugging of the target system. Includes CPU board and memory board in addition to XDS-22 (to be announced).	—	—
XDS-44	Standalone emulator. All features of XDS-33 plus bulk memory storage capability with additional board (to be announced).	—	—

Development systems

XDS* — Extended Development Support

Texas Instruments has introduced (2H83) a new range of development systems — the XDS series — for its microprocessor families.

This is a new concept in development support from Texas Instruments. The XDS systems separate the program development functions of a development system from the in-circuit emulation and debug facilities. Program development is handled by a host computer (which can be a non-TI host), and all emulator and debug facilities are provided by XDS. The host communicates with XDS via an RS 232C link.

A range of XDS systems are available. At the low end of the range the host communicates with XDS using simple 'primitive' commands. At the top end of the range a set of sophisticated high level language commands and procedures are provided.

To support program development on non-TI computers a range of cross-support software packages is also being introduced featuring relocatable assemblers and linkers.

Cross Support Software

PART NO.	DESCRIPTION
TMDS 7040210*	VAX-11 Compatible Software (VMS Operating System)
TMDS 7040310*	IBM 370 Compatible Software (Series I)
TMAM 1004 & TMAM 4016-21	INTEL MDS-800 cross-support package includes plug-in board and software

*These software packages which are written in transportable Pascal include assemblers and linkers to allow TMS 7000 program development on non-TI computers.

Additionally, independent suppliers, offer support packages such as CP/M and Intel Series II MDS. Contact TI for more details.

Cross assembler TMS 7000 IBM PC.
Kost prijs 30 000 F

Masking Timescales

Software to be masked into the ROM of the TMS 7000 is supplied to TI or one of its distributors in the form of a TI system compatible diskette or an EPROM

It normally takes around 12 weeks to produce the first masked ROM samples of a TMS 7000 device. Approximately 10-25 prototype devices are supplied at this stage. Following customer approval of the prototypes production can begin.

Documentation

The following documentation is available from Texas Instruments for the TMS 7000 family and development systems.

- TMS 7000/7020/7040NL Data Manual
- TMS 70C00/70C20/70C40NL Data Manual
- TMS 7041 Data Manual
- TMS 7000 Family Assembly Language Manual
- TMAM 6100A Standalone Development Board Brief
- TMS 7000 Family Micro-architecture User's Guide
- TMS 7000 Microassembler User's Guide
- TMS 7000 Microcode Development Guide
- TMS 7000 Microprogrammer's Reference Card
- Microsystems Designer's Handbook

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