4.18.1 DMA Controller $\overline{CS}$ Signal Supply Circuit

The CS (Chip Select) signal of two DMA controllers μPD8237 (IC19J and IC21J) is supplied as shown in Fig. 4-44.

When either of these two DMA controllers is selected, the bus line must be used only by the CPU and use by the other devices is inhibited. So the $\overline{BUSAK}$ signal output from the CPU and supplied to the gate to provide the $\overline{CS}$ signal must be at high level. The address lines A7, A6 and A4 are used to supply the $\overline{CS}$ signal.

Therefore, DMA controllers are selected when A7 is 0 and A6 is 1.

Address line	A7	A6	A5	A4	A3	A2	A1	A0	I/O address
8237 (21J) $\overline{CS}$	0	1	0	0	×	×	×	×	40 ~ 4FH
8237 (19J) $\overline{CS}$	0	1	0	1	×	×	×	×	50 ~ 5FH

Table 4-18

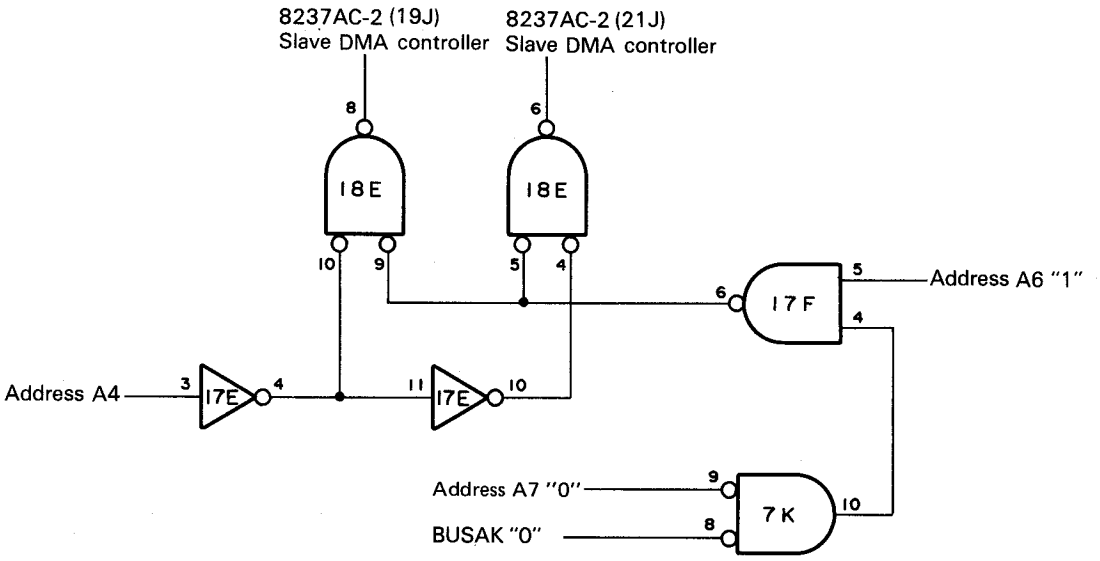


Fig. 4-44 Controller $\overline{CS}$ Signal Supply Circuit

4.18.2 Circuit to Supply DRQ Signal from CRT Drive Circuit

DMA transfer of the GDC is valid only during the CRT display period. If the DRQ is output from the Q10GMS board at the end of the display period as shown in the Fig. 4-45, the $\overline{DRQ}$ signal duration is ensured by the circuit shown in Fig. 4-46 to make DMA transfer valid until the $\overline{DACK}$ signal is output from the DMA controller μPD8237.

The timing chart is shown in Fig. 4-47.

When the high level $\overline{DRQ}$ signal from the Q10GMS board is applied to the D-type flip-flop LS74 (24M), a low level signal is generated at the $\overline{Q}$-terminal and sent to the DMA controller μPD8237 (21J). The Q-terminal is then set to high level. The signal goes through the OR gate IC20L and re-enters LS74 (24M) as its D-input.

Therefore, even if the $\overline{DRQ}$ signal is set to low level, the D-input signal is held and the $\overline{DREQ}$ signal to the μPD8237 is held at low level.

Receiving the $\overline{DRQ}$ signal, the μPD8237 transfers HRQ and HLA signals with the $\overline{DRQ}$ and then outputs the active low $\overline{DACK}$ signal. The $\overline{DACK}$ signal resets LS74 (24M), and the $\overline{DREQ}$ signal is released as a result.

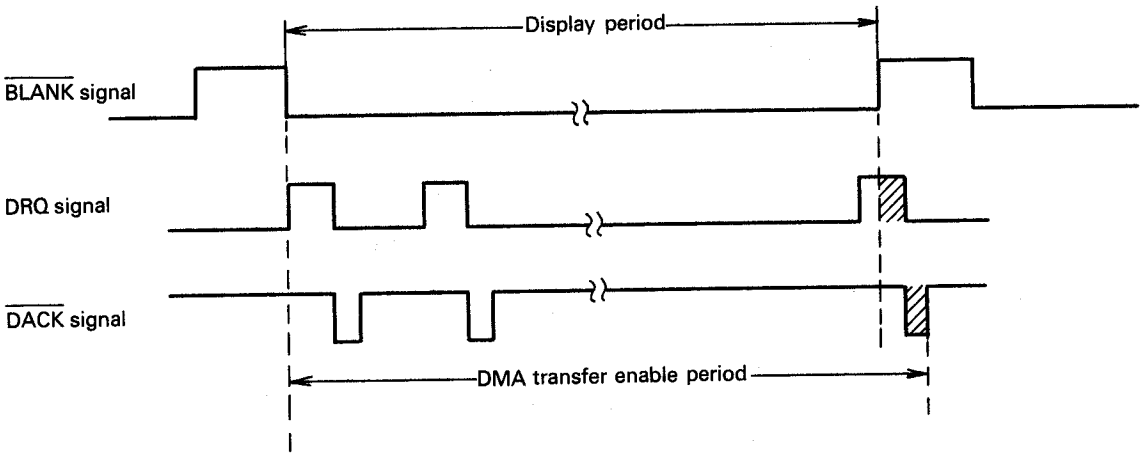


Fig. 4-45

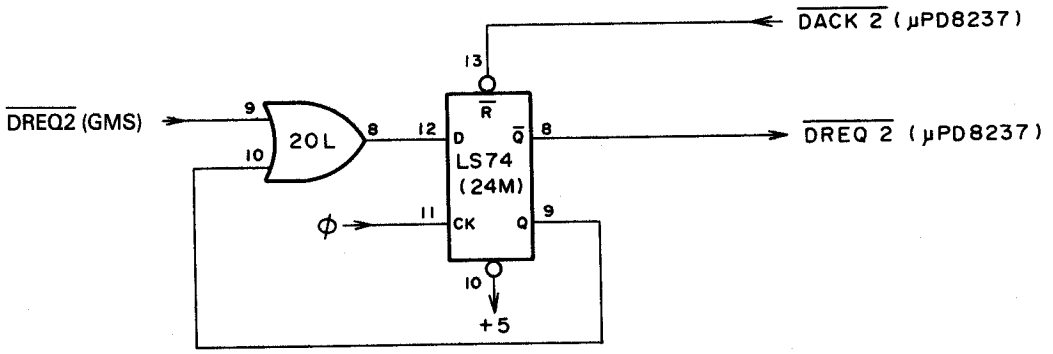


Fig. 4-46 Circuit to supply DRQ signal from CRT display circuit

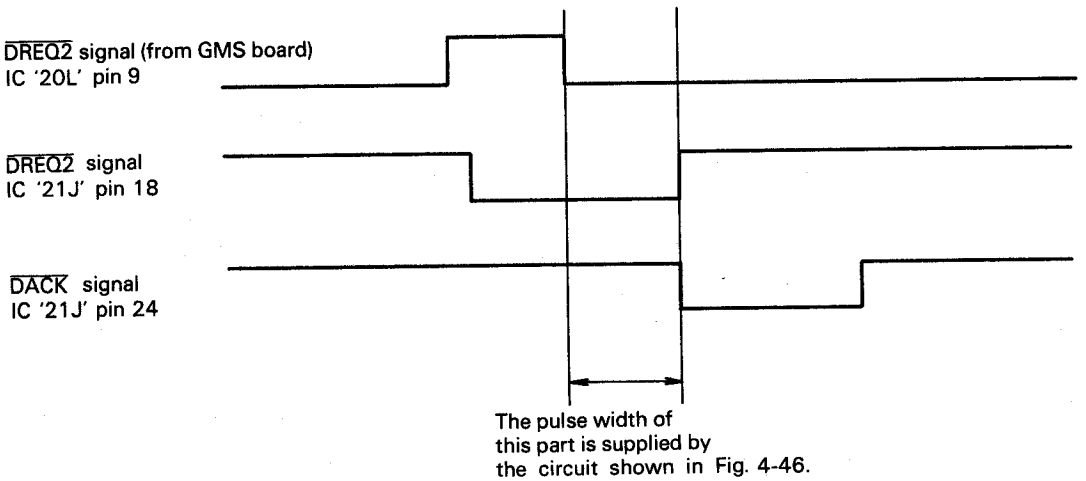


Fig. 4-47

4.18.3 DMA Transfer from Option Card

In the case of DMA transfer by connecting a low-speed memory and I/O device using an option card, the data may not be defined because the pulses of $\overline{IOW}$ and $\overline{IOR}$ signals of the μPD8237 are too short. It is necessary to wait definition of data input/output by effecting WAIT to $\overline{IOW/IOR}$ cycle by making the ready signal terminals of the μPD8237 active at $\overline{IOW/IOR}$.

The circuit shown in Fig. 4-48 is used for this purpose.

WAIT is effected by holding the $\overline{IOW/IOR}$ signal for a duration equivalent to three clocks from its active time.

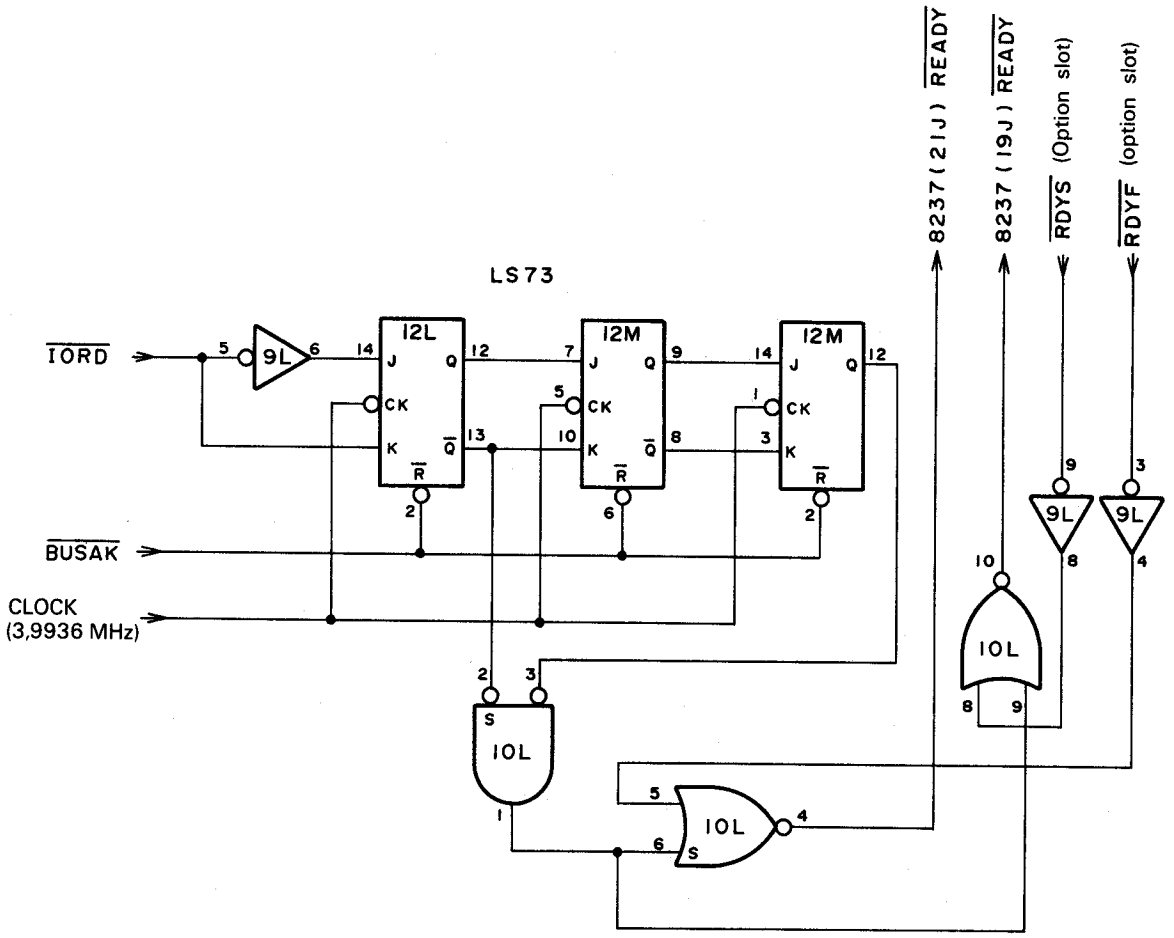


Fig. 4-48 Circuit to supply READY signal at DMA transfer from option card

4.18.4 DMA Transfer

The operation sequence of the μPD8237 for DMA transfer is described using the timing chart of Fig. 4-49.

(1) A DMA transfer request ($\overline{DREQ}$) signal from an external I/O device is applied to the μPD8237.

(2) The μPD8237 judges the priority of the $\overline{DREQ}$ signal, and supplies the active high HRQ signal to the $\overline{BUSRQ}$ signal input of the CPU through the inverter.

(3) Receiving the $\overline{BUSRQ}$ signal, the CPU sets the three-state address and data bus to the high impedance state, outputs the $\overline{BUSAK}$ signal and supplies and active high signal to the HLA signal terminal of the μPD8237 through the inverter.

(4) The μPD8237 outputs the ADEN (Address Enable) signal in order to output the memory address of the data to be sent in DMA transfer, and makes the OUTPUT CONTROL terminal of the external latch LS373 (16K) active.

(5) The μPD8237 makes the ADSTB (Address Strobe) signal and the ENABLE terminal of the external latch LS373 (16K) active, and sends the high-order eight bits of the address to be output to the data buses DB0 ~ DB7 to the system address buses A8 ~ A15.

(6) The address buses A0 ~ A7 are simultaneously output from the μPD8237 to define the address. The μPD8237 outputs the $\overline{DACK}$ signal to permit DMA transfer as an active signal to the I/O device which made the DMA transfer request.

(7) The μPD8237 outputs the $\overline{IOR}$ signal and accesses the data from the peripheral circuit, or outputs the $\overline{IOW}$ signal to load data into the peripheral circuit.

(8) DMA transfer can be terminated by the EOP (End of Process) signal.

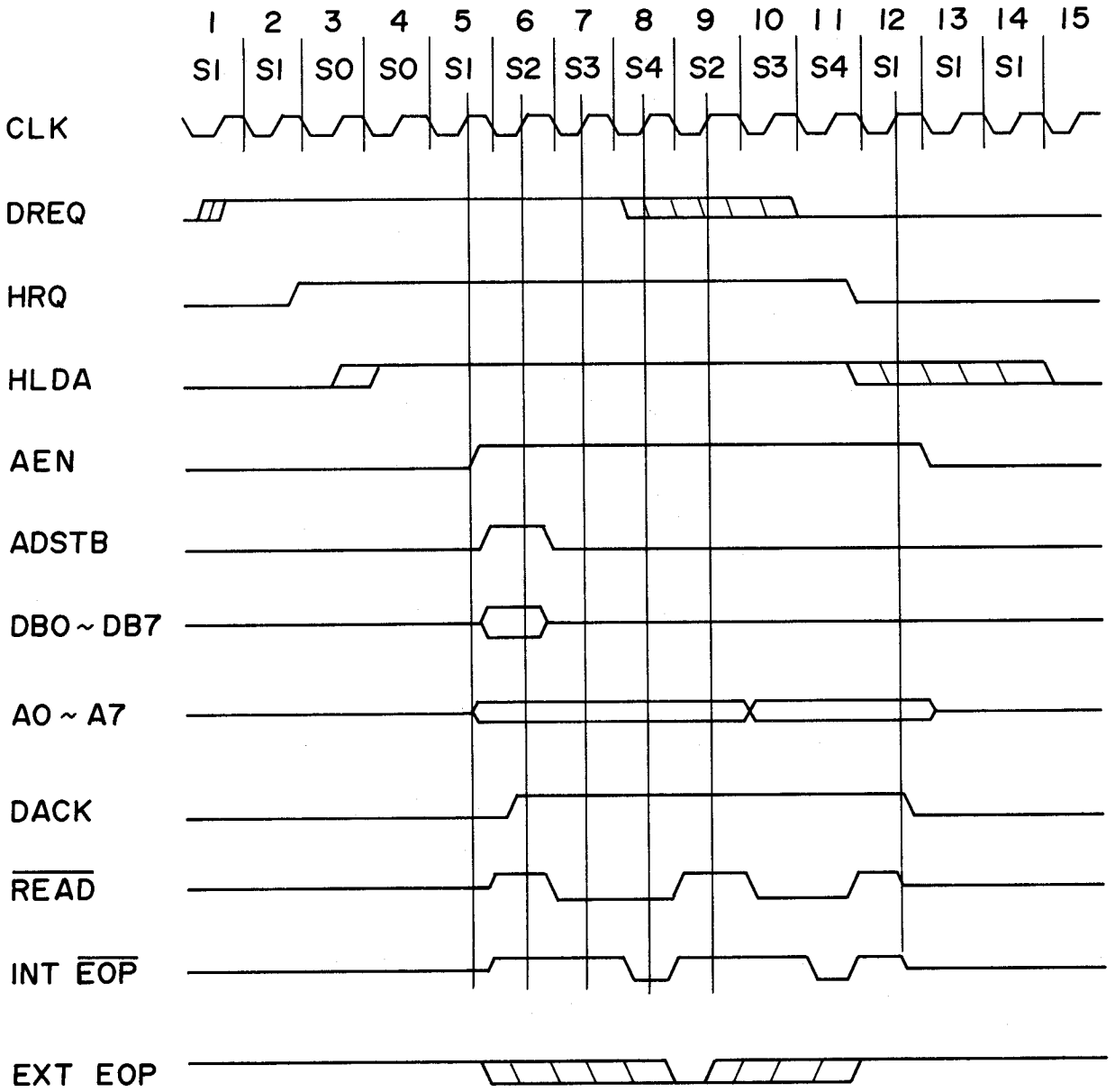


Fig. 4-49 Timing chart of DMA transfer

4.18.5 Memory-Memory Transfer

Memory-memory transfer is made as shown in the timing chart in Fig. 4-50.

(1) Output the memory address of the reading data onto the address bus. In this case, the high-order addresses A8 ~ A15 are once output onto the data buses DB0 ~ DB7 and transferred onto the address bus when the ADSTB signal is set to the high level.

(2) By making the $\overline{MEMR}$ signal active low, take out the data from the selected memory location and put it on the data bus and hold it in the temporary register provided in the μPD8237.

(3) The μPD8237 gives an address to the writing memory as in step (1).

(4) When the $\overline{MEMW}$ signal is made active low, the written data is output from the temporary register and stored in the memory.

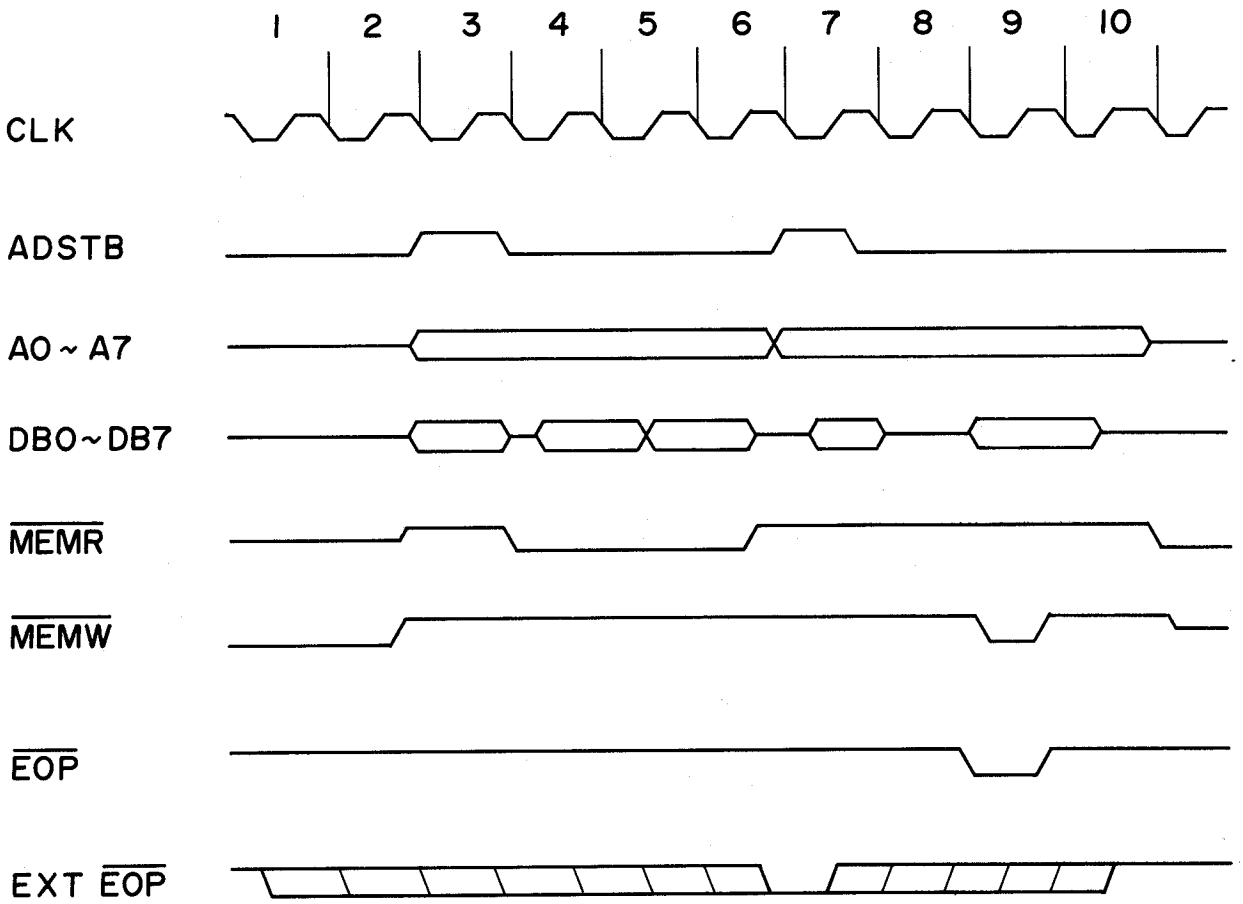


Fig. 4-50 Timing chart of memory-memory transfer

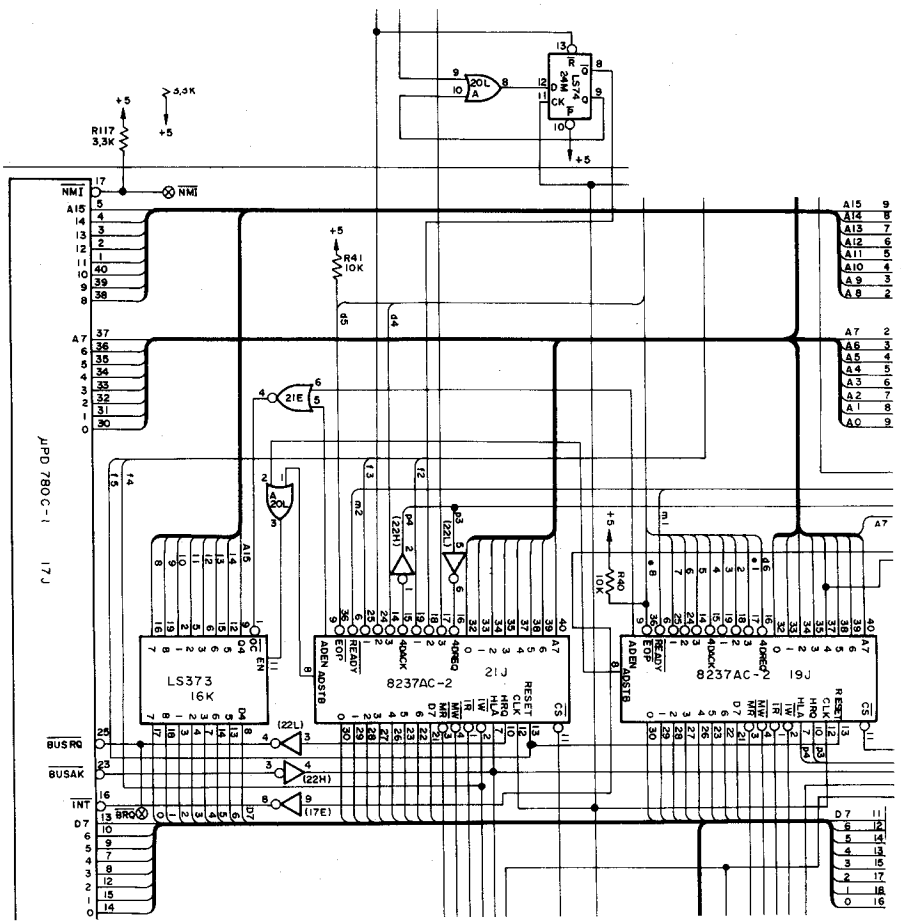


Fig. 4-51 DMA circuit

4.19 MEMORY CIRCUIT

4.19.1 Memory Address Map

The memory space comprises a resident RAM, a memory bank RAM, a P-ROM and a C-MOS RAM. Address allocation is as shown in Fig. 4-52 for power on, normal operation and use of C-MOS RAM.

The resident RAM area is selectable in 4 KB, 8 KB, 16 KB, 30 KB and 32 KB by the jumper wire on the main circuit board.

The P-ROM can be selected in 2 KB, 4 KB and 8 KB.

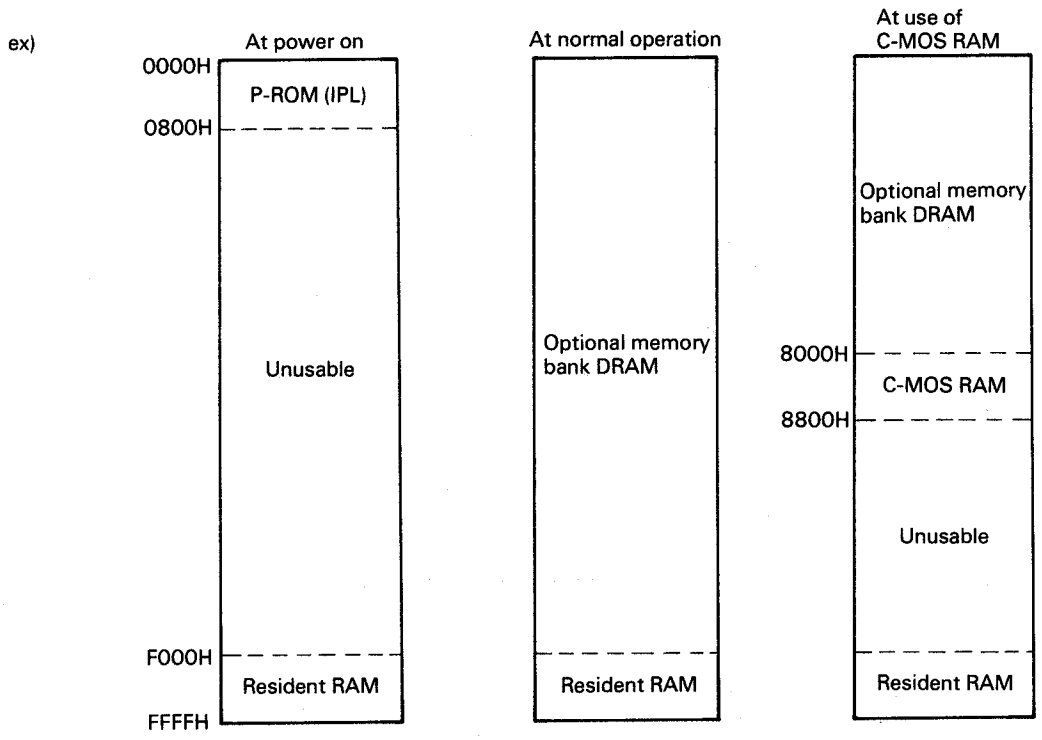


Fig. 4-52 Memory map

The resident RAM capacities of P-ROM and D-RAM are shown in Table 4-19 for each specification.

At power on, the CPU executes IPL (Intial Program Loader) stored in and after the address 0000H of P ROM, and allocates the addresses of the resident RAM area as shown in Fig. 4-53.

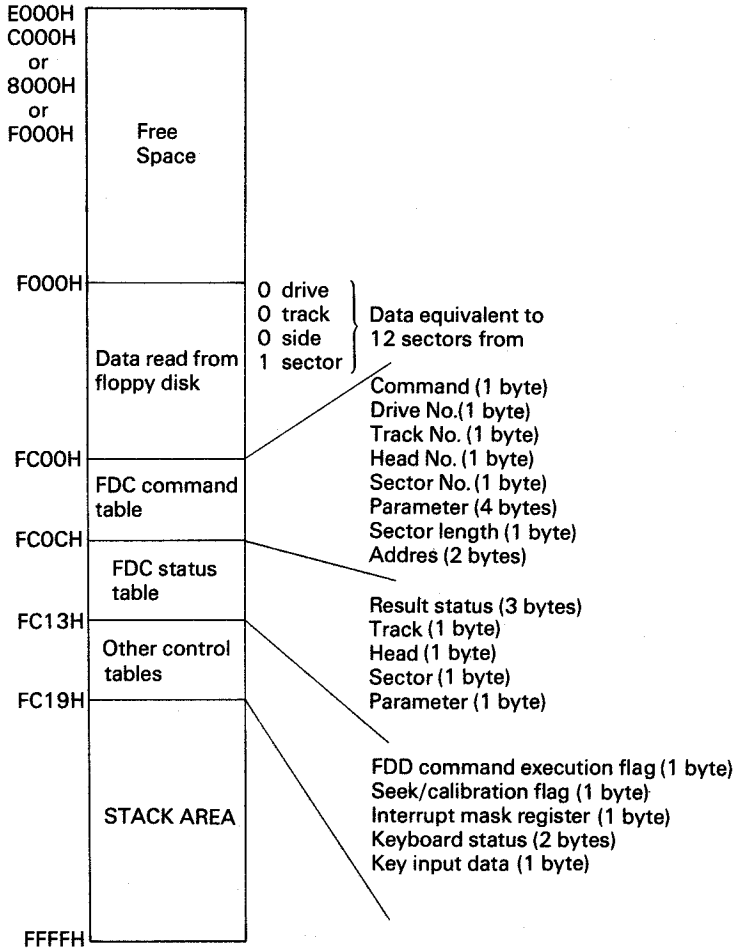


Fig. 4-53 Address Allocation of Resident RAM

	Model	QX-10 U.S.A. Specifications		QX-10 Europe Specifications		QC-10 Japan Specifications	
	Derivative version / Item	HASCI version	ASCII version	Standard version	Multifonts version	Standard version	Kanji version
ROM	IPL	U.S.A. specifications 2 KB 2716 × 1	←	Europe specifications 2 KB 2716 × 1	←	Japan specifications 2 KB 2716 × 1	←
ROM	Character generator (for display)	U.S.A. specifications 4 KB 2732 × 1	←	Europe specifications 4 KB 2732 × 1	←	Japan specifications 4 KB 2732 × 1	←
RAM	For Video	128 KB 64KRAM × 16	32 KB 16KRAM × 8	32 KB 16KRAM × 16	←	32 KB 16KRAM × 16	←
RAM	Main	256 KB 64KRAM × 32	64 KB 64KRAM × 8	64 KB 64KRAM × 8	192 KB* 64KRAM × 24	64 KB 64KRAM × 8	192 KB* 64KRAM × 24
RAM	Resident RAM	8 KB	←	8 KB	←	8 KB	←

*: Increase memory stage

Table 4-19

4.19.2 Setting of Resident RAM Capacity

The resident RAM capacity is set by the jumper wire J4 of the circuit shown in Fig. 4-54. The jumper wires and address wires are connected as shown in Table 4-20.

The resident RAM capacity is set as shown in Table 4-21.

The setting of each resident RAM capacity is described here.

Address line	Jumper wire
A11 + A12 + A13 + A14	B
A12	C
A13	D
A14	E

Table 4-20

Setting of Resident RAM Capacity (By J4)	Resident RAM capacity
Without jumper	32 kB
E	16 kB
E, D	8 kB
E, D, C	4 kB
B	All of the back of C-MOS RAM area (30kB)

Table 4-21

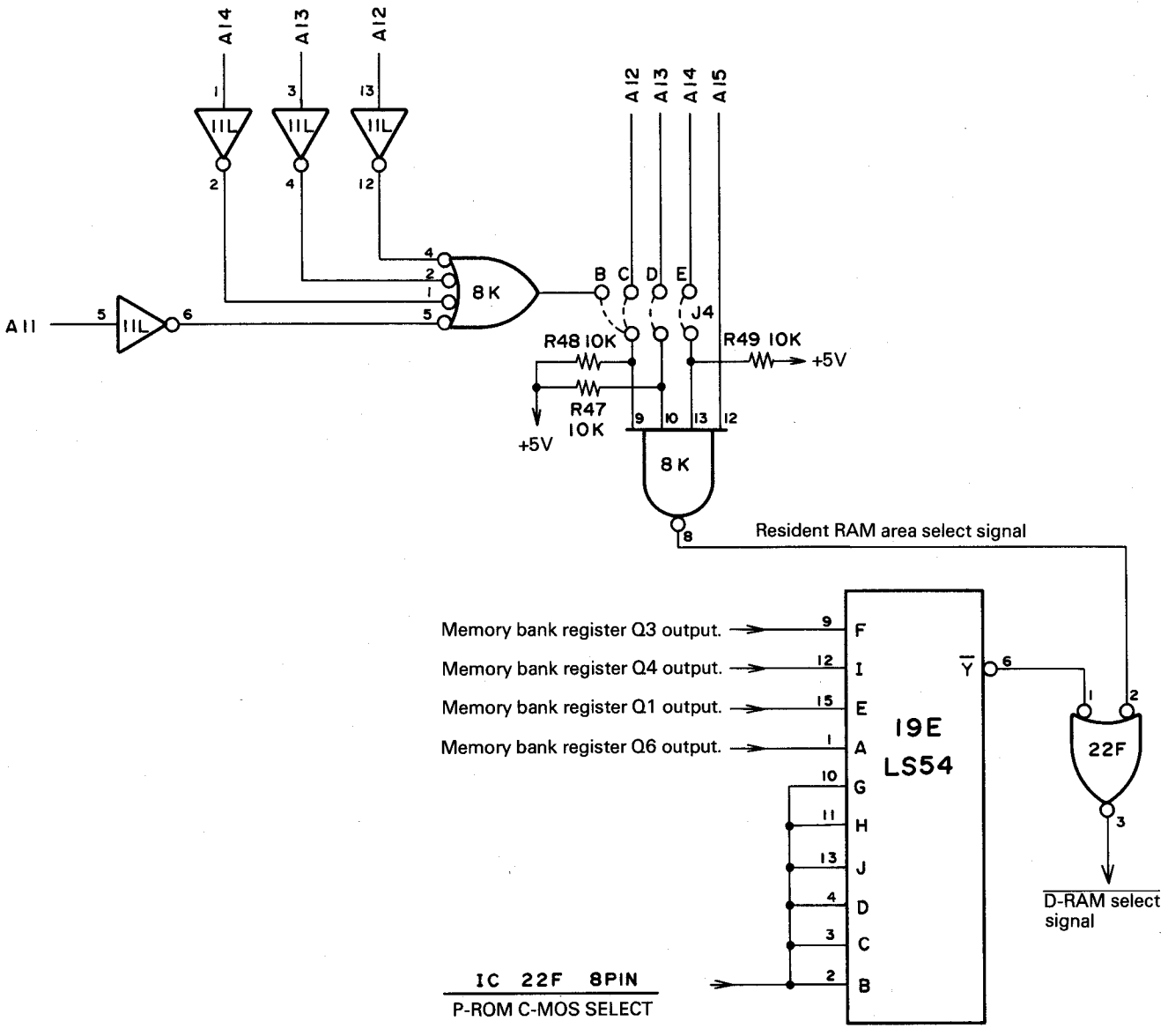


Fig. 4-54 Setting of Resident RAM Capacity (By J4)

(1) Setting the resident RAM capacity to 32 KB

When the resident RAM capacity is set to 32 KB, the resident RAM area is allocated to 8000H ~ FFFFH in the memory map as shown in Fig. 4-55. In this case, the jumper wire J4 is not used for connection.

Since only the most significant bit A15 of the address line is usually 1, when the addresses 8000H ~ FFFFH are specified, the output of pin 8 of IC8K is set to high level, and the outputs of pin 6 of IC21F and pin 3 of IC10K are set to high level in order to make the output of pin 3 of IC21F low level.

Finally, to make the $\overline{CS1}$ terminal of the C-MOS RAM μPD449, the C-MOS RAM set in the addresses 8000H ~ 87FFH is not selected and the resident RAM area is set.

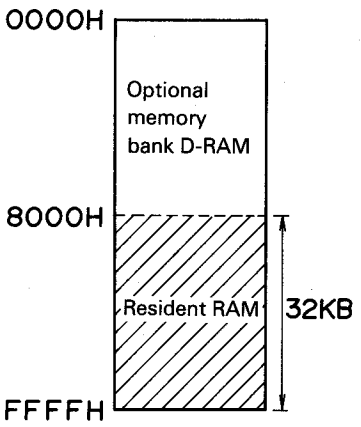


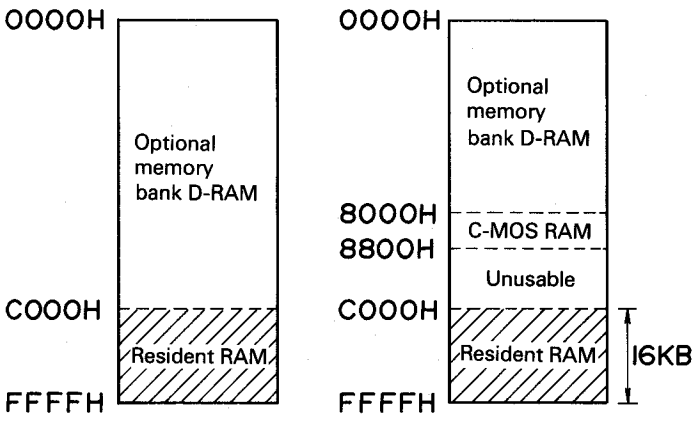
Fig. 4-55 Address map at setting resident RAM to 32 KB

(2) Setting the resident RAM capacity to 16 KB

When the resident RAM capacity is set to 16 KB, the resident RAM area is allocated to C000 ~ FFFFH in the memory map as shown in Fig. 4-56. When the C-MOS RAM is used, the C-MOS RAM area should be set to 2 KB in 8000 ~ 8800H.

Thus, only the E-terminal of the jumper wire J4 is used to set the resident RAM area and C-MOS RAM area as above described.

That is, when the resident RAM area is specified, the high-order two bits of the address lines A15 and A14 are usually "1", the input signals of pins 12 and 13 of IC8K are set to high level, and a low level signal is output from pin 8 and the C-MOS RAM is not selected.



(1) At normal operation (2) Use of C-MOS RAM

Fig. 4-56 Address map at setting resident RAM to 16 KB

On the other hand, when the C-MOS RAM area of 8000H ~ 87FFH is specified, the address line A14 becomes zero bit and the output of pin 8 of IC8K is set to high level.

All the inputs of IC21F are set to high level, and a low level signal is supplied from pin 3 of IC10K of the next stage, and the $\overline{CS1}$ terminal of the C-MOS RAM μPD449 (16M) is made active, providing the condition to select the C-MOS RAM.

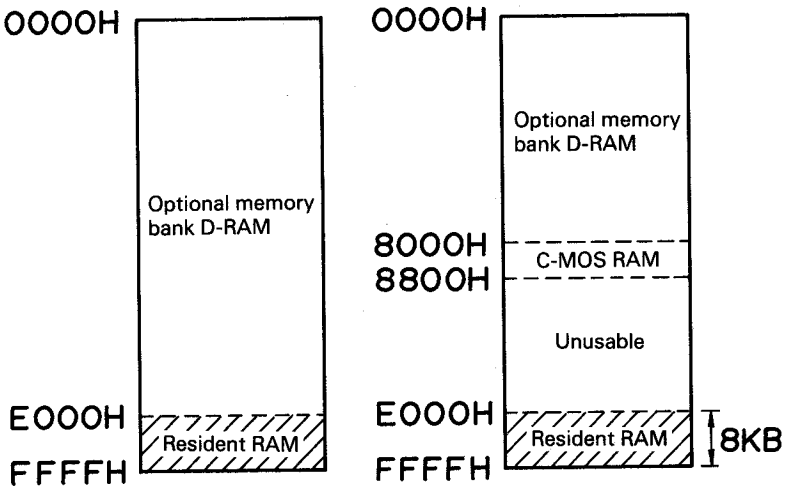
(3) Setting the resident RAM cpacity to 8 KB

The resident RAM area is allocated to 8 KB, E000H ~ FFFFH on the memory map. In this case, D and E terminals of the jumper wire J4 should be connected.

When the resident RAM area is specified, the high-order three bits of the address lines A15, A14 and A13 are usually "1", the output of pin 8 of IC8K is set to low level and the C-MOS RAM is not selected.

When the C-MOS RAM area is specified, only the bit the address A15 is set to "1", and A14 and A13 are "0".

The output of pin 8 of IC8K is set to high level making the CS1 terminal of the C-MOS RAM μPD449 (16M) active and enabling setting of the C-MOS RAM area.



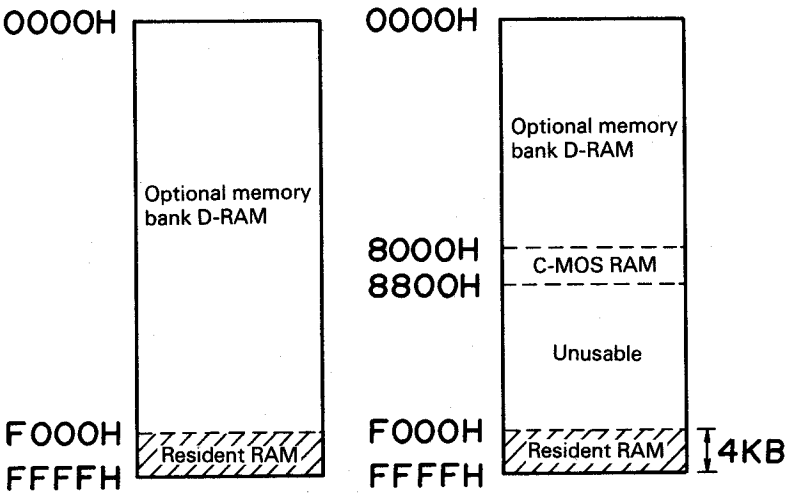
(1) At normal operation **(2) Use of C-MOS RAM**

Fig. 4-57 Address Map at Setting Resident RAM to 8 KB

(4) Setting the resident RAM capacity to 4 KB

The resident RAM are is allocated to 4 KB, F000 ~ FFFFH on the memory map. One of C, D and E terminals of the jumper wire J4 should be connected. As in the case of (3), when the resident RAM area address is specified, all the input bits of IC8K are set to "1", and the output of pin 8 is set to low level and the C-MOS RAM is not selected.

When the C-MOS RAM area is specified, all the signals except for the address line A15 are set to low level, and the output of pin 8 of IC8K is set to high level, making the $\overline{CS1}$ terminal of the C-MOS RAM μPD449 (16M) low level and enabling selection of the C-MOS RAM.



(1) At normal operation **(2) Use of C-MOS RAM**

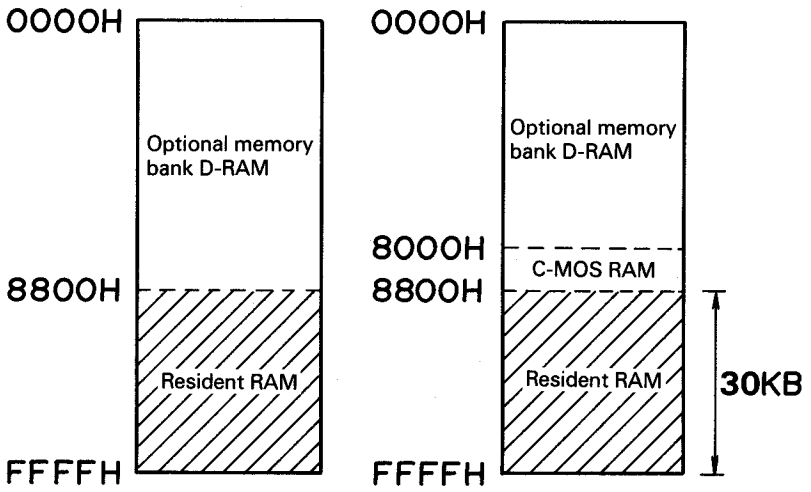
Fig. 4-58 Address Map at Setting Resident RAM to 4 KB

(5) Setting all memory areas after C-MOS RAM area to the resident RAM area

By connecting the B-terminal only of the jumper wire J4, set the C-MOS RAM area and resident RAM area to 8000H ~ 87FFH and 8800H ~ FFFFH respectively on the memory map.

The OR output of four address lines A11 ~ A14 is connected to the B-terminal of the jumper wire J4.

That is, when the addresses 8000H ~ 87FFH are specified, the output of pin 6 of IC8K is usually set to low level, and the output of pin 8 of IC8K is set to high level, making the C-MOS RAM μPD449 (16M) low level, and the C-MOS RAM is selected.



(1) At normal operation **(2) Use of C-MOS RAM**

Fig. 4-59 Setting All Memory Areas after C-MOS RAM Area to Resident RAM Area

When the addresses 8800H ~ FFFFH are specified, the output of pin 6 of IC8K is usually set to high level, making the $\overline{CS1}$ terminal of the C-MOS μPD449 (16M) high level. So, 8800H ~ FFFFH can be ensured for the resident RAM area without selecting the C-MOS RAM.

4.19.3 P-ROM Select Signal Supply Circuit

The $\overline{CS}$ signal to select P ROM (14M) for IPL is supplied by the D-type flip-flop LS74 (22K) of the circuit shown in Fig. 4-60. When the power is turned on, the power on reset signal is applied to the reset terminals of pins 1 and 13. Receiving this signal, the $\overline{Q}$-output of pin 6 of the flip-flop is set to high level and the Q-output of pin 9 is set to low level, respectively.

The output of pin 6 of the NAND gate formed by IC21F is set to high level. This signal is applied to pin 1 of IC21F. Then, the AND of this signal, the input signal of pin 2 or D-RAM select signal (D-RAM is not selected and set to high level then) and the output signal of pin 6 of flip-flop LS74 (22K) is taken.

A low level signal is supplied from the output of pin 12 of IC21F to the P-ROM (14M), and the P-ROM is selected.

After IPL by selecting the P-ROM, the I/O address 1CH is specified and "1" is set to the least significant bit "D0" of the data line, thereby setting the $\overline{Q}$-output of pin 6 of flip-flop LS74 (22K) to the low level, and the $\overline{CS}$ signal to the P-ROM is set to high level and the memory map is transferred from the P-ROM area to the D-RAM area.

4.19.4 C-MOS RAM Select Signal Supply Circuit

The C-MOS RAM μPD449 (16M) which is used for writing the data such as a stack point at power down is selected by the CPU when the interrupt made by detection of PWD signal is received.

That is, receiving this interrupt, the CPU outputs the I/O address 20H to the low-order of the address bus in order to select the C-MOS RAM, and supplies a low level signal to pin 4 of IC23F, where the $\overline{IOWR}$ signal from the CPU is connected to the input of pin 5 of IC23F. The AND of these signals is supplied to pin 11 of flip-flop LS74 (22K).

The data line "D0" bit is connected to the D input terminal (pin 12) of this flip-flop. By setting "1" in this bit, a high level signal is output from the Q-output of pin 9 to the input of pin 5 of IC21F.
After supplying the I/O address to the C-MOS RAM, the CPU outputs the C-MOS RAM area 8000H ~ 87FFH onto the address line. At this time, the address line A15 is usually at high level and the input of pin 4 of IC21F connected with the address line A15 is also set to high level.
The input of pin 3 of IC21F is connected to the resident RAM select signal. Since this signal is set to high level when the C-MOS RAM area is specified, a low level signal is output from pin 6 of IC21F and a low level signal is supplied from pin 3 of IC10K. That is, the active low $\overline{CS1}$ signal of the C-MOS RAM μPD449 (16M) is supplied from this signal, and the C-MOS RAM is selected.

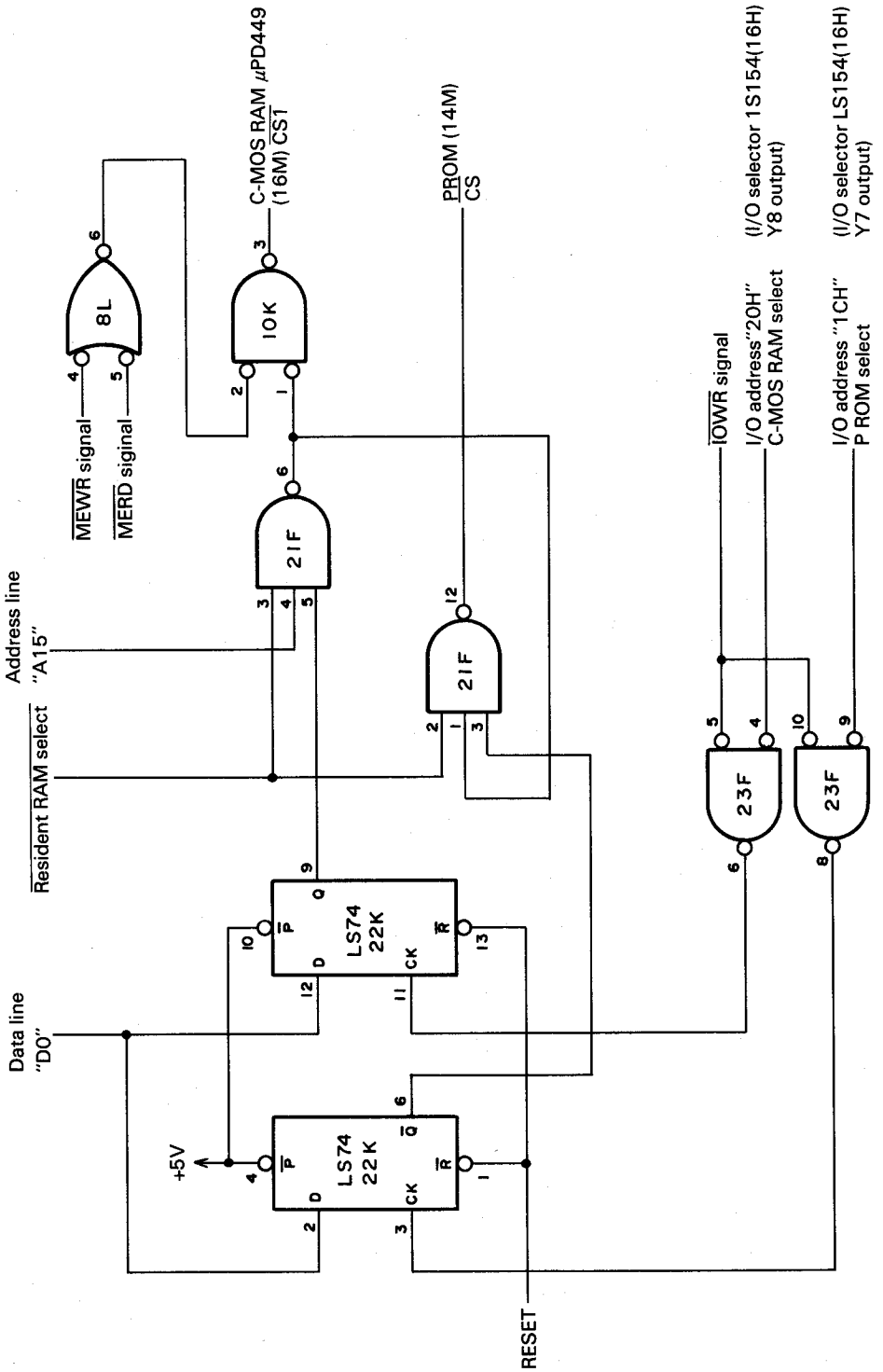


Fig. 4-60

4.19.5 D-RAM

The CPU (μPD780) can directly access a memory of 64 KB maximum through 16 address buses. The QX-10 has four memory banks (#0 ~ #3) and provides a memory capacity of 256 KB maximum by switching the memory bank register.

The memory bank configuration is shown in Fig. 4-61.

The memory bank #0 is usually selected by IPL after the power is turned on. The capacities of each memory bank can be selected by the jumper wire provided on the main board.

The relationship between the jumper wire connection and memory capacities is shown in Table 4-22.

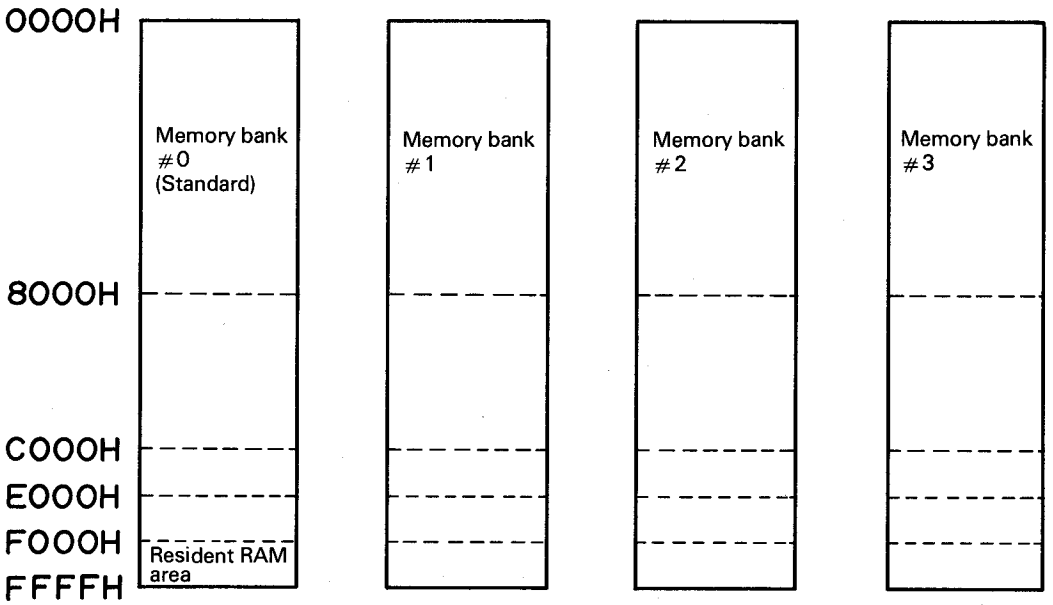


Fig. 4-61 Memory Banks

Jumper wire-connection	Memory Capacity
———	32KB
E	16
E, D	8
E, D, C	4
B	30

Table 4-22 Jumper Wire Connection and Memory Capacities

Memory banks #0 ~ #3 are selected by the memory bank register allocated to the I/O address 18H. The memory bank size depends on the resident RAM capacity. As the resident RAM area is increased, the memory bank capacity is decreased.

The D-RAM circuit configuration is described next.

4.19.6 D RAM Select Signal Supply Circuit

The D RAM select signal is supplied by the circuit shown in Fig. 4-62. LS74 (19E) comprises four internal AND gates, an OR gate to get the OR of the outputs of these gates, and an inverter. The memory bank register output is connected to the inputs of four AND gates.

An active low D-RAM disable signal is connected to the other inputs of these AND gates.

Therefore, when the memory bank is specified, the Y-output of LS54 (19E) is set to low level and the active low D-RAM select signal is supplied from the output of pin 3 of IC22H.

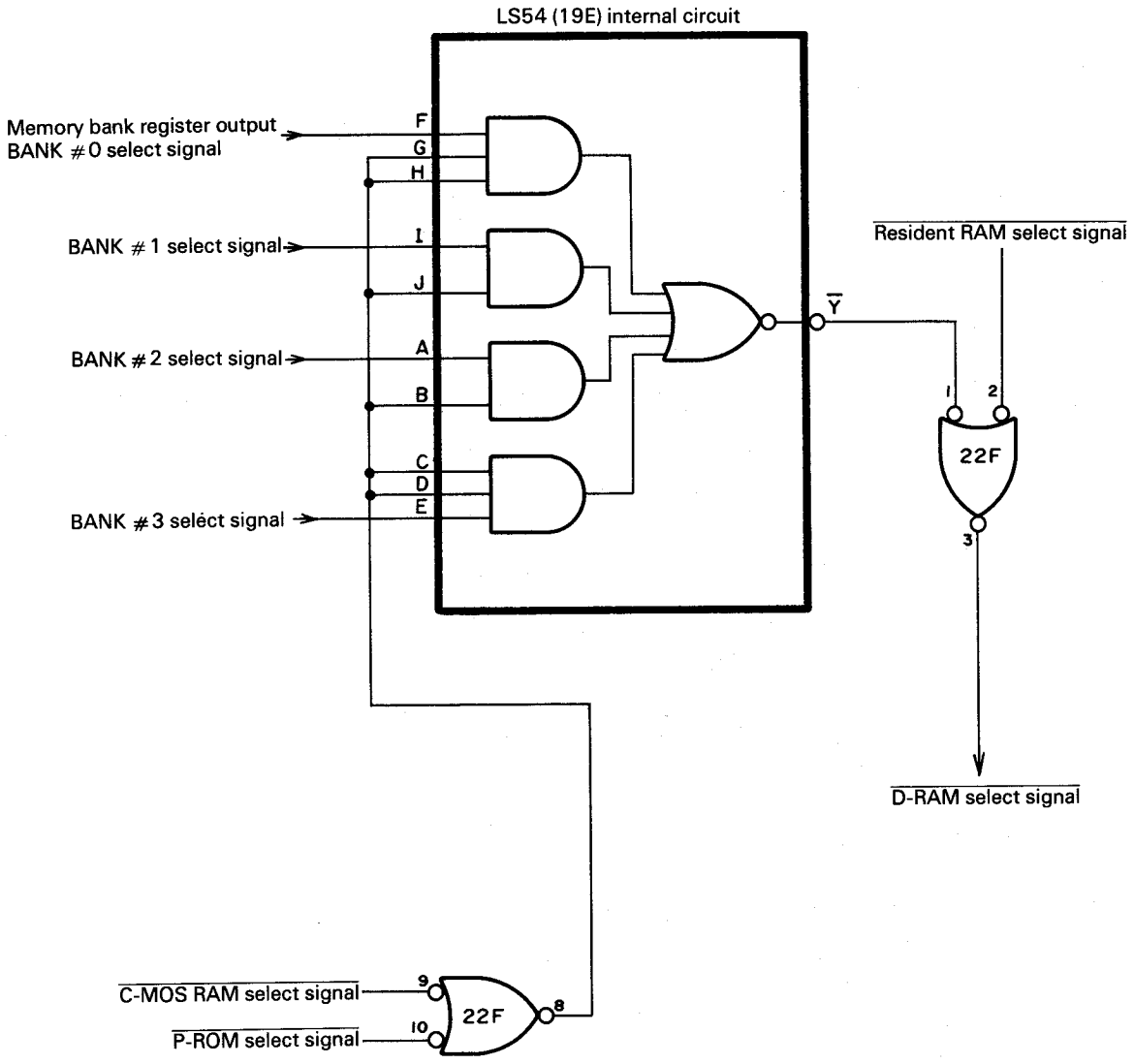


Fig. 4-62 D RAM Select Signal Supply Circuit

4.19.7 D-RAM Bank Selector

Since the CPU μPD780 has a16-bit address bus, it can access addresses of up to 64 KB at a time.

The QX-10 uses the 64K-bit dynamic RAM μPD4164-3 to ensure a large capacity, and has four banks with different specifications as shown in Table 4-19, enabling it to control a memory of 256 KB (64 KB × 4) maximum.

These memory banks are selected by the D-type FFs LS273 (18F) which is used as a memory bank register as shown in Fig. 4-63.

That is, this memory bank register is allocated to the I/O address 18H. An active low signal is output from the Y-6 terminal (pin 7) of the I/O selector LS154 (16H), and the OR of this signal and the $\overline{IOWR}$ signal from the CPU is taken by gate IC23F, and the output of this gate is used as a clock signal of the memory bank register LS273 (18F). The memory bank register is made active by this, and when it receives the bank select data input sent together with the I/O address 18H, it sets the bit of the bank to be selected in the output side.

As for the data corresponding to the I/O address 18H, since the memory bank register select signal is allocated to the high-order four bits out of eight bits and "1" is set in the bit corresponding to the memory bank to be selected, only one of Q1, Q3, Q4 and Q6 outputs must be a high level output even in the output side.

The memory bank select signal goes through the NAND gate of IC19F and OR gate formed by IC17F and IC18F, through which AND of this signal, RAS signal and PRI signal is taken.

One of these outputs supplies the $\overline{RAS}$ signal of one memory bank. Therefore, only the memory bank with the $\overline{RAS}$ supplied to it is selected as a direct access memory of the CPU.

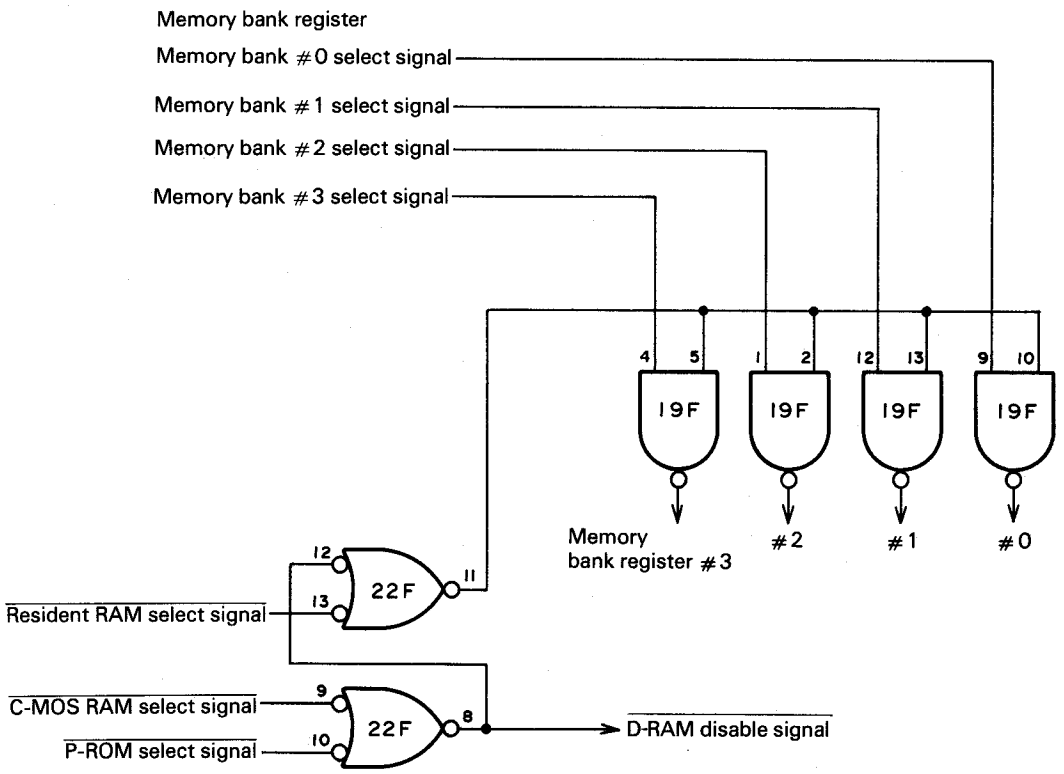


Fig. 4-63 Memory Bank Specify Gate Circuit

4.19.8 RAS Precharger

RAS and CAS signals are given to the D RAM at the timing shown in Fig. 4-64. In this case, the RAS signal is set to low level in the refresh cycle to refresh the D-RAM.

To define the trailing edge of the $\overline{RAS}$ signal in refreshing, it is necessary to fasten the leading edge of the $\overline{RAS}$ signal in OP code fetching to secure the pulse width shown in Fig. 4-64.

The two-stage flip-flop LS73 (20M) in the circuit shown in Fig. 4-65 is used for this purpose. It fastens the leading edge of the $\overline{RAS}$ signal to prolong the high level period of the signal double, about 0.14μsec.

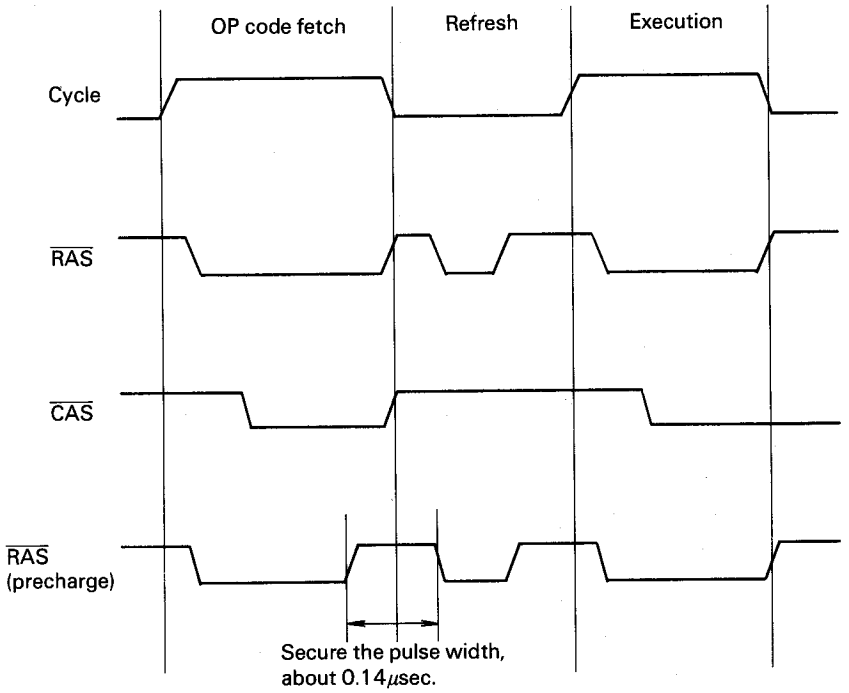


Fig. 4-64 D RAM RAS/CAS Signals Timing

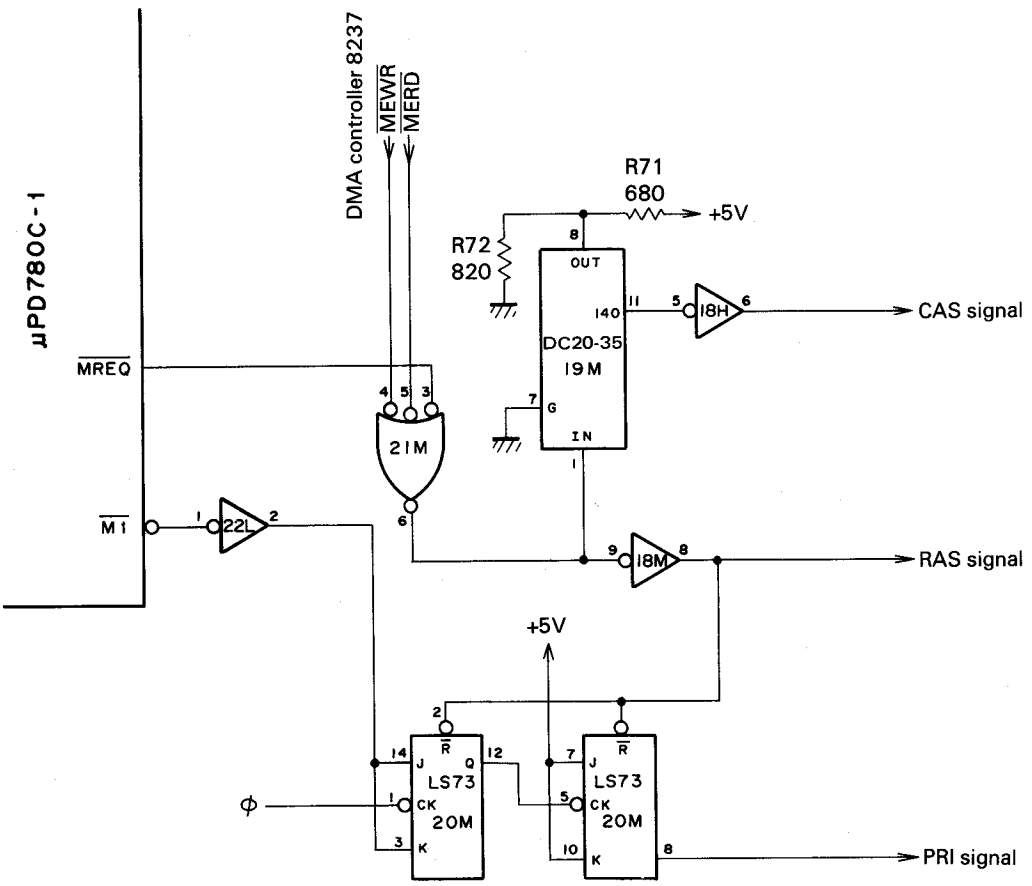
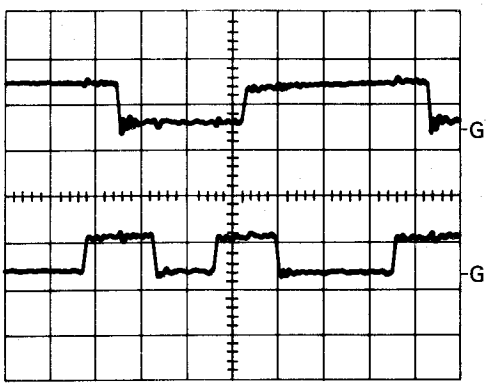
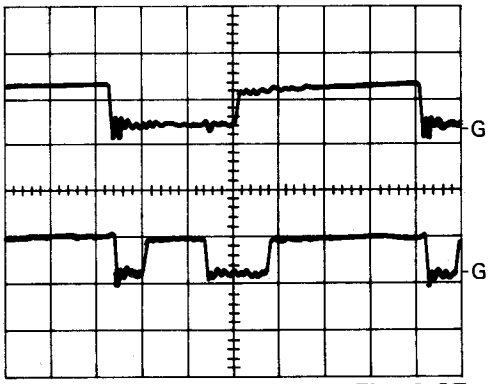


Fig. 4-65



Upper: M1
Lower: D RAM RAS
sweep 0.1 μsec 5V/div.

Fig. 4-66



Upper: M1
Lower: RAS
Sweep 0.1 μsec 5V/div.

Fig. 4-67

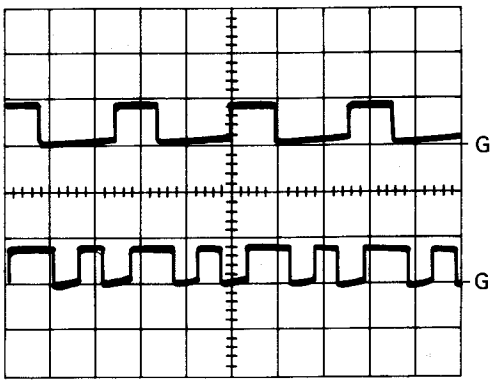
4.19.9 RAS/CAS Signal Supply Circuit

Address allocation of 64 KB RAM is made by dividing into high-order and low-order bits and accompanied by strobe signals called RAS (Row Address Select) and CAS (Column address select). The circuit shown in Fig. 4-65 is used for supply of RAS and CAS signals from the CPU.

The $\overline{RAS}$ signal is supplied by $\overline{WR}$, $\overline{RD}$ and $\overline{MREQ}$ signals output from the CPU. That is, address allocation to the D RAM is made when the $\overline{MREQ}$ signal is active and the $\overline{WR}$ or $\overline{RD}$ signal is active.

These signals are supplied through the gate of IC21M.

The $\overline{CAS}$ signal is obtained by applying the output of pin 6 of IC21M which is supplied as a $\overline{RAS}$ signal to the delay element IC19M to delay the signal 140 nsec.



Upper: RAS
Lower: CAS
Sweep 0.5 μsec. 5V/div.

Fig. 4-68

4.19.10 Gate circuit for Supplying $\overline{WE}$ Signal to D RAM

$\overline{WE}$ signal to DRAM is supplied by the gate circuit shown in Fig. 4-71.

► NON DMA transmission

As pin 2 input of IC23K is always low-level, pin 3 output of IC23K is high level, and $\overline{WE}$ signal to D RAM is controlled by only $\overline{MEWR}$ signal.

The timing chart in this time is shown in Fig. 4-69.

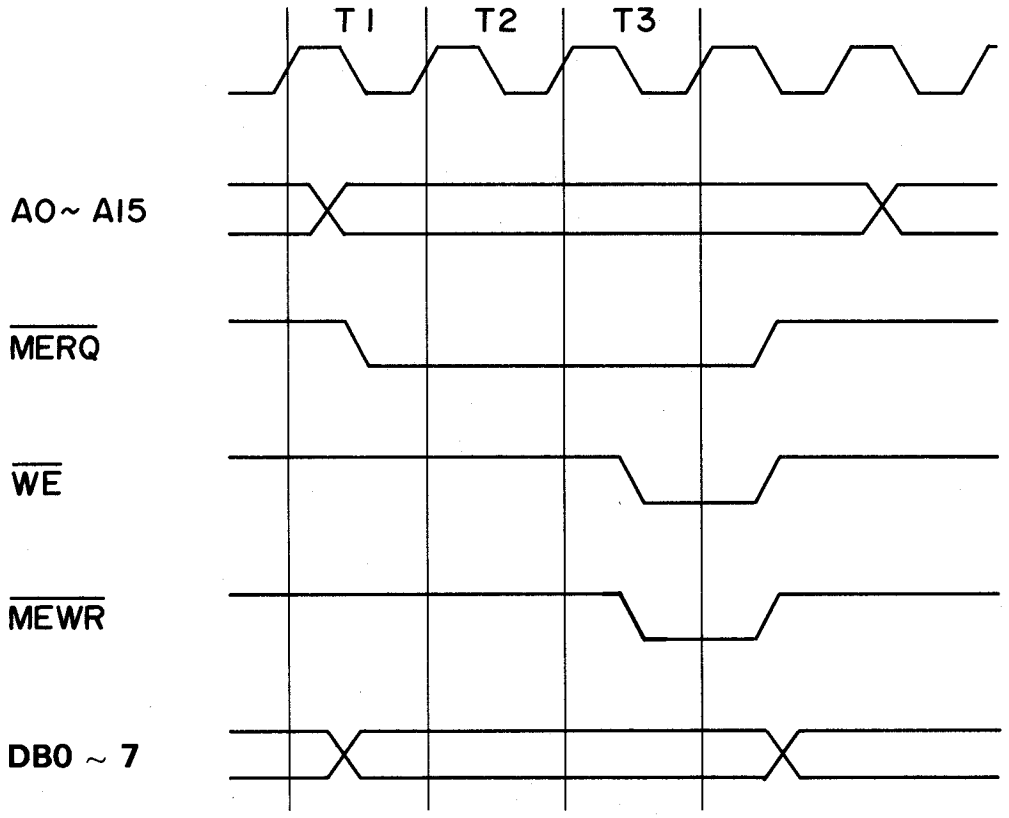


Fig. 4-69

► DMA transmission

In DMA transmission, data writing to the memory must be performed guaranteeing therefore, $\overline{WE}$ signal is supplied to D RAM with the two flip-flop of the circuit shown in Fig. 4-71 being late for 3 clocks from the trailing edge of $\overline{MEWR}$ signal.

The timing chart in this time is shown in Fig 4-70.

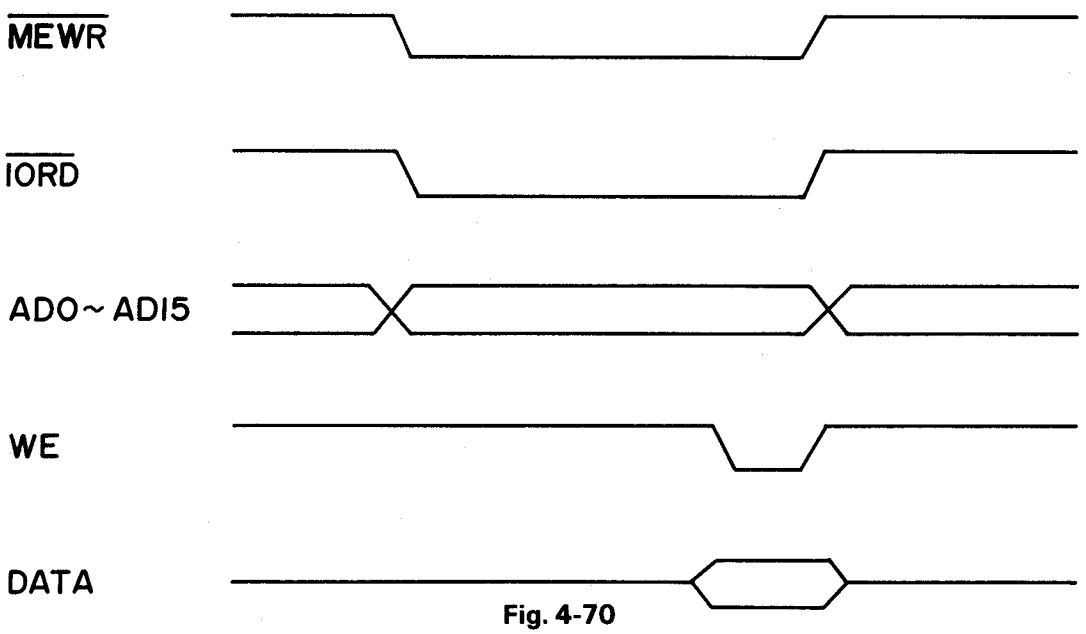


Fig. 4-70

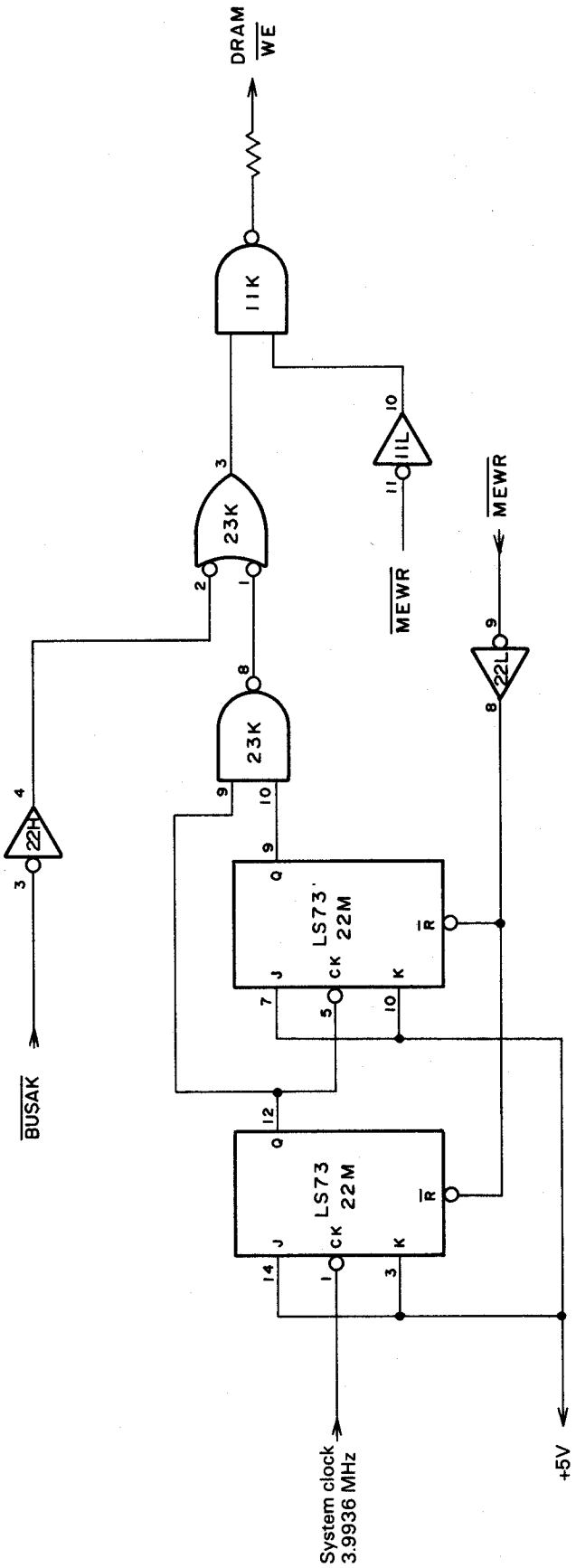


Fig. 4-71 D-RAM $\overline{WE}$ signal supply circuit

4.19.11 D-RAM $\overline{RAS}$ Signal supply gate circuit

The $\overline{RAS}$ signal applied to the D-RAM is supplied through the gate which takes the AND of the $\overline{RAS}$ and PRI signals supplied from the CPU through the delay element and the bank select signal supplied from the memory bank register.

The timing of input/output of the gate in the M1 cycle is shown in Fig. 4-73. The $\overline{RAS}$ signal of the memory bank selected in the M1 cycle is made active low at OP code fetching and refreshing. (RAS ONLY REFRESH)

The $\overline{RAS}$ signal of the memory bank not selected is made active low only at refreshing. At this time, all the D-RAMs are refreshed.

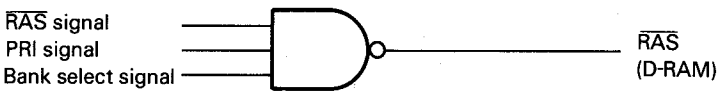


Fig. 4-72

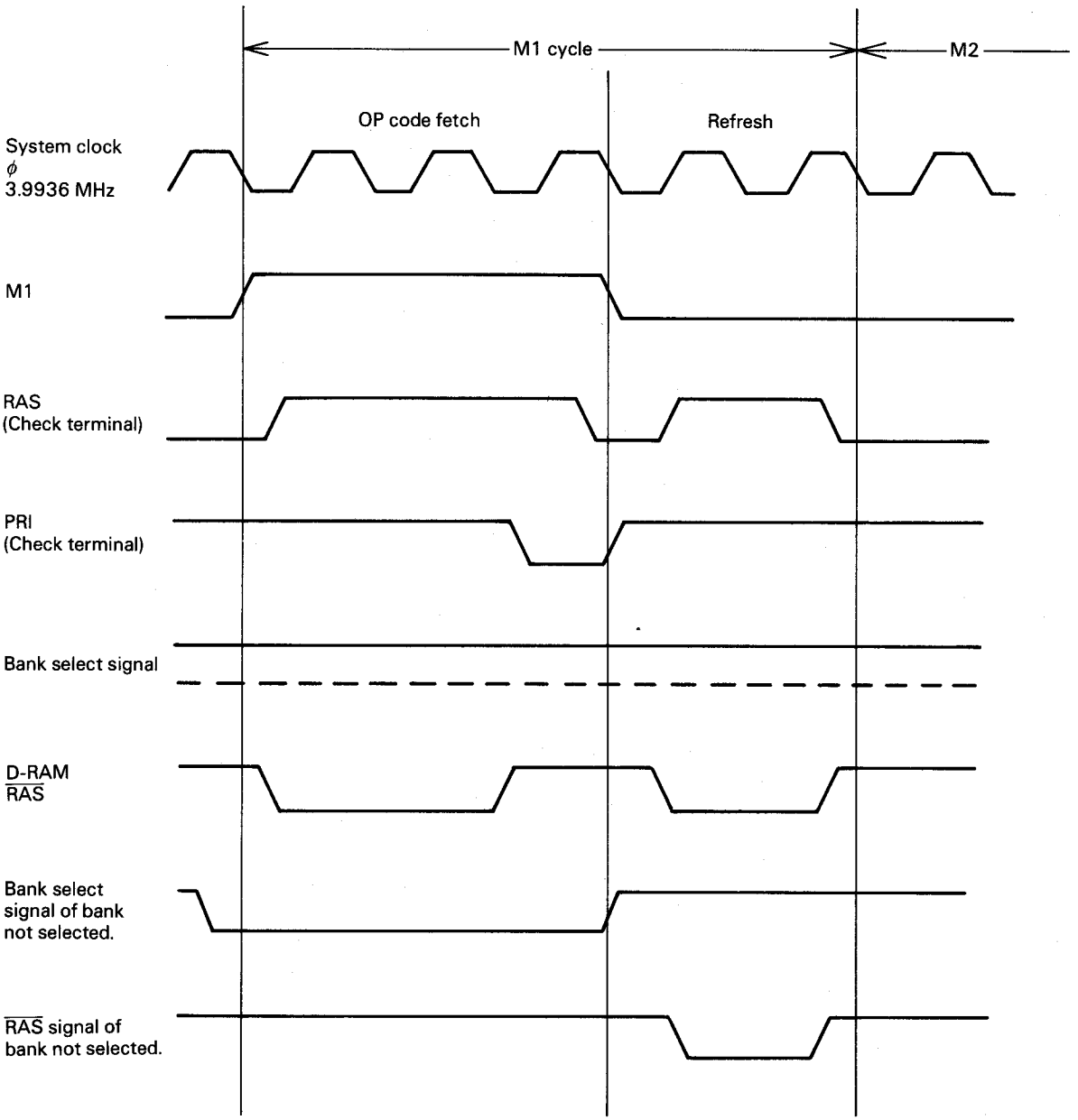
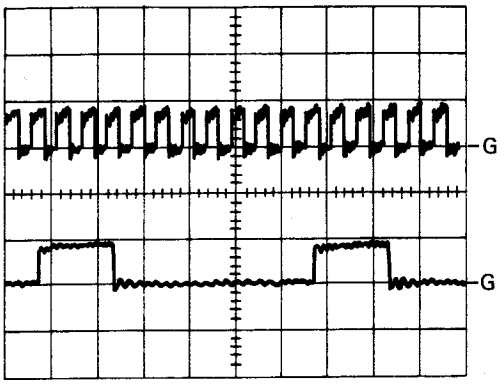
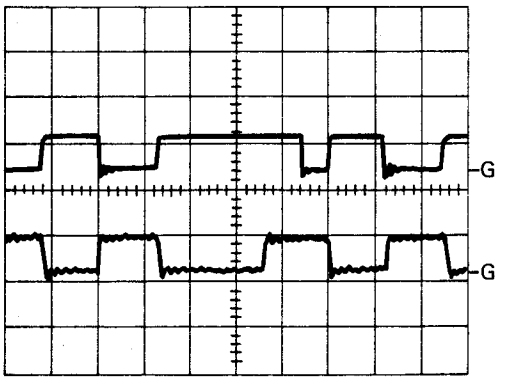


Fig. 4-73



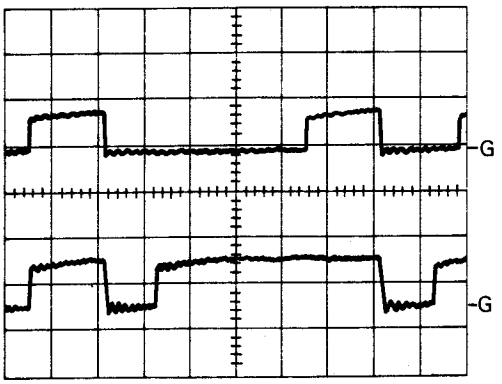
Upper: System clock
ϕ3.9936 MHz
Lower: M1
(Sweep 0.5μsec. 5 v/div.)

Fig. 4-74



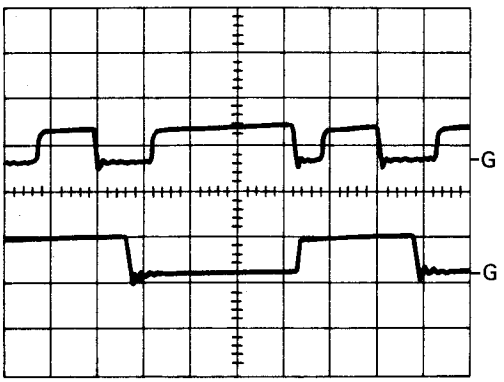
Upper: $\overline{RAS}$
Lower: $\overline{RAS}$
(Bank select)
(Sweep 0.2 μsec 5V/div)

Fig. 4-77



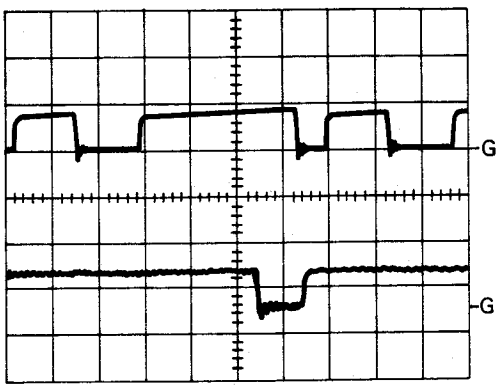
Upper: $\overline{M1}$
Lower: $\overline{RFSH}$
(μPD780, Pin 28)
(Sweep 0.5μsec. 5 v/div.)

Fig. 4-75



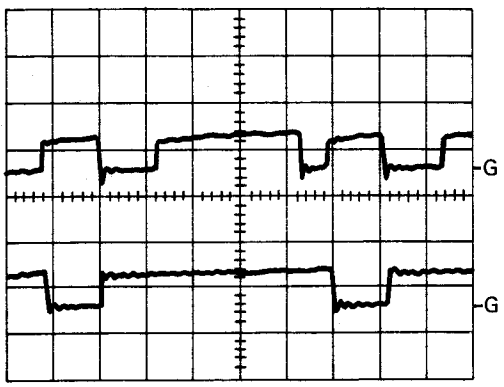
Upper: RAS
Lower: Bank not selected
Pin 13 of IC11H
(Sweep 0.2μsec. 5 v/div.)

Fig. 4-78



Upper: RAS
Lower: PRI
(Sweep 0.2 μsec 5V/div)

Fig. 4-76



Upper: RAS
Lower: Pin 12 of IC 11H
Bank not selected
(Sweep 0.2 μsec 5V/div)

Fig. 4-79

4.19.12 D-RAM $\overline{CAS}$ Signal Supply Gate Circuit

The $\overline{CAS}$ signal applied to the D RAM is supplied by AND of RAS, CAS and $\overline{RFSH}$ signals applied to the gate circuit shown in Fig. 4-80. In this case, the timing in the M1 cycle is as shown in Fig. 4-81. The D RAM is refreshed by the $\overline{RAS}$ signal. The $\overline{CAS}$ signal is set to high level during the refresh period.

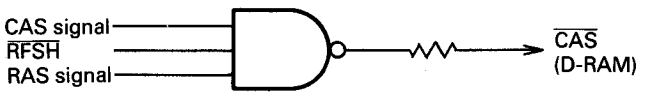


Fig. 4-80

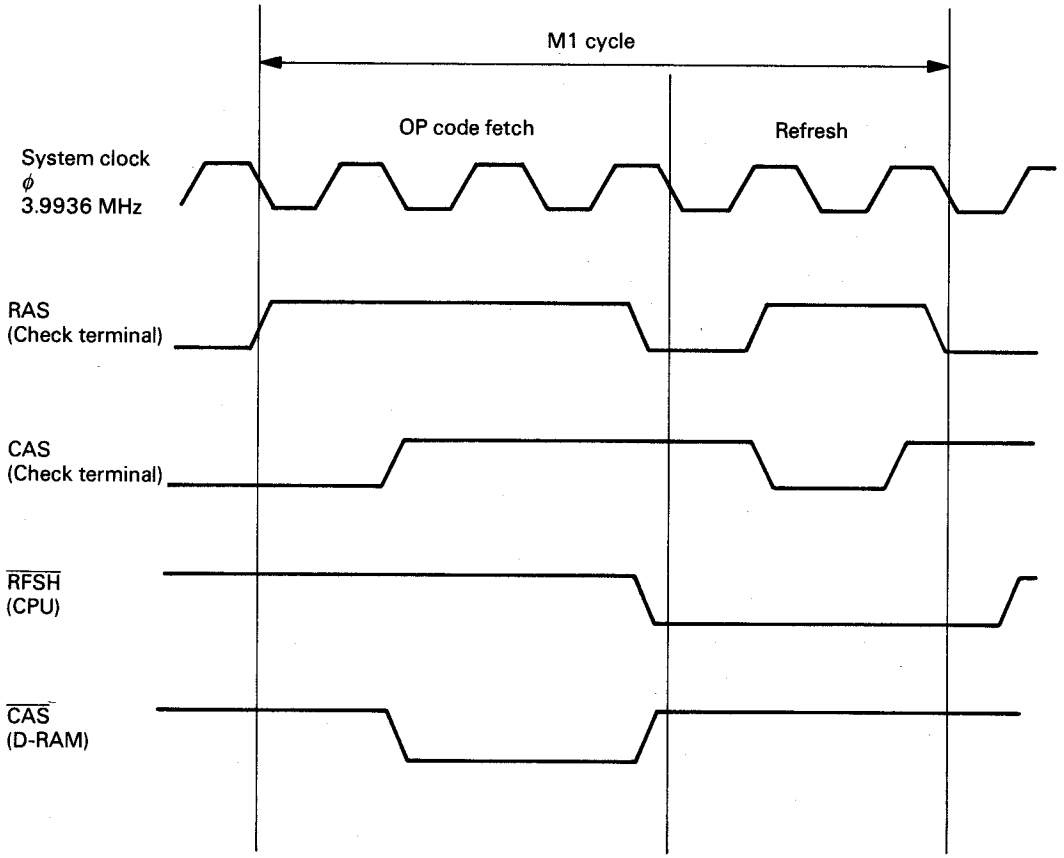
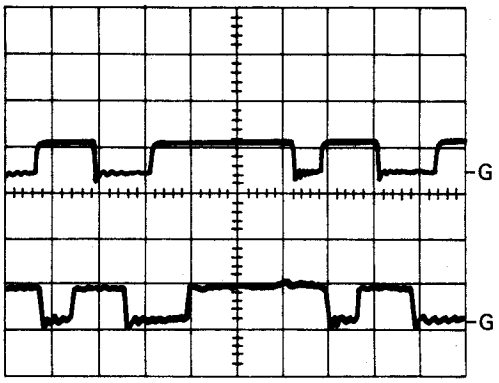
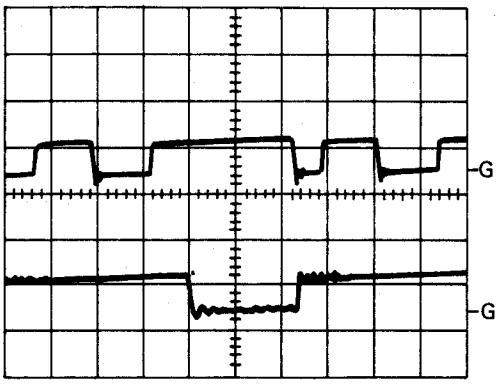


Fig. 4-81



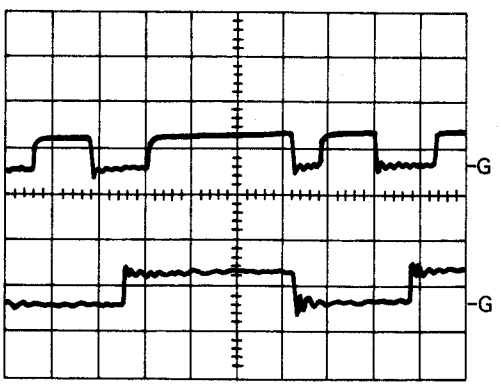
Upper: RAS
Lower: CAS
(Sweep 0.2μsec. 5 v/div.)

Fig. 4-82



Upper: $\overline{RAS}$
Lower: $\overline{WE}$ (D-RAM)
(IC12 Pin 72)
(Sweep 0.2 μsec. 5V/div.)

Fig. 4-84



Upper: $\overline{RAB}$
Lower: $\overline{RFSH}$
(IC12J Pin 12)
(Sweep 0.2μsec. 5 v/div.)

Fig. 4-83

4.19.13 Data Input/Output Control

Data input/output to the D-RAM is made through the 3-state bus buffer LS244 (7H and 6H). Input/output is controlled by 1G and 2G terminals.

The 2G terminal is connected to the ground.

Therefore, the 2G terminal is usually at low level, and the input data from the data bus is output as a data to be written into the D-RAM as it were.

AND of the D-RAM select signal and $\overline{\text{MERD}}$ signal from the CPU is applied to the 1G terminal. The signal controlled by the input signal to the 1G terminal, that is, the data to be read out from the D-RAM, is selected by the D-RAM $\overline{\text{MERD}}$ signal is active.

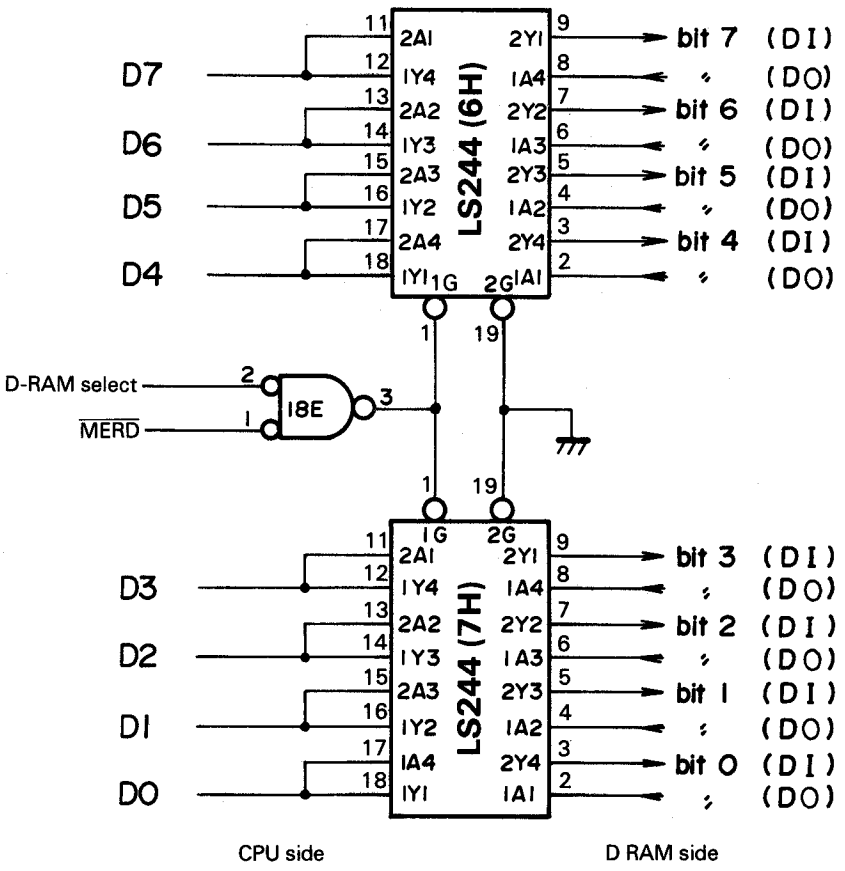


Fig. 4-85

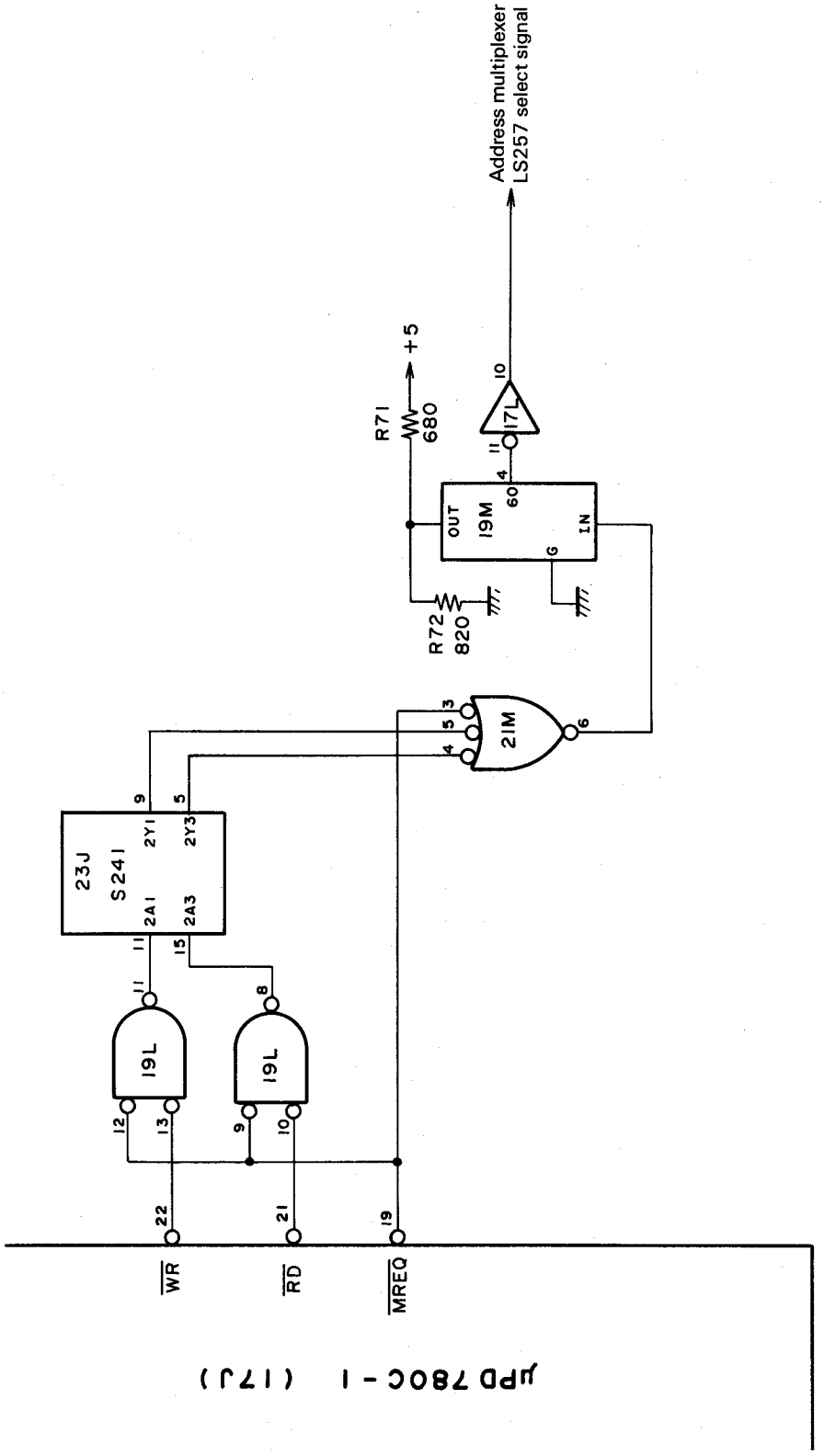


Fig. 4-86 D-RAM Address Multiplexer LS257 (7J, 8J, 9J, and 11J) Select Signal Supply Circuit

4.19.14 Refresh Circuit

The D-RAM stores one-bit information in correspondence with charge/discharge of one condenser. Therefore, the stored data will disappear in time.

Thus, a refresh operation is necessary to re-store the same data before it disappears.

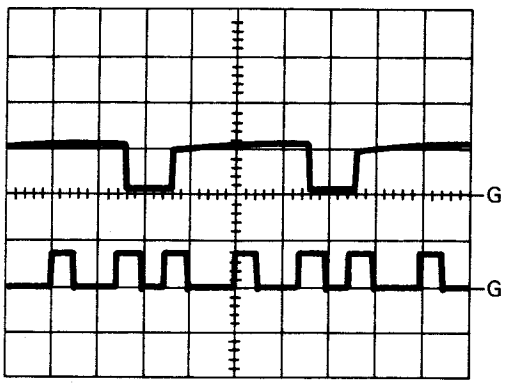
For this purpose, a refreshing address and a refresh instruct signal ($\overline{RFSH}$) are generated by utilizing the idle time during decoding inside after the CPU reads an instruction code.

In this system, by taking AND of $\overline{RFSH}$, $\overline{RAS}$ and PRI signals, the $\overline{RAS}$ signal is supplied to the D-RAM in synchronization with the $\overline{RFSH}$ signal output from the CPU, and it is used as a refresh signal.

As a refresh address, the low-order address is selected by the $\overline{RAS}$ signal.

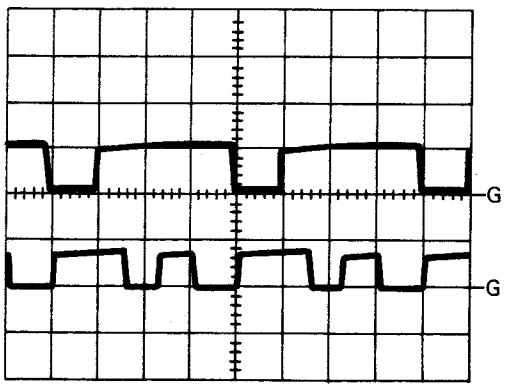
This refresh method is called RAS ONLY REFRESH.

The timing chart is shown in Figs. 4-87 and 4-88.



Upper: $\overline{RFSH}$ (CPU)
Lower: RAS (D-RAM)
Sweep 0.5 μsec.
5V/div.

Fig. 4-87



Upper: $\overline{RFSH}$ (CPU)
Lower: CAS (D-RAM)
Sweep 0.5 μsec.
5V/div.

Fig. 4-88

4.19.15 External Memory Select Signal Supply Circuit

The select signal to external optioned memory is supplied by the gate output from PIN 8 of IC 20F shown in Fig. 4-89.

When external memory is selected, memory in main unit must never be selected. For this reason, the select inhibit in signal to P-ROM, D-RAM and C-MOS RAM respectively and the select signal to the external memory are connected with the gate input of IC 20F.

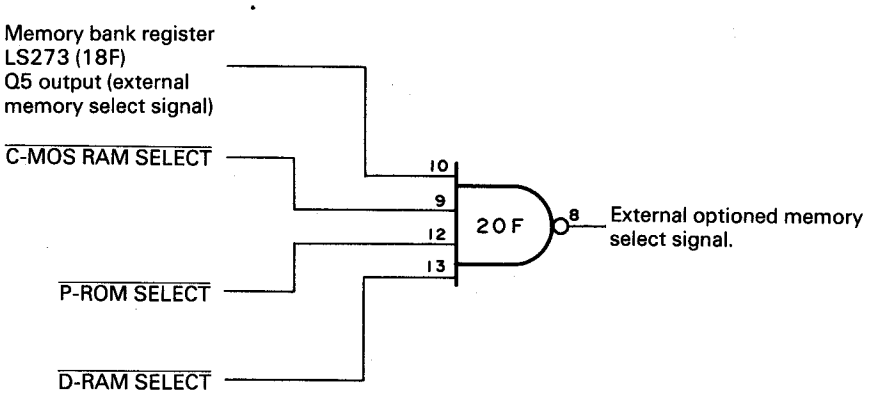
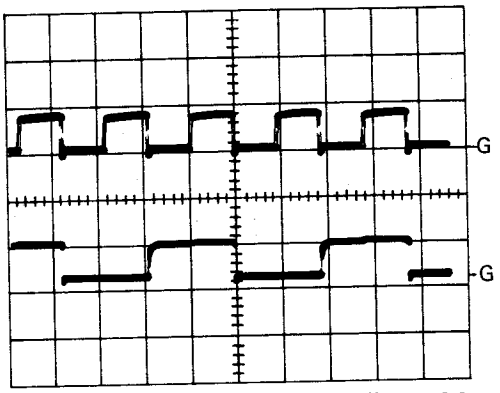
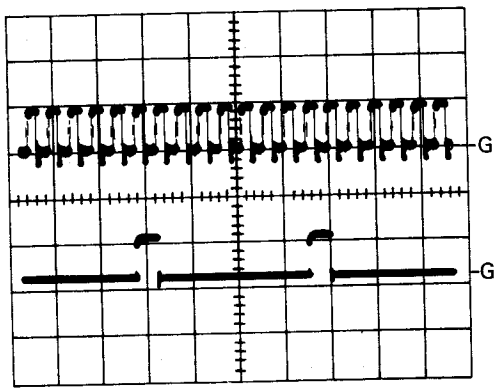


Fig. 4-89 External memory select supply circuit



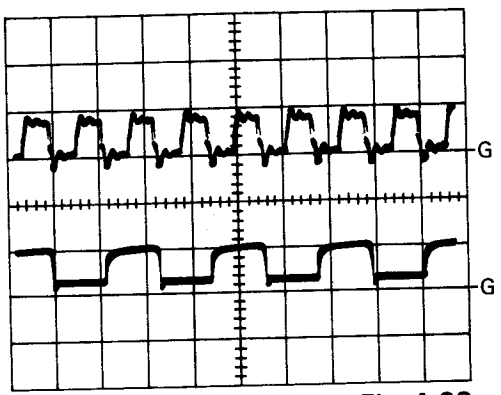
IC19H
Upper: 2QC output (pin 9)
Lower: 2QD output (pin 8)
(Sweep 0.5 μsec 5V/div)

Fig. 4-90



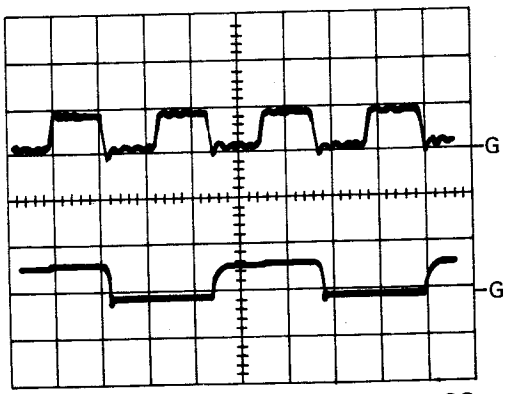
μPD765
Upper: φ (pin 19)
Lower: WCLK (pin 21)
(Sweep 0.5 μsec 5V/div)

Fig. 4-91



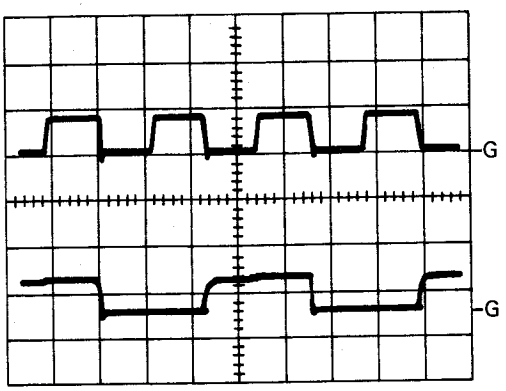
IC19H/LS393
Upper: 2A input (pin 13)
Lower: 2QA (pin 11)
(Sweep 0.1 μsec 5V/div)

Fig. 4-92



Upper: 2QA output (pin 11)
Lower: 2QB output (pin 10)
(Sweep 0.1 μsec 5V/div)

Fig. 4-93



Upper: 2QB output (pin 10)
Lower: 2QC output (pin 9)
(Sweep 0.2 μsec 5V/div)

Fig. 4-94