October 1983

Diskless Computers Emerge With Proper Mix of Firmware, Processor, and Bubble Memory

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ORDER NUMBER 230861-001

DISKLESS COMPUTERS EMERGE WITH PROPER MIX OF FIRMWARE, PROCESSOR, AND BUBBLE MEMORY

A CP/M-86 operating system on a chip, a 16-bit microprocessor, and bubble memory oust floppy disks from portable computers.

SMALL COMPUTERS

If one thing can be said about portable personal computers, it is that few are truly easy to carry or move—a consequence, in large part, of their integral floppy-disk drives. Of course, the storage capacity afforded by floppy disks is a necessity, as personal computers must be able to hold an operating system, transport application programs, and maintain enough data files to support those programs. To be truly portable, however, a PC must be small, lightweight, and power-thrifty—without sacrificing any of the functions, performance, or storage of their desktop counterparts.

Exit the sacrifices, enter the operating system processor—a two-chip set comprising an 80186, 16-bit microprocessor and the 80150 CP/M-86 operating system kernel. Add a bubble memory and some dynamic RAM to the chip set, designated the iAPX 186/50, and all the elements of a diskless, truly portable personal computer—including the operating system—are in place (Fig. 1).

Flexibility is a key advantage of the configuration, as the nucleus can be modified to specific situations. The 80186 microprocessor, for instance, simplifies system construction because it incorporates direct memory access, a timer, an interrupt controller, chip-selection logic, circuits that generate ready signals, and many peripheral interfaces. Most important is the modular architecture of its CPU, which permits resident silicon code to be adapted to or combined with code written by the user—all of it driving bubble memory and other peripheral devices.

The large amount of firmware means that the iAPX 186/50 system could conceivably operate without a single line of user-written code. However, when bubble memory or other external parts are added, a designer must develop some custom drivers, which will be linked during initialization. Although the code within the operating system kernel cannot be modified, an OEM designer has the option of attaching the 80150 to any 16-kbyte boundary of memory (except the highest, FC000H, or the lowest, 00000H).

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sists of three parts: the console command processor, or CCP; the basic disk operating system, or BDOS; and the basic I/O system, or BIOS. The processor interprets command lines and executes five built-in commands, such as DIR (list directory). It can format floppy disks, transfer files between devices, and alter the status of an I/O device or peripheral.

The BDOS manages directories, files, and most disk operations, including listing the I/O functions. An unusual feature of the 80150 that is closely related to the BDOS is the semiconductor "memory disk," a block of RAM whose size is determined by the user and which CP/M-86 treats like a standard floppy disk. The RAM block is one of 16 devices that the BDOS can address.

All system-dependent I/O routines reside in BIOS, and several of them are called by other software. A designer writing CP/M-86 code can modify the standard I/O routines, as well as tailor his own routines to almost any hardware environment. The 80150's BIOS routines offer greater flexibility and maintain complete compatibility with standard CP/M-86.

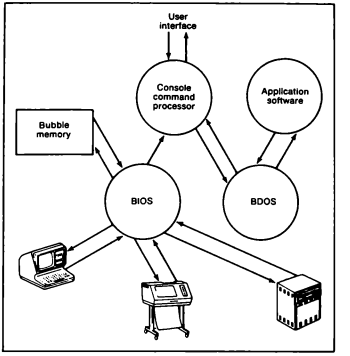
The basic I/O system can be configured in two ways. In the first, the predefined configuration mode, it operates with several standard peripheral components. There is no need to develop or modify the operating system. In the OEM configuration mode, a designer can employ standard and nonstandard peripheral components and device drivers.

Before the 80150 can be customized to specific hardware configurations, the designer must understand the relationships among CP/M-86's major elements and how they interact with him (Fig. 2). If a designer wanted to add performance features to the 80150 by, say, replacing built-in device drivers, he would strategically write intervention points into the operating system code that would later be activated during normal execution of CP/M-86. The user intervention points (UIPs) can be inserted in both the predefined and OEM configuration modes. With them the designer can create new commands and alter certain routines.

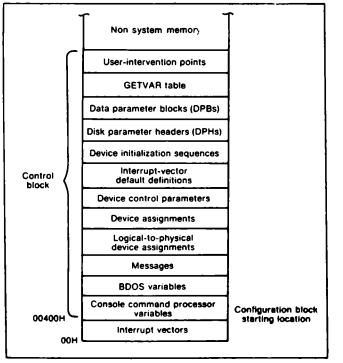
Configuration block is key

The intervention points are stored in a configuration block, which is copied from the 80150 ROM to either a predefined or a user-selected location in RAM (Fig. 3). Regardless of the location, however, the block's contents are initially set up with default data corresponding to the predefined configuration mode.

For the OEM configuration mode, a software interrupt, called GETVAR, has been devised that permits the user to change system variables and pointers within the configuration block. Each system



2. CP/M-86 has a modular architecture which allows designers to write programs that make the bubble memory resemble the disk it replaces. The bubble memory device driver in the BIOS (basic I/O system) is transparent both to the operating system and to the user-written software.



3. The firmware in the iAPX 186/50 chip set is configured as a block, and all table data pertaining to the block is stored either in a predefined location of RAM or in an area that the user selects. The GETVAR table lets the designer change values within the block.

variable has its own index number. By activating the interrupt with the appropriate index number of the desired variable pointer, GETVAR returns the segment and offset address. A boot-up procedure uses that information to read or modify the pointers or variables.

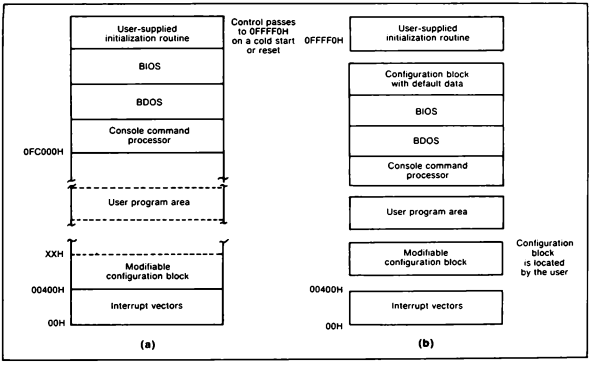
The manner in which the system is initialized depends on the mode of configuration. In the predefined mode the 80150 memory must be located at absolute-segment address 0FC000H (Fig. 4a). Notice that the configuration block is fixed at 00400H, immediately above the interrupt vectors. Upon a cold start or reset, the 80150 copies the configuration block to low RAM and sets the interrupt vectors. Other routines are initialized as the operating system uses them. Each device in the system contains a default routine that is reached by passing through the configuration block to obtain the address vector.

In the OEM mode the 80150 can be positioned on any 16-kbyte boundary save FC000H or 00000H (Fig. 4b). The cold-start bootstrap routine must be located at absolute-segment address 0FFFF0H, but the user determines the placement of the configuration block and programming area. In this mode, the configuration block can be modified before actual CP/M operation begins.

The initialization sequence begins once the 80150 has located the configuration block, which it does by loading the 80186's data register with the desired segment address (Fig. 5). The kernel thus places the block in a specific location and then builds a default interrupt table.

The 80150 returns to the bootstrap routine with the address required to resume CP/M operation. Control returns to the bootstrap routine after execution of a far return, in which the return address is stacked prior to the call. The GETVAR interrupt now locates variables and pointers, so that the system can be modified appropriately. When initialization is complete, control passes to the console command processor.

Like all operating systems, CP/M-86 executes routines that handle disk memory I/O activities.



4. The configuration mode of the 80150 determines the chip's initialization sequence. For the predefined mode, its memory must be located at absolute segment address 0FC000H (a). In the OEM mode, the memory may be located on any 16-kbyte boundary, except FC000H or 00000H (b).

Adding even more flexibility is the bubble memory, a nonvolatile form of storage that eliminates the space, size, maintenance, and reliability headaches frequently associated with disk memories. This particular system can accept as many as eight 1-Mbit bubble memories, each containing a magnetic device and five support circuits. The user can expand or reduce the amount of bubble storage in 128-kbyte increments. Governing all the bubble memories is a controller, the 7220-1 (see Fig. 1, again).

The benefits of bubble memory are numerous. Before taking along a personal computer on an overnight trip, a user can load needed programs from a disk into a computer and then transfer them to a bubble memory, leaving the disk on his desk. A similar scheme can be implemented from remote locations over telephone lines via modems. When the user is back in the office or at the work station, the resident bubble memory can augment a disk drive and may, in fact, offer a twofold increase in performance.

Together firmware and bubble memory offer a distinct advantage. Designers do not have to wait until the operating system is brought up and bootstrapped before initializing the computer, since the operating system already resides in hardware.

The hardware interface between the microprocessor and the 80150 kernel is simple and straightforward, as is the peripheral circuitry for the bubble memory. Completing the basic nucleus of the diskless system is a universal synchronous/asynchronous receiver-transmitter (USART) and local memory. The latter comprises RAM and ROM (or EPROM), some of which is reserved strictly for the iAPX 186/50 operating system processor.

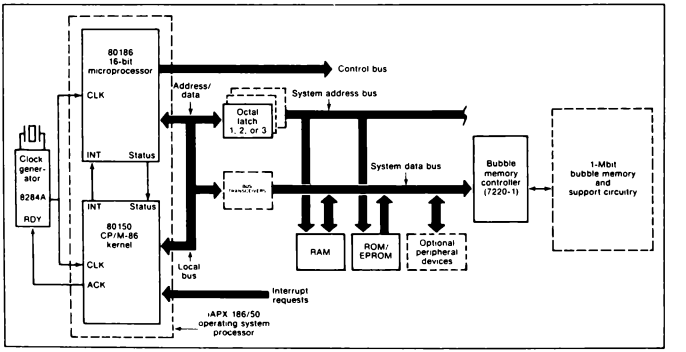
The 80186 contains chip-selection logic; thus little if any logic must be added. Six output lines address memory; seven, peripherals. Because the microprocessor's address and data lines are multiplexed on the same set of pins, the address bus must be demultiplexed with latches. For most standard memories or peripherals, the addresses must remain stable throughout the bus cycle. However, the 80150 firmware requires no constant addresses and thus no latching.

Inside the kernel

The 80150 firmware embodies version 1.1 of CP/M-86 and contains timers, programmable interrupt logic, and control provisions. The kernel con-

Comparing the performance of floppy disks with bubble memory

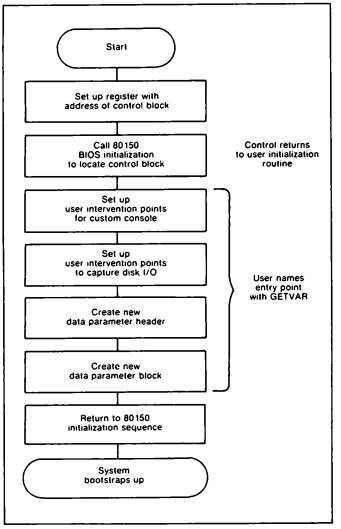
Performance parameter	5¼-in. floppy	8-in. floppy	Bubble memory
Average access time (ms)	250	200	41
Data rate (kbits/s)	250	200	100
Average latency (ms)	100	83	7



1. The two-chip iAPX 186/50 joins with a 1-Mbit bubble memory and sufficient RAM and ROM to form the heart of a diskless personal computer. The chip set comprises an 80186 16-bit microprocessor and an 80150 operating system kernel; together these chips serve as a complete CP/M-86 operating system.

Combined with the management capabilities of the operating system, these routines organize the storage, allocation, and retrieval of data from disk. Since bubble memory easily emulates disk memory, files can freely move from a standard floppy disk to the bubble, so that the disk may be removed.

The system's BIOS contains device drivers for a floppy-disk controller. The drivers implement high-level disk I/O routines like SELDSK (select disk), SETTRK (set track), SETSEC (set sector), and SETTRAN (translate sector). Whenever the system must access a disk, it employs one of these routines in conjunction with three data structures—the disk parameter header (DPH), the disk parameter block (DPB), and the disk request block (DRB)—all of which are located in the configuration block. The first structure contains information about the disk drive and supplies a scratchpad area for certain BDOS operations; the second holds the specifics for each disk drive in the system (for instance, the total capacity, number of sectors per track); the last contains information pertaining to the specific device being accessed.



5. Initialization in the OEM mode requires that the 80150 locate the configuration block where desired, build a default interrupt table, note the configuration block's location, and return the return address for the bootstrap PROM so that 80150 operation can be resumed.

Even the semiconductor "memory disk" mentioned earlier has its own disk parameter header and block, as well as an entry into the disk parameter table designating its assigned drive number. When files are manipulated by the semiconductor disk, memory-to-memory transfers occur in a split second.

Assume that the BIOS routine SELDSK is choosing a floppy disk for access. It looks up the disk parameter header in a table containing CP/M's 16 possible disk devices, at one DPM per device. The DPHs act as pointers to the disk's setup read and write routines, as well as to the disk parameter block associated with each device driver. Using that information, the routines set up the track and sector of the disk, the destination addresses, and so forth. Afterward, the Read or Write function performs the actual I/O operation. The bubble memory driver can emulate this operation by converting the disk's address (track and sector) into a bubble memory address (page). It also issues the appropriate commands to the bubble memory controller and checks for errors.

Disks and bubbles store information differently; thus a comparison of their major performance parameters like average access times and data transfer rates is difficult to make without bringing in other performance data (see the table). However, there are significant differences that can be observed. For instance, whereas a disk must be formatted and algorithmically controlled to position stored sectors consecutively, a bubble memory needs no formatting and can be started and stopped instantaneously at the correct position. For these reasons and others, bubble memories eliminate much of the software overhead associated with disks and thus boost performance.□

January 1984

Bubble Up: Megabits That Don't Forget

By
William F. Arnold

JANUARY 1984
ORDER NUMBER: 230928-001

Bubble up: megabits that don't forget

Bubble memories may yet fulfill their promise. The technology is sound and the market is expanding

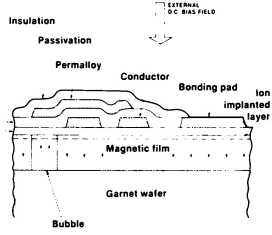
By William F. Arnold

Not long ago, charged-coupled-device (CCD) and magnetic-bubble-memory technologies promised to change the face of computing-system memories dramatically. But advancing memory-chip and disk-drive technologies shoved CCDs into niche applications such as image-sensing and TV-filtering.

And bubbles? Well, after a slow start and some notable defections of potential manufacturers, magnetic-bubble-memory technology just might become a nice business for its several merchant suppliers. The worldwide market is expected to reach $112 million this year and to surpass $500 million by 1987, according to Intel Corp. of Santa Clara, Calif. Intel's projections are based on estimates by San Jose-based Dataquest Inc., an electronics-industry scorekeeper.

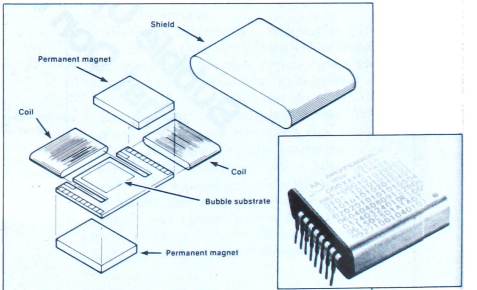
Nonmechanical bubbles are inherently rugged, light, dense and nonvolatile (i.e., they hold their storage when the power goes off). Those properties make them a natural fit in harsh environments that have high temperatures, much dirt, and electrical noise, such as in manufacturing controllers, military avionics or portable instruments. Intel, which claims one-third of today's market, says that about 75% of bubble-system sales are for harsh-environment applications and the rest for commercial uses.

But by 1987 Intel expects that ratio to be reversed to 60/40. According to Michael W. Eisele, Intel's bubble-memory product manager, harsh-environment users are being joined by commercial users. Lundy Electronics Systems Inc. of Glen Head, N.Y., for example, has employed the bubble system for a bank-teller terminal, and



MAGNETIC BUBBLE TECHNOLOGY differs from semiconductor technology in the materials used and in the complexity of the process

Source: Intel Corp., Motorola Corp.



BUBBLE MEMORY UNITS contain the bubble chip, the coils that generate the rotating field, two permanent magnets for the bias field and a magnetic shield

manufacturers of data-collection systems are eyeing bubbles to ensure security of data, Eisele says.

Intel hopes that expanding commercial uses for bubbles will generate new customers. Examples of such uses include a point-of-sales terminal from Nixdorf Corp. and add-on memory cards for International Business Machines Corp.'s Personal Computer (PC) made by Helex Laboratories and MPC Peripherals. And a stunning use was by Grid Systems Corp. in its less-than-10-pound portable executive PC [ELECTRONIC BUSINESS May p98].

Helping bubble technology gain a wider market is Intel's strategy of guaranteeing future price cuts for its BPK 70-4 one-megabit subsystem. In a second round of price guarantees, Intel's prices will be $199 each for 5,000 units now, $149 for 10,000 units early next year, and $99 each for 25,000 by late 1984, according to Eisele. These price guarantees have put Intel's bubble business on a steep and profitable ramp-up, he says.

The preannounced price cuts are very good for the industry, asserts Leonard Call, marketing manager for bubble memories at Motorola Inc.'s Semiconductor Products Sector in Tempe, Ariz. Motorola, the only other U.S. merchant bubble supplier, joins Japan's Fujitsu Ltd. and Hitachi Ltd. and France's Sagem in the bubble marketplace. "Motorola will be a competitor" on the price cuts and is evaluating them, Call declares.

The bubble challenge

At those prices, bubbles can challenge the two competing ways of getting nonvolatile mass storage: the floppy-disk drive and low-power complementary metal-oxide-semiconductor (CMOS) random-access memory (RAM) chips linked to a battery for backup power, Eisele says.

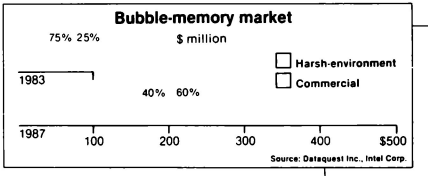
Compared with floppies, bubbles are more reliable, smaller and faster, Eisele maintains. The CMOS-RAM-battery option, on the other hand, would need "a lot of CMOS RAM" to get a two-megabit system that is achieved easily with a bubble, Motorola's Call notes. But CMOS RAMs are faster, he adds.

Before changing to bubbles, Lundy Electronics used the CMOS-RAM-and-battery combination for its teller terminal, a Lundy spokesman says. "With bubble memories you don't have to worry about the batteries," he says. The technology also allows a large internal-storage capacity, he adds.

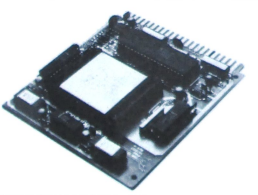
Also distrusting the CMOS-battery combination is Michael B. Olex, senior design engineer with Amhurst, Ohio-based Nordson Corp.'s Robotics Division, a $150 million-a-year maker of industrial coating equipment. "I don't trust battery backup," he says. "You never know if the battery is fully charged." The ruggedness and nonvolatility of bubbles seem suited for the company's $100,000 base-priced MRC-II, a modular robot control for sprayers, he says.

Bubbles also most likely will get a boost from higher densities' availability which will lower further bubbles' cost per bit of memory. Sharing some of the same processing steps as very-large-scale integrated circuits, bubbles benefit from advanced techniques such as scaling and advanced lithography. Intel, for example, has announced a four-megabit bubble memory made with advanced x-ray lithography for fine line patterning of the circuit. Eisele and Call predict a 16-megabit bubble subsystem by sometime between late 1986 and 1988.

To alleviate some potential users' concern that Intel is the only U.S. supplier, the company has signed a



GRID SYSTEM'S portable-personal computer, with a bubble memory, is designed to operate in harsh environments



BUBBLE MEMORY SUBSYSTEMS include the bubble-memory package, two coil formatters, a drive transistor, a current-pulse generator and the bubble-memory controller, which can drive up to eight bubble memories

second-source agreement with Motorola to produce Intel's one-megabit chip and, importantly, most of the support circuitry needed to make it work. Motorola's Call says that he will begin sampling the part next month, with production beginning in the spring.

Single sourcing is a major concern. Nordson's Olex as well as Mary Kay Winter, a product-planning specialist at the control products business unit of John Fluke Manufacturing Co. in Everett, Wash., cited it as a problem. "Intel has pretty much a monopoly in the United States," Olex states. "When I started the design, I had to convince my management to go single source."

Winter, whose company offers bubble memory as an option for an instrument controller, concedes that she was "very reluctant to go single source." But because it is only an option, "the whole instrument won't go under" if Fluke can't get Intel's bubble memories.

Winter's concern was heightened a few years ago when National Semiconductor Corp., Rockwell International Corp., and Texas Instruments Inc. dropped out of the market. That now leaves Motorola as a second source for two bubble designs, Intel's and the National design now used by Sagem. Call says that the two designs are complementary, the former for consumer applications, and the latter for high-performance, high-temperature uses. Intel and Motorola have not agreed yet to second source the former's four-megabit part.

Whether or not these developments will let bubbles really break out of their niche orientation is unclear. Intel chairman Gordon Moore has said that the bubble market has not lived up to the company's initial expectations, but implies that it will be a nice, small business.

Fluke's Winter, however, says that although she would use more where they are called for, she doubts that, even with all the features, bubbles will break out of niche markets. But some companies do very well serving niche markets. Motorola's Call says that bubbles should not be compared with RAMs; they should be compared with other nonvolatile memories. □

APRIL 1984

On/off Scheme Slashes Bubble Memory's Power Drain

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ORDER NUMBER 231072-001

Because of its nonvolatility, magnetic-bubble mass storage can be switched off when not in use. It then consumes the power of a CMOS static RAM system, which a battery can readily supply.

On/off scheme slashes bubble memory's power drain

Every computer worthy of the name needs as much mass storage as it can get, and battery-powered, portable microcomputers are no exception. Where they are exceptional is in the demands they make of their mass storage: low power consumption, to extend battery life; ruggedness, to survive the perils of being portable; and of course the highest possible number of bits per square inch of board space.

Battery-backed CMOS static RAMs storing 16 or 64 kbits apiece have been favored for the job. But magnetic-bubble memory chips holding 1 Mbit each could be serious rivals, if the memory subsystem takes advantage of their nonvolatility.

To date, bubble systems have lost out because when powered continuously, they consume at least three to four times the wattage of RAMs. But mass storage is seldom active more than 10% of the time, and a bubble system's average power consumption falls to the RAM system level if it is switched off when not in use.

Consider a 128-kbyte system built around a 7110 1-Mbit bubble memory and a 7220 bubble memory controller. When actually transferring data, these two devices, along with their support ICs, typically consume about 3.5 W. In the conventional stand-by mode, they dissipate about 1.5 W. When a power switch is employed, this standby figure drops dramatically—to below 25 mW.

Thus, assuming a 10% duty cycle, the conventional bubble system will dissipate an average of 1.7 W, whereas one that switches off when not in use will consume less than 400 mW—a reduction of more than 75%. In comparison, a 128-kbyte CMOS RAM system, which must run continuously, draws about 500 mW.

With power consumption equalized, the bubble system's greater bit density per device now really shines. A 256-kbyte system uses only two 1-Mbit bubble devices, which together with support circuitry occupy just 25 in.^{2} of board space. Such a system is smaller, less complex, and hence more reliable than a RAM-based 256-kbyte memory, which needs 51 in.^{2} of board to hold 32 64-kbit chips plus their support circuitry or 160 in.^{2} to hold 256 16-kbit chips. The respective costs of the three systems are estimated to be about $400, $1100, and $700.

A modified system

A bubble memory system modified for power switching includes bus isolation circuitry and power-switching circuitry, in addition to a 4-MHz clock, the bubble memory, its pulse generator, and its controller (Fig. 1). The bus isolation circuitry prevents the processor and the memory controller from sending destructive noise to each other during power-down and power-up. The power-switching circuit controls switch timing, as well as the 5-V dc and 12-V dc power switches.

The controller must never see inputs greater than $V_{cc}+0.5$ V. Therefore, when the power to the controller is removed—that is, when V_{cc} goes to zero—its various inputs must also be disabled. Its clock signal is suppressed by powering down the clock itself. All the controller's other inputs come through the bus isolation cir-

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cuit, which effectively turns them off.

The actual switches in the power-switching circuitry are FETs (Fig. 2). Their reliability is high enough not to compromise the reliability of the bubble memory. An n-channel transistor switches the 5-V line, and a p-channel FET handles the 12-V.

Operation is straightforward. The Power-On input from the host processor goes to a pair of comparators. One of these sends the signal to the bubble memory controller's Reset input, and the other level-shifts the signal and delivers it to a D flip-flop's Set input.

If the signal is high, the memory controller is unaffected, but the outputs of the D flip-flop, Q and $\overline{Q}$ are set to 12 and 0.0 V dc, respectively. Since the outputs are tied to the gate inputs of the two FETs—Q to the n-channel and $\overline{Q}$ to the p-channel device—the high signal causes the FETs to turn on and deliver power to the bubble system.

Turn it off

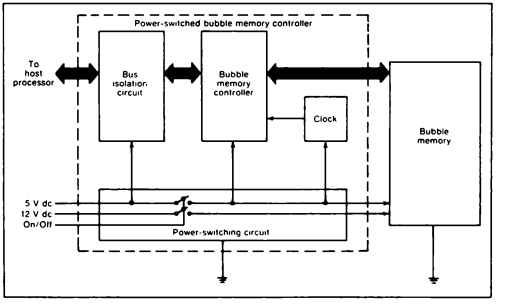
To switch off the system, the Power-On signal is pulled low, to less than 1.5 V. As before, one comparator will send the signal to the controller's Reset input. The logic low will cause the controller to begin the power-down sequence, ensuring that no data is lost.

At this point, it is necessary to remember the power-supply decay rate limitations specified by the bubble manufacturer. For the 7110, the 5-V line must not decay faster than 0.45 V/ms, and the 12-V line not faster than 1.10 V/ms. These limits must be observed for 120 μs after the memory controller's Reset input goes low.

Meeting the decay-rate limitation

In the present circuit, compliance with the decay rate limitation is ensured by maintaining the supplies for 150 μs after Power-On goes low. The delay is created by connecting the comparator output that goes to the flip-flop's Set input to a one-shot's trigger input as well. When Power-On goes low, the negative falling edge triggers the one-shot and a 150-μs delay commences, after which the flip-flop is clocked, its outputs are reset, Q goes to 0.0 V dc and $\overline{Q}$ to 12 V dc, and the FETs are turned off.

The microprocessor is isolated from the bubble memory controller by two bus transceivers, a comparator, and an optional AND gate (Fig. 3). The comparator compares the 7230 current-pulse generator's power-failure output (Power-fail) (which is connected to the controller's Reset line) with 2.5 V dc. If it is greater, the supplies are operational and the control-signal bus's transceiver is enabled. The data bus's



1. The power to this bubble memory controller is switched on only when the memory is needed. Bus isolation circuitry prevents the controller and the host processor from sending destructive noise to each other during the switching.

transceiver is enabled when Chip Select ($\overline{CS}$) goes low to signal that a data transfer is beginning. In this case, Data Acknowledge ($\overline{DACK}$) is simply returned to 5 V through a 5.1-kΩ resistor. The AND gate, which allows either $\overline{CS}$ or $\overline{DACK}$ to enable the data bus, is needed only if direct memory access is being implemented.

Note that the output of the comparator that is used to enable the control-signal bus transceiver also serves as a Power-On Interrupt signal, which can be used to interrupt the processor when the bubble memory supplies become operational. The optional circuitry supplies the active-high complementary signal.

Power-on interruption

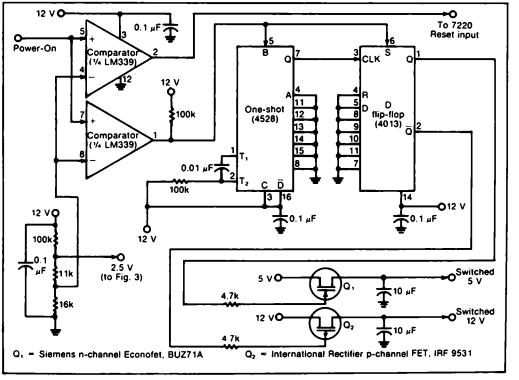
The power switch can operate with systems using either direct memory access or polled data transfers. Regardless of which type is selected, the bubble memory controller must be initialized every time power is applied. Initialization puts the controller into a known state by loading the boot-loop code from the bubble memory into the boot-loop registers and synchronizing the controller with the memory's first 64-byte page.

When the entire machine is powering up from a cold start, the host machine starts the initialization by sending the controller the Initialize command.

This form of initialization takes 170 ms in the worst case. Therefore, to save time later on, when the machine has been running and the bubble memory has been powered down in an orderly fashion, the host emulates the bubble memory to the controller in order to initialize the latter. The emulation takes only about 5 ms.

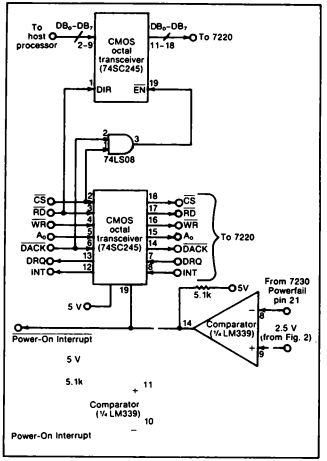
To emulate initialization, an external copy of the boot loop code must exist. Consequently, this code is read into the host's RAM at the time of the cold start. When it is time to power down the bubble system, always execute a Read Seek command to page $9B_{16}$ or a Write Seek to page 395_{16} before removing power. This will synchronize the bubble memory to the same page that an Initialize command would. (Since the bubble memory is nonvolatile, the synchronization is not lost when power is removed.)

To access the memory again, the initialization process begun by sending the Seek command must be completed. When the supplies are operational and the controller has been reset by the Abort command, execute the bubble memory purge command and write to the controller's parametric registers. Then reset the FIFO. Finally, transfer the boot loop code from RAM (or EPROM) to the controller's FIFO and from there to the boot-loop registers. (Use the



2. To give the controller time to power down the bubble memory in an orderly fashion, the one-shot waits 150 μs before it clocks the D flip-flop, which then turns off the switches.

On/off bubble scheme



3. When the comparator finds that the bubble memory supplies have been switched on, its active-low output enables the control-signal bus's transceiver and interrupts the processor. Then $\overline{CS}$'s going low enables the data bus's transceiver. The optional circuitry shown in color sends an active-high interrupt signal to the processor.

Write Bootloop Registers Masked command.) The memory is now ready for data transfers.

Power-downs are unchanged. All that is required is that a Seek command be executed before power is removed.

When the memory is being accessed, the amount of power it consumes can be kept to a minimum if the accessing is done efficiently. Keep in mind that if information is required sequentially, it should be stored in sequence and that a few large transfers are more efficient than many small ones. Instead of repeatedly accessing the memory for the same information, frequently used data should be transferred into system RAM.□

APRIL 1984

Bubble Memories: Their Military Role

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ORDER NUMBER: 231072-001

BUBBLE MEMORIES: Their Military Role

by RICHARD PIERCE

MAGNETIC BUBBLE MEMORIES are rapidly moving into a wide range of military and aerospace systems because of their increased availability in high-reliability, militarized versions. They promise to take over in systems that previously incorporated such traditional mass storage devices as core memories, tape recorder units, drum memories and disc memories. Designers are interested in reducing physical size and increasing system reliability (MTBF), thus reducing lifetime service and maintenance costs without compromising performance. In short, a designer wants to replace that "big box" with a more reliable smaller box.

The limitations of traditional storage devices are many, including the requirement of controlled environment for reliable operation, regular maintenance and their physical size. In contrast, bubble memories can, and do, operate under extreme conditions.

To understand why bubble memory holds so much potential for military system designs, let's look at some common requirements of mass memory for military equipment.

Selection criteria. First, let's establish the common requirements of mass memory for military equipment for comparison purposes.

RELIABILITY. This requirement varies. For example, NASA fail operation/fail safe (FO/FS) guidelines for the space shuttle mandated the safe return of the vehicle and crew after two like failures in the system. Other applications are specified by Mean Time Between Failures (MTBF).

SERVICE AND MAINTENANCE. The cost of periodic service and maintenance continues to climb, thus increasing product life-cycle costs, as military applications currently using disk and tape technologies are painfully aware. Design trends are to reduce product life-cycle costs, incorporate built-in testing, and reduce large systems to many smaller plug-replaceable units.

TEMPERATURE EXTREMES. Most equipment must be able to operate over an extended temperature range, on the low end from −20°C to −55°C, and in the upper ranges from +71°C to +85°C. Non-volatile storage temperature requirements are typically −62°C to +100°C.

ALTITUDE. Operation to 10,000 feet and transport to 50,000 feet.

VIBRATION AND SHOCKS. Reliable operation up to 10G vibration and 15G mechanical shock.

PERFORMANCE. While speed of data transfer and access time are important selection criteria, evaluations must be made carefully and within very narrowly defined limits. In general, actual throughput is dependent on the specific application and involves consideration of

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the exact hardware implementation (memory size, data transfer lengths, etc.)

Bubble memory. Bubble memories have no moving parts or maintenance requirements and can perform over a wide operational range. For memory requirements of 10^6 to 10^8 bits, bubbles are quickly becoming the preferred mass storage in military and aerospace applications. Complete extended temperature (−20°C to +85°C) 1 mbit bubble subsystems have been delivered since 1982 (including controller and support ICs) for applications such as test, field command, communication terminals, and flight navigation systems.

A −55°C to +85°C bubble subsystem is realizable in the not-so-distant future. Such developments will help bubble memories continue to garner an increasing share of design wins where more traditional devices might have been used.

Magnetic bubble technology has come a long way since magnetic bubbles were first observed at Bell Labs in the late 1960s. Advances in VLSI technology, along with improvements in bubble device architectures, have expedited the evolution of magnetic bubble technology. Today a solid, healthy technology exists—one that continues to influence product development trends and where volume commercial applications provide the technology learning that allows for improved performance specifications for military systems.

Design advantages. Bubble memories offer several design advantages. First the highly integrated bubble support chip set (including controller) yields a compact design which can be adapted to custom requirements. Designing with the complete Intel memory subsystem reduces to interfacing a bubble memory controller (BMC) chip and following layout guidelines for a bubble cell. The BMC allows the bubble memory device (and support ICs) to be treated as a subsystem, much like a floppy disk controller (FDC), eliminating the need to be concerned about disk drive mechanics (head positioning, bad sector information, etc.).

Flexibility is another key design advantage. One 7220-1 BMC can accept as many as eight one-megabit bubble memory cells, each containing a magnetic device and five support circuits. The user can expand or reduce the amount of bubble storage in 128-Kbyte increments. Additional flexibility is provided for transferring data. Three modes are supported—polled, interrupt-driven, or DMA.

Software options include three levels of automatic error correction and various data transfer rates (for multiple bubble systems). Governing all these possibilities is the completely programmable BMC. Again, compared to a floppy disk subsystem, the BMC provides equivalent if not better flexibility at about one-fourth the software overhead. Such design flexibility is attractive for custom requirements (especially space) and future expansion capability.

An example of such design flexibility is a fully-militarized communication terminal developed for the US Army. The Single Subscriber Terminal (SST), designed and manufactured by the Librascope Division of the Singer Company, is a member of the Modular Record Traffic Terminal (MRTT) equipment family.

It consists of a plasma display panel, standard keyboard, a communications interface and a fully-maintained cassette containing 256 Kbytes of bubble memory for communications storage.

Bulk storage requirements. The goal for the bulk storage requirements was to find the densest and most reliable memory available and to configure it so it was (1) removable

and (2) conformed to a particular file management system. Flexibility allowed the bubble cassette to be designed so that it contained the bubble devices and only one support component (the Formatter/Sense Amplifier). The remaining support electronics, including a dedicated microprocessor, remain inside the terminal.

The SST system software can view bubble memory as a solid-state disk. Data organization is such that the data transfer is a page (or *sector* in disk technology) which is typically 64 bytes. This data formatting is not "soft" as in the case of disk technology but instead is a result of the device architecture. Conforming to different file management systems and format styles is simply a software exercise. For this application, the sector size is 1024 bytes (that is, sixteen 64-byte bubble pages).

As mentioned before, future expansion is important. A major problem facing military designers is the length of a design cycle. Providing for an upgrade path over a design's life is a key consideration in military designs. Properly implemented designs can accommodate next generation devices as they become available.

Alternative technologies. Mechanical magnetic memories all suffer from a common disadvantage: limited reliability. Their precision electromechanical construction cannot withstand harsh environmental conditions (dust, dirt, shock, vibration, humidity) without special adaptation. Usually this entails adding heaters, fans, or special shock and vibration mountings to make tougher a disk or tape.

These techniques do not address the fundamental need for regular service or the soft error rate of disks. A complete one-megabit bubble memory subsystem has a MTBF of over 320,000 hours at 100 percent duty cycle at 55°C. This translates to better than 40 hours. This compares to the 5,000 to 10,000 hours quoted for disk drives at room temperature and 20 percent duty cycle. Reliability is key in military applications and reliability translates into significant reductions in product life-cycle cost.

Magnetic media. Core memory has long been a standard of military system designers. Virtually every military general-purpose computer uses some core memory. However, let's compare. Bubble memory volume is about one-fourth that of core at substantially reduced power consumption. Another consideration is weight—bubble memories weigh less than 90 grams per 128 kbytes of storage. All of these factors are just about enough to convince a system designer to draft bubbles for their application.

One hurdle to overcome, however, is speed. Core memory typically has an access time of 400 ns and cycle times of 900 ns. The solution is simple, yet application-dependent. A system design would need, say, a megabit of fast RAM integral to system. When a system is powered-up, the bubble is downloaded into RAM in 1–3 seconds. Should any power interruptions occur, the bubble automatically downloads into the RAM again. Finally, bubble costs anywhere from one-fourth to one-tenth as much as a megabit of core.

Semiconductor memories will always maintain a performance advantage over bubbles. Bubble memory's 48-msec average access time is two to five times better than a disk drive, yet not designed for real-time operations. However, let's consider some other factors.

Volatility is the fundamental problem of CMOS RAM chips. In small systems, non-volatility might be achieved with battery back-up, but the current drain becomes excessive for high bit densities, not to mention the additional board area due to chip count. Batteries also introduce undesirable periodic maintenance. As for power consumption, bubble memories can compete favorably with CMOS RAM devices.

Bubble device characteristics encourage switching power off during stand-by mode. Depending on the system duty cycle, significant power savings are possible.

ROMs and EPROMs are frequently limited because they lack reprogrammability (without system disassembly). EEPROMs lack the required density in many applications and have a limit on the number of times they can be "written over." Most systems will need both bubble and semiconductor memory technologies. For example, dynamic RAM and EEPROM plus memory is a higher performance, lower cost memory solution than core.

Reliability and storage. It is precisely these considerations that are convincing military systems designers that bubble memories are the logical choice. When compared to disk or tape technology, bubble reliability and storage density easily outweigh the cost of service and maintenance and the cost of lost data. Only in applications where enormous storage capacity (greater than 10 megabytes) is needed will large disk and tape units prove cost-effective. With present cost and performance characteristics, magnetic bubbles offer unsurpassed alternatives to other storage techniques in the capacity range of 128 kbytes up to 10 megabytes of data storage.

At RCA Automated Systems, engineers have developed a sophisticated test set around a multiprocessor-based architecture. This system is designed to keep today's Army vehicles, with their complex electronics and propulsion systems, at full combat readiness at all times. The Simplified Test Equipment (STE-X) consists of an Intel 8088 as the main processor with 640 kbytes of directly accessible bubble memory and three eight-bit peripheral processors.

In addition there are provisions for a 128 kbyte bubble memory cassette. All share a common bus. The 8088 handles the bulk of the test selection, performing measurements and making diagnostic decisions, while the peripheral processors handle the various functions: (1) dynamic RAM refresh operation (2) slave activities downloaded from the 8088 (e.g., a "small" FFT) and (3) acting as a multifunction frequency counter. All of this functionality fits in a unit measuring 12" × 12" × 13" and weighs less than 40 lbs.

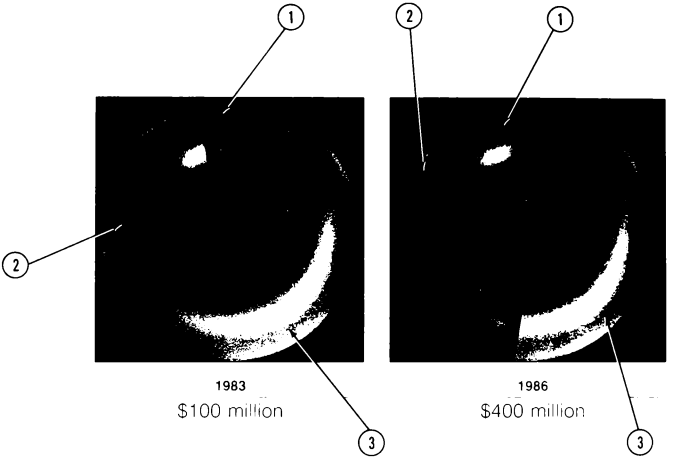
According to Steve Courcy, program manager of STE-X at RCA, the 8088-based portable STE sets are often used in the harsh "edge-of-battle" environment. This places substantial demands on the unit, particularly any mass program storage device. All the mass storage devices considered, such as Winchester disks, floppy disks, cassette tapes, or strip cards, were deemed too fragile to withstand the hostile environment. Bubble memory's solid-state, truly non-volatile storage is a clear advantage.

Advantages. Environmentally, bubble memories excel when compared to other magnetic media and presently match semiconductor devices except for temperature range. Bubble memory subsystem operating temperature range of −55 to +85°C will be achieved within the next year.

The need to eliminate space, size, maintenance and reliability headaches frequently encountered in military systems continues to accelerate. Bubble memory can help. Bubble subsystems, available today in high volume, operate over wide temperatures and have a very high tolerance for shock and vibration, humidity and high altitude extremes.

Customer response to the hi-rel extended temperature 1 mbit bubble subsystem indicates that this market will outpace many other technologies in the high growth electronics industry. The market will more than double each year, growing from $5 million in 1983 to $100 million in 1986. This increase will bring the 1986 military bubble market to 25 percent of the total bubble market (see figure 1). •

FIGURE 1: Total projected Bubble Memory Sales



○ Military (1)

○ Commercial (2)

○ Industrial (3)

APRIL 1984

Bubble Memories Are Back

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ORDER NUMBER: 231108-001

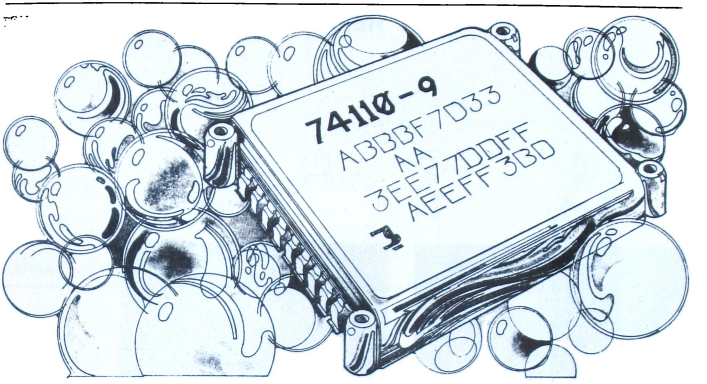

Illustration: Mike Eagle

Bubble memories are back

Random-access bubble memories are five times faster than floppy disks—and more efficient for working mass storage.

Systems integrators who haven't checked magnetic bubble technology recently may have overlooked the fact that bubble technology is now a cost-efficient way to implement working mass storage in such microsystems as desktop or personal computers, terminals, and instrument controllers.

Early bubble technology developers touted these memories as a dynamic RAM replacement. But, because of their high density and solid-state reliability, random access bubble memories have gained acceptance as working mass-storage devices that replace floppy disks. When used to replace one of the disks in a typical two-disk microsystem, a bubble memory can function as a second mass storage device that provides about five times faster access to random storage (Fig. 1).

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The bubble memory subsystem is ideal for transferring files, compiling programs, and even executing programs, especially where applications use large look-up tables, or operating systems optimize storage space by using randomly distributed files.

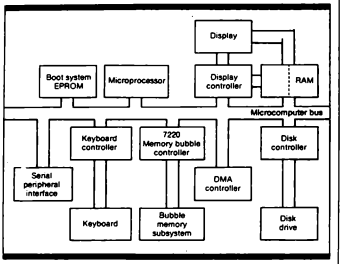
Bubble memories can greatly improve the performance of a two-drive system. One-Mbit bubble provides storage capacity similar to a single-sided, single-density 5¼-in. floppy. And the new 4-Mbit bubble chips each provide the same capacity as a double-sided, double-density 5¼-in. floppy, as well as provide far higher speed for random access. They can often fit on the same board as the microprocessor, and they are more reliable than floppy disks. Typical error rates are 1000 times lower in a bubble memory, or 10^{-16} compared with 10^{-13} for a 5¼-in. disk.

Whereas bubble memories at one time required system designers to build expensive circuits to support read and write functions, bubble units today

are equipped with all the required support—including a controller that generates timing signals, as well as circuits that provide the required formatting, sensing, drives, and automatic error correction (see "Reading and writing with bubbles").

What this means is that system designers need only supply software commands to the controller to communicate with the bubble subsystem.

The iPDS Personal Development System, for instance, is a computer-system development tool



1. Working off the system bus, a bubble memory can act as a second disk drive that is much faster than a floppy—and is, therefore, ideal for working mass storage in transferring files, compiling programs, and even executing applications that involve large look-up tables and randomly distributed files.

that uses an optional bubble/floppy memory to greatly increase throughput. Software development is speeded by the 40-ms average access time of the bubble memory compared with 250 ms for the floppy. A Basic program interpreter or 8085 macro-assembler executes up to twice as fast with the bubble unit in place. Operating system utilities stored in the bubble unit, instead of on the floppy, also speed the development and debugging of programs.

Since bubble memories are accessed by software commands to the controller, both software and hardware must be considered in implementing a specific design. The design alternatives can be illustrated using the Intel 7220 memory controller (Fig. 2) and the 7110 1-Mbit bubble memory. The design is centered on using the bubble memory to emulate a floppy disk, and then operating the bubble unit as a second disk drive in the disk operating system.

However the design is implemented, the host operating system issues all commands to the bubble memory. It does so by sending the commands to a set of subroutines called the bubble driver. The driver controls and monitors the execution of commands, and returns operational status data when commands are completed. It also supports the controller's command and status registers, as well as the parameter registers that define different operating modes. The parameters are supplied by the operating system when it issues commands.

There are three possible levels of interaction between the host system and the bubble driver. For small, simple applications, the main program can call the bubble driver directly.

At the next higher level, the bubble system can be viewed as a logical device. Here, the driver is designed as a mapping of the logical bubble interface into the physical bubble interface. The mapping isolates applications programs from the specific commands and sequencing of the bubble controller.

Finally, at the highest level—the operating system—the mechanics of bubble access are ignored; the operating system merely opens, closes, reads, or writes the desired bubble files.

The bubble memory is integrated into an existing operating system through a structured BIOS. The BIOS is expanded to interface with the bubble controller and subsystem—by adding calls to communicate with the bubble—while the existing BIOS continues to run the peripherals already in the system.

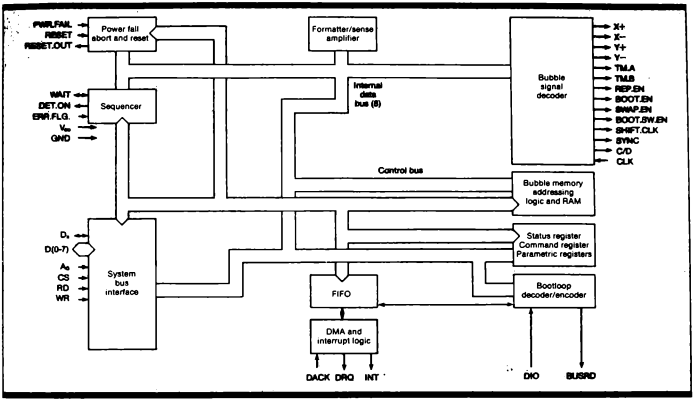
A new jump table is installed in the BIOS that points to the new primitives needed for the bubble memory (Fig. 3). The primitives include initialize, abort, read page, write page, etc. The new operating system must, therefore, keep track of whether the original disk or the bubble subsystem has been selected.

Bubble operating-system primitives are developed from different combinations of commands to the bubble controller. The 7220 command set has 16 commands, where each command is selected by a 4-bit command code. The commands are written to the controller's command port. In addition to such commonly used commands as read, write, abort, and initialize, there are diagnostic commands including "read bootloop register," "write bootloop register," and "write bootloop."

Data are transferred logically between the host and the bubble in pages of 64 kbytes. Error correction is done automatically.

Data in the bubble are organized in a format analogous to the storage of data in a disk sector. Bubble-page sizes are established by system control, just as sector sizes are fixed when formatting a disk. Pages in multiple bubble systems can range from 64 to 512 kbytes. The page size depends on the data rate supported by the system.

Since bubble memories have no active elements, they rarely exhibit hard, or non-recoverable errors. Soft errors do occur that are classified as either data or read errors. Data errors may be recovered by rewriting the data. Read errors—the most common



2. The bubble memory controller provides the interface between the bubble driver—a set of subroutines in the operating system—and the host processor. Commands entering from the system bus are converted to controller commands for reading and writing in the memory, as well as performing diagnostics.

type—can be recovered simply by repeating the read operation.

Each 64-kbyte page has two 14-bit codes that can detect and correct all errors up to five bits in length. Error correction is handled automatically by the bubble memory controller.

Controller is key to subsystem. The key hardware element in the bubble-memory interface is the 7220 controller. In providing a complete interface to a microprocessor bus at the TTL-level, it frees system designers from the need to generate the intricate timing signals and waveforms required to support the bubble memory subsystem.

To transfer data to or from the subsystem, the host must first load the parameters into the controller, and then issue a read or write command.

An 8-bit bidirectional port in the 7220 interface provides access to internal registers. An address line is used to select either the command status registers or the parameter registers.

A command register issues instructions, such as read or write data. A status register provides information of commands and the readiness of the controller to transfer data. The parameter registers have flags and parameters that determine how the controller will respond to software commands.

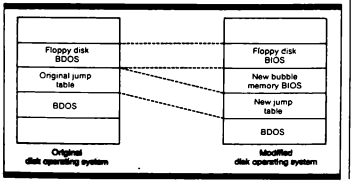
The data register itself is actually a 40-bit FIFO that buffers the timing differences between the 7110 bubble memory and the host processor.

The controller provides users with three different transfer modes: DMA, interrupt driven, or polled I/O.

In the DMA's mode, the controller operates together with a DMA controller, using the data-request and data-acknowledge lines for handshaking. Once data transfer begins, program intervention is not required until the entire data transfer has been completed.

In the interrupt mode, the 7220 along with an interrupt controller uses the data-request line to initiate a data transfer. The request line becomes active when the 7220 is ready to send or receive a burst of data. A typical data burst is 22 contiguous bytes for an interrupt-driven interface. A set of software drivers is also needed to service the interrupts and coordinate the transfer of data

3. The bubble memory subsystem is integrated into the disk operating system via the BIOS. The BIOS is extended to communicate with the bubble subsystem through a new set of system calls, while a new jump table is added to point to additional primitives.



between the 7220 and the memory associated with a host processor.

One advantage of the interrupt mode is multitasking. Since the host processor is only servicing the 7220 during data transfers, idle time between data transfers can be utilized for other processor tasks.

A polled-mode interface reads the 7220 status register to determine when to transfer one byte of data. Of all the interface modes, polled I/O is the simplest configuration to implement. No special hardware or external controllers are necessary to interface the controller with a microprocessor. The major portion of a polled-mode design is the software. A set of software drivers are required to read and write data to the controller. □

Reading and writing with bubbles

A magnetic bubble-memory stores data in the form of cylindrically-shaped magnetic domains in a thin film of magnetic material. (The axis of the cylinder is perpendicular to surface of the material.) The presence of a domain (a bubble) is interpreted as a binary 1, and absence of a domain is a zero. Bubbles are created from electrical signals by a bubble generator within the memory, and reconverted to electrical signals by an internal detector. Externally, the memory is TTL-compatible.

An external rotating magnetic field propels bubbles through the film. Metallic patterns, called chevrons, deposited on the film steer the domains in the desired directions. In these respects, magnetic-bubble memories are serial high-density storage devices like electromechanical disk memories. In disks, however, the stored bits are stationary on a moving medium, whereas in the magnetic bubble memory the medium is stationary and the bits move.

In the absence of power, the stored bits ("bubbles") are held intact by the presence of permanent magnets, contained within the memory's shielded package. Hence, the non-volatility of data is assured.

Bubble densities have typically outpaced semiconductor memory. A 256-kbit bubble device appeared in the mid-1970's. 1979 saw the introduction of 1-Mbit chips; 4-Mbit chips became available in 1983.

A 1-Mbit (128-kbyte) bubble chip provides about the same storage capacity as a single-sided, single-density 5¼-in. floppy disk. The new 4-Mbit chips (512 kbytes) each provide about the same capacity as a double-sided, double-density 5¼-in. floppy disk.

With sub-100 ms read or write average access times, and high density, bubble memory has long held promise as a solid-state mass storage memory for microprocessor-based systems.

The acceptance of bubble memory and the production experience of bubble suppliers has allowed the cost/bit of bubble memory to decrease by an order of magnitude over the last four years. Like other solid-state semiconductor memories, bubble memory follows "learning curve" trends for both cost and increased density.

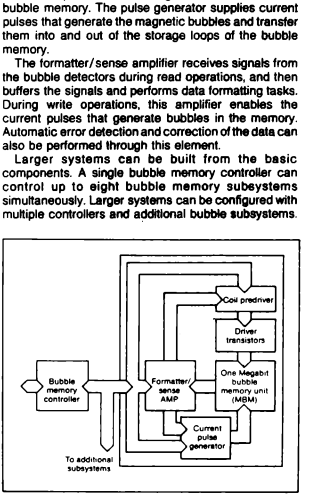
The system interface of bubble memories has been simplified by the availability of VLSI support circuits that take care of "bubble housekeeping". Interfacing bubble memory to a microprocessor-based system requires data conversion from the parallel bus to serial data for writing to or reading from the bubble. In addition, the TTL-level signals of the system must be converted to correspond to either reading (detecting) bubbles or writing (creating) them.

The support circuitry used with a 7110 (128-kbyte) magnetic-bubble memory consists of the following integrated circuit components: a 7250 coil predriver; two 7254 VMOS-drive transistor packs; a 7230 current pulse generator; and a 7242 formatter/sense Amplifier. The 7220 bubble memory controller (BMC) completes the basic system (see figure).

The predriver and the driver packs supply the current needed to create the in-plane rotating magnetic field (X and Y coils) that move the magnetic bubbles within the bubble memory. The pulse generator supplies current pulses that generate the magnetic bubbles and transfer them into and out of the storage loops of the bubble memory.

The formatter/sense amplifier receives signals from the bubble detectors during read operations, and then buffers the signals and performs data formatting tasks. During write operations, this amplifier enables the current pulses that generate bubbles in the memory. Automatic error detection and correction of the data can also be performed through this element.

Larger systems can be built from the basic components. A single bubble memory controller can control up to eight bubble memory subsystems simultaneously. Larger systems can be configured with multiple controllers and additional bubble subsystems.



June 1984

Bubble Memory in Communication Products

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June 1984
ORDER NUMBER: 231110-001

Bubble Memory in Communication Products

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In the world of telecommunications, reliability is a key feature that adds value to a product. The cost of PABX downtime is high in terms of lost sales calls and other revenue-generating activities. PABX buyers scrutinize equipment service and maintenance factors before they make a buying decision. In addition, a portable test terminal had better work when the service personnel are out at a field call.

Bubble memory is used to improve communication products by providing greater reliability. For instance, the 1-Mbit Intel bubble memory system has a projected mean time between failures of 40 years measured at 55°C and a 100 percent duty cycle. It works almost anywhere because of its immunity against mechanical shocks, temperature extremes, and dust. Also, bubble memory's performance, temperature options, and low power help to meet strict product standards (**Table 1**).

This article discusses a variety of communication products where bubble memory can add value. Specifically, it discusses the product improvements gained by using bubble memories in PABX applications, portable communication terminals and test equipment, configuration terminals, and speech products.

THE USE OF BUBBLE MEMORY IN PABX'S

The versatility of bubble memory and its combined read and write capabilities allow it to be used for several memory functions in a PABX. It works well as the backup storage medium for a PABX and for some software-controlled features.

Stored-program control appeared in the telecom switching arena about a decade ago. Earlier, all the control and execution of the switching was implemented in wired hardware and was difficult, if not almost impossible, to change. Thus, any modification to the PABX was a cumbersome task.

The stored-program approach changed this when the control routines were stored in software rather than in wired hardware. With the appearance of second- and third-generation PABX's, a myriad of software-controlled operating features were added.

The programs are executed out of fast-system random-access memory (RAM). However, routines have to be stored and backed up in a nonvolatile medium to prevent the loss of critical programs and data because of a power loss. There are several methods available to prevent losses. One direct approach is to use a battery backup to ensure that the volatile RAM would still get power in the case of power failure and, thus, would not lose data. However, the reliability of the system depends on the reliability of the battery.

Another method is to use EPROM/PROM, which is a truly nonvolatile storage medium, for program storage. EPROM/PROM typically is complemented by E^2PROM to store the latest input of data for data-base features. The disadvantage of this medium is that the updating of programs is difficult. Changes with such an approach typically are implemented by replacing the EPROM/PROM chip — a time-consuming activity.

Magnetic tape also is used as a backup medium to RAM. The tape has many inherent disadvantages. First of all, the tape has a limited life span due to wear on mechanical parts and the device's susceptibility to dirt and temperature variations. Also, with the slowness of magnetic tape, it takes a relatively long time to start up a PABX again. Consequently, although tape has been used in older designs, it typically is phased out of today's PABX designs.

BUBBLE MEMORY CHARACTERISTICS

Solid-State: Bubble memory is a solid-state technology similar to semiconductors.

Nonvolatile, Read-Write: Bubble memory is nonvolatile, i.e., if power fails the stored data is retained. ROM, EPROM, and E^2PROM also share this feature, but magnetic bubble memories can have data written into them easily at any time at speeds comparable to those at which data are read.

Density: Available in 1-Mbit modules that can be expanded into larger systems.

Performance: The average random access time for read/write operation is 40 ms.

Temperature: Options of 10° to 55°C, 0° to 75°C and -20° to 85°C are available to maximize performance in different applications.

Power: Low power consumption of 3.9 W, typically active, and 1.55 W, typically standby. By using power-cycling techniques, i.e., switching on power to the system only when it is accessed, the average power can be reduced drastically.

Winchester disks for larger PABX systems and floppy-disk drives for low-end PABX's are other alternatives. However, these alternatives have the same inherent limitations as magnetic tape when it comes to reliability. Reliability estimates of disk drives typically are in the range of thousands of hours measured at low duty cycles and room temperature.

Bubble memory works well as the backup storage medium for medium-sized and lower-end PABX's. With the 1-Mbit bubble memory available in commodity volumes, up to 3-4 Mbytes of bubble memory are typically the largest memory requirements where bubble memory has a good fit. A rough guideline is that bubble memory should be evaluated in systems with less than 1000 lines. In a low-end PABX or key telephone system with only tens of lines, the bubble memory is often the superior medium by virtue of its combined solid-state reliability and read and write capabilities. The latter facilitates the design of systems by users.

For some software-controlled PABX features, a nonvolatile write memory is required — for example, for station message detail recording (SMDR), which provides a detailed usage analysis of individual extensions. These data must be stored in a reliable, nonvolatile storage medium, since the data cannot be recovered if lost. Bubble memory, therefore, has found its way into many "call accounting systems."

Bubble memory also affords other advantages. It is immune to most environmental hazards. Also, its power consumption is relatively low. By using power-cycling techniques and switching off the power to the bubble system when it is not in use, the power consumption can be minimized further. In combination with a wide temperature range, bubble memory options eliminate the need for an air-conditioned and controlled environment for telecommunication systems.

OTHER USES OF BUBBLE MEMORY

Portable Communication Terminals

Bubble memory can provide several functions when used in portable communication terminals. First, it collects data reliably because it is the only solid-state, nonvolatile memory with unlimited write cycles. E²PROM may be used for data collection purposes, but its unlimited write cycles are often a concern in data collection. CMOS RAM depends on the critical battery backup for retention of data. Although CMOS RAM is used in applications with low density requirements, bubble memory is preferred in any higher density requirement.

The bubble also provides storage of different program packages, such as the application-editing program in editorial terminals. It can store changing user programs as well.

In all of these memory functions, the bubble memory provides a reliable, nonvolatile communication buffer. Thus, it stores the data collected before they are transmitted over a communications link and stores the new program received over a telephone line.

Solid-state reliability is critical in portables since they typically are exposed to a variety of small environmental hazards ranging from temperature shocks to mechanical shocks. A disk drive has lower reliability and its long initialization prevents effective power switching, therefore eliminating the battery operation needed for a system to be truly portable.

The bubble memory's small space requirements facilitate the design of compact, lightweight, portable products. From a power consumption perspective, the easy use of power-cycling techniques increases the operating time on a limited battery power budget.

Portable Service and Test Equipment

In portable service and test equipment, bubble memory essentially has the same advantages it has in a portable communication terminal. It stores test and diagnostic programs and different test parameters, such as protocols. It also collects data for further analysis. It facilitates the design of "ease-of-use" equipment by storing all data and programs internally. There is no need to use PROM modules to load different programs or to use a floppy disk.

Configuration Terminals

Configuration equipment act as controllers and facilitate the communication between different equipment. In such products, bubble memory can provide three different memory functions.

First, it stores such permanent configuration data as a device's address, data rate, protocols, and terminal type. The commonly used approach with battery backup RAM can fail when a battery breaks down. This is of concern since the data might be cumbersome to recover, thereby increasing the downtime of the system and reducing productivity.

Second, bubble memory stores program packages to convert data of different types from one terminal to another terminal. Compared to PROM, bubble memory provides easier updating and revision of program packages.

Third, in networks with data rates below the 100-kbps range, bubble memory performs the actual buffering of incoming and outgoing data. Its nonvolatility assures data integrity.

Speech Products

Speech recognition and synthesis are two areas which have been discussed for decades in the science community. Low-end products, such as speech chips in cars, already have a relatively strong position in the marketplace. More advanced, high-end systems are being introduced, not only with speech synthesis but also with speech recognition capabilities.

In speech recognition applications, there is a need to store the words to be recognized. Each person pronounces a word a little bit differently, and today's systems typically are required to store speaker-dependent data. Bubble memory's reliability assures the integrity of the critical speaker-dependent data, and its read and write capability allows the intensive "learning" of speech needed in speech recognition systems. Many applications typically require 100- to 200-word storage — for example, a speech system at an assembly line that recognizes operator input. The 1-Mbit bubble memory density meets this requirement.

CONCLUSION

In telecommunications equipment reliability is a key feature. Customers are willing to pay the extra dollars to get a reliable product and to reduce the negative costs associated with a lack of reliability — service and maintenance, lost data, and downtime.

Bubble memory fits well in several communication applications. No system is stronger than its weakest link and the use of bubble memory ensures that a product's mass memory storage is not the weak link from a reliability perspective. □