BRUTECH ELECTRONICS
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B.E.M-SBC2X/SBC3X

LOW COST SERIES OF SINGLE BOARD COMPUTERS
(B.E.M-SBC2X based on 6502, B.E.M-SBC3X based on 6809)

GENERAL DESCRIPTION

The B.E.M-SBC2X/3X series of advanced single board computers, designed around the 6502 respectively 6809 microprocessor, are intended to replace the B.E.M-SBC2/3 series directly. Connector pin functions, pin locations and mounting holes are fully compatible. The new boards not only offer much more onboard memory capacity with JEDEC JC-42 pin compatible memory devices (three 28-pin sockets are available) and the same I/O capability (one 2651/2661 USART for serial and three 6522 VIA's for parallel I/O applications), but also provide a real time calendar clock, watch dog timer and battery backup for RAM and clock.

Two memory sockets can individually be set for battery backup (CMOS RAM's only) or not (NMOS RAM's or EPROM's). The applied Lithium battery with a capacity of .85 Ah is generally installed for life (more than 10 years of backup capability under normal operating conditions with low power CMOS RAM's). **Note:** with the Real Time Clock installed, using the same backup battery, the backup capability will be reduced (at least 2 years).

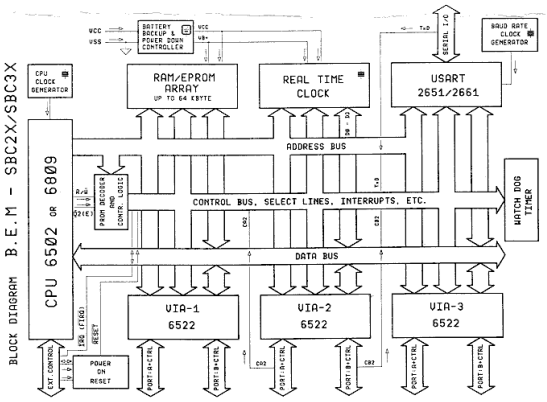
A PROM decoder is used to allocate the map areas of local devices (VIA's, USART, RAM, EPROM and RTC). Decoding is done in minimum blocks of one page (256 bytes). A jumper is used to select between two useful map configurations. The cards are delivered with a standard PROM (2XA), resulting in the maps printed on page 6. Custom map configurations are possible within the limits of the design. Please contact factory or nearest representative for details and cost.

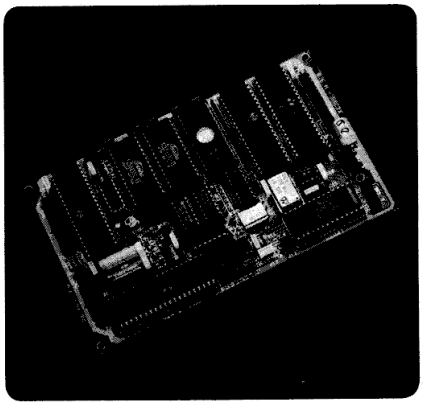
The B.E.M-SBC2X is provided with an NMOS 6502 processor in standard version (CMOS processors, such as the enhanced 65C02 or even the advanced 16-bit 65SC802 are optional). The B.E.M-SBC3X is provided with a NMOS 6809 processor. Clock signals for processor and USART are generated by separate crystal based clock generators. Basic system clock frequencies for both CPU's is 1 MHz in standard version (4 MHz crystal used with 6809 processor).

continued on page 2

FEATURES

- ADVANCED 6502 (B.E.M-SBC2X) AND 6809 (B.E.M-SBC3X) BASED, SINGLE BOARD COMPUTERS
- TWO JUMPER SELECTABLE STANDARD MAP CONFIGURATIONS. MAP 1: UP TO 40 KBYTE RAM AND 16 KBYTE EPROM. MAP 2: UP TO 16 KBYTE RAM AND 32 KBYTE EPROM
- THREE 28-PIN SOCKETS AVAILABLE, ACCEPTING JEDEC JC-42 COMPATIBLE MEMORY DEVICES (e.g. 27XXX FAMILY OF EPROM's)
- SINGLE POWER SUPPLY (+5V) REQUIRED
- REAL TIME CALENDAR CLOCK CIRCUIT WITH INDEPENDENT REGISTERS FROM TENTHS OF SECONDS UP TO TENS OF YEARS. AUTOMATIC LEAP YEAR CALCULATION AND EXTENSIVE INTERRUPT CAPABILITY, PROGRAMMABLE INTERVALS FROM 0.1 SEC. UP TO 60 SEC.
- LITHIUM BATTERY (.85Ah) BACKUP AND POWER DOWN CONTROL CIRCUIT TO MAINTAIN CMOS RAM's DATA INTEGRITY AND CORRECT TIMEKEEPING OF REAL TIME CLOCK DURING POWER DOWN CONDITIONS
- FLEXIBLE WATCH-DOG TIMER AND IMPROVED POWER-ON-RESET CIRCUIT
- SEPARATE CRYSTAL BASED CLOCKS FOR CPU, USART AND RTC
- 3 VIA's (6522) FOR PARALLEL I/O AND TIMER APPLICATIONS, OFFERING A TOTAL OF 60 PARALLEL I/O LINES, 6 TIMER/COUNTERS (16-BIT) AND 3 SHIFTREGISTERS (8-BIT)
- 1 USART (2651/2661) FOR SYNCHRONOUS AND ASYNCHRONOUS SERIAL I/O COMMUNICATION
- STRAIGHT FLAT CABLE HEADERS FOR ALL I/O CONNECTIONS. EXTENDED PINS AT THE SOLDER SIDE FOR ADD-ON APPLICATIONS
- GENEROUS OEM DISCOUNTS AVAILABLE





pin	function (port:A)
1	VCC (+5V)
2	CA1
3	CA2
4	N.C.
5	PA0
6	PA1
7	PA2
8	PA3
9	PA4
10	PA5
11	PA6
12	PA7
13	VSS (0V)

pin	function (port:B)
14	VSS (0V)
15	PB0
16	PB1
17	PB2
18	PB3
19	PB4
20	PB5
21	PB6
22	PB7
23	*
24	CB1
25	CB2
▶26	VCC (+5V)

VIA FLAT CABLE HEADER CONNECTIONS

* Connected to local interrupt via jumper.
See page 8 for details.

continued from page 1

Each 6522 VIA provides two 8-bit bi-directional ports, each with two programmable control lines for handshake or other purposes. Each line can individually be programmed to be input or output. Moreover, two 16-bit programmable interval timers/ counters and an 8-bit shiftregister are available to the user. With all VIA's installed, the cards offer the impressive total of 60 parallel I/O lines, six 16-bit timers/ counters and three 8-bit shiftregisters.

The 2651/2661 USART (Universal Synchronous and Asynchronous Receiver Transmitter) is used for serial communication. The USART is a highly sophisticated device of which all parameters can be programmed (baud rate, parity, stop bits etc.). Applications range from simple terminal or printer control to complex synchronous multi-user networks.

For I/O connections each VIA and USART is connected to a 26-pin respectively 10-pin straight header with a pin lay-out equal to those on other BEM application cards provided with PIA's, VIA's and USART's. Most parallel and serial I/O adapters already available for BEM-BUS compatible cards, including the whole VIOBUS family, can directly be connected to the SBC2X/3X series. Special headers with pins extending at both sides of the print are used for all I/O connections (including the external control header). The headers not only accept standard female flat cable connectors at the component side but also enables the single board computer to be sandwiched to a custom board (add-on module).

The cards are provided with an improved POWER-ON-RESET circuit. Besides to the processor and I/O IC's, the output of this circuit (open collector) is also connected to pin 1 of the Ext. Control header. A remote controlled reset switch (user supplied) can be connected directly between pin 9 and 10 of the same header (switch normally open). If used, the on-board circuit will eliminate contact bounce.

The Watch-dog timer, if installed, activated and properly supported by the software, will cause a hard RESET only at a run time failure.

The Watch-dog timer circuit consists of a multistage counter circuit (4060), instead of a more simple one-shot multivib circuit, avoiding accidental triggering by interference. Application software must take care to clear the counter before it can trigger the RESET circuit. One of three delay times can be selected with a jumper plug (respectively 1x, 2x or 4x the time base). If necessary, the time base (approximately 1.25 sec.) can be changed by replacing the RC components involved. One of three trigger sources can be selected with a jumper plug (respectively CA2 or CB2 of VIA-2 or TxD of the USART). The Watch-dog timer is deactivated by putting the timing jumper plug in the "off" position. The source jumper plug may also be installed in a neutral position.

The Real Time Clock (RTC) circuit, if installed and properly supported, is capable of timekeeping from tenths of seconds up to tens of years in independently accessible registers. Moreover, the MM58274A clock IC, applied on these new boards, is provided with a leap year register and can also be programmed for 12 or 24-hour operation. The build-in test mode and buffered crystal frequency output will simplify oscillator setting. The clock provides extensive interrupt capability, programmable at 0.1, 0.5, 1, 5, 10, 30 or 60 sec. intervals. An individual power source selection jumper plug enables the circuit to profit the on-board Lithium battery, originally intended to backup the (CMOS) RAM's, also to backup the clock. However, If used, the increased current drain will limit the total continuous backup time to approximately 2 years (10 years or more with low power CMOS RAM's only).

A single (+5V) power supply voltage is required to operate the cards. Power supply connections are generally made via the special screw terminal block. However, power supply pins are also available in each I/O connector.

The B.E.M-SBC2X/3X cards are provided with high quality machine tooled sockets. Low Power Schottky IC's are used where possible. Most jumpers are provided with jumper plugs for quick and simple modifications.

EXTERNAL CONTROL HEADER FUNCTIONS

pin	B.E.M-SBC2X
1	$\overline{\text{RESET}}$
2	$\overline{\text{IRQ}}$
3	$\overline{\text{NMI}}$
4	N.C.
5	SYNC
6	RDY
7	VSS (0V)
8	VCC (+5V)
9	EXT. RESET SWITCH
▶10	EXT. RESET SWITCH

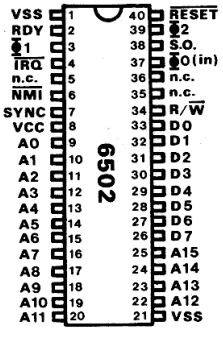
pin	B.E.M-SBC3X
1	$\overline{\text{RESET}}$
2	$\overline{\text{FIRQ}}$
3	$\overline{\text{NMI}}$
4	$\overline{\text{IRQ}}$
5	$\overline{\text{HALT}}$
6	N.C.
7	VSS (0V)
8	VCC (+5V)
9	EXT. RESET SWITCH
▶10	EXT. RESET SWITCH

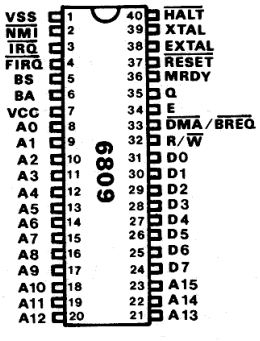
USART FLAT CABLE HEADER CONNECTIONS

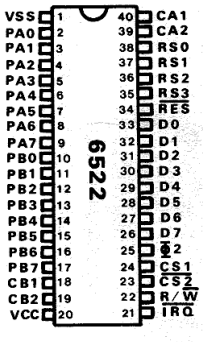
pin	function
1	VSS
2	$\overline{\text{DCD}}$
3	$\overline{\text{CTS}}$
4	TxD
5	VCC/$\overline{\text{DSR}}$ *
6	$\overline{\text{RTS}}$
7	$\overline{\text{DTR}}$
8	$\overline{\text{RxC}}$
9	$\overline{\text{TxC}}$
▶10	RxD

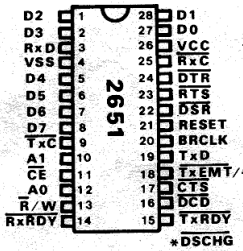
* Strapped to VCC in standard version. See page 8 for details.

CPU, VIA AND USART PIN CONNECTIONS









ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias..... 0°C to + 70°C
Storage Temperature..... -55°C to + 85°C
Voltage on any Pin with respect to ground..... -0.3 V to + 7 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the B.E.M-SBC2X/SBC3X cards. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

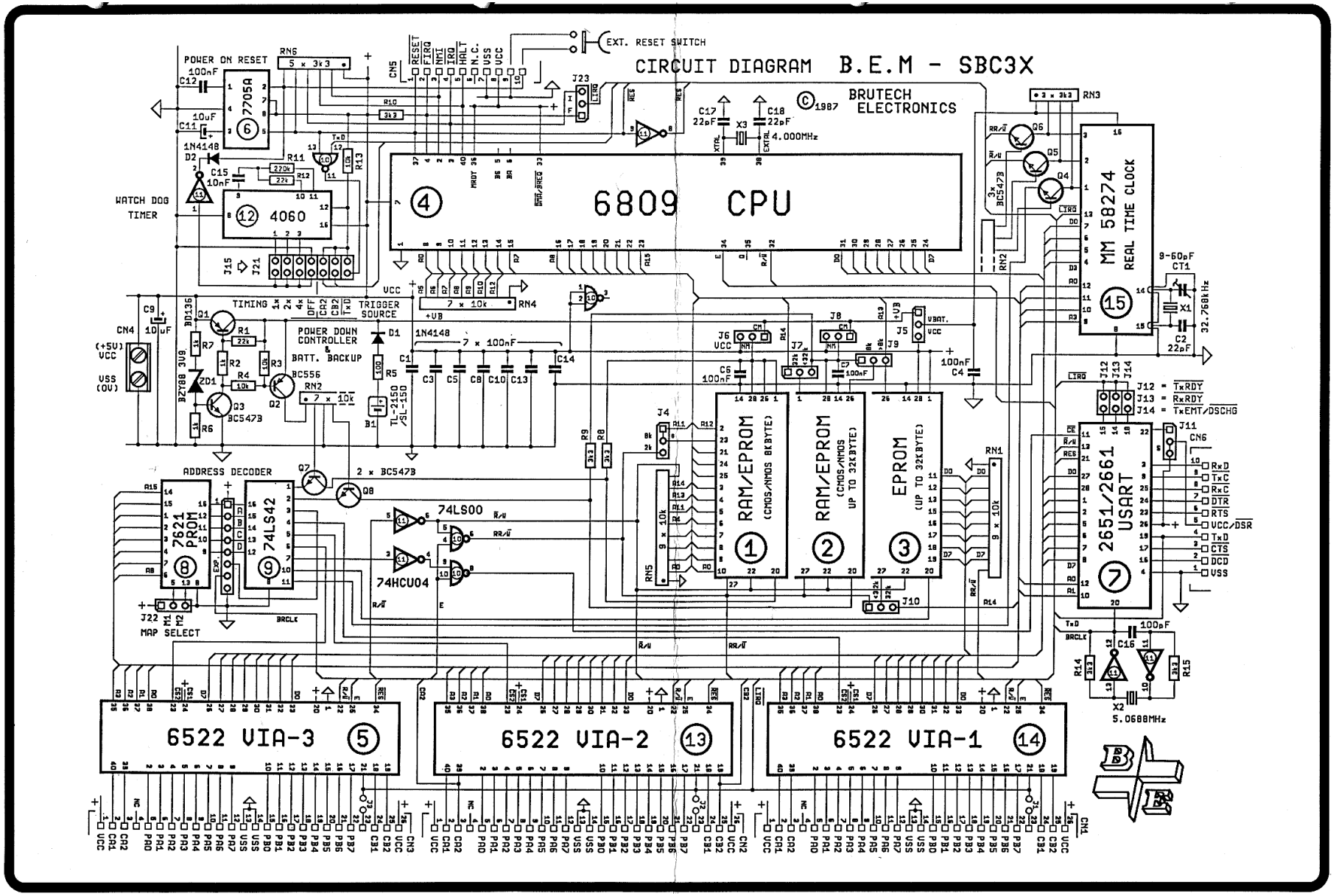
DC CHARACTERISTICS

TA = 0°C to +70°C, VCC = +5.0 V ±5% (unless otherwise specified)

	Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Unit	Test Conditions
CARD CURRENT		VCC Power Supply Current with VIA's in input mode and without EPROM's					
	I_{CC}	SBC2X, 8 kbyte RAM, 1 VIA & 1 USART		430	650	mA	
		SBC2X, 40 kbyte RAM, 3 VIA's & 1 USART		640	980	mA	VCC = 5.25V TA = 0°C
		SBC3X, 8 kbyte RAM, 1 VIA & 1 USART		480	730	mA	(worst case conditions)
		SBC3X, 40 kbyte RAM, 3 VIA's & 1 USART		690	1040	mA	
VIA	V_{IHV}	Input Voltage "High level"	2.4		VCC	V	
	V_{ILV}	Input Voltage "Low Level"	-0.3		0.4	V	
	I_{INV}	Input Leakage Current CA1			±2.5	µA	V_{IN} = 0 to 5V
	I_{IHV}	Input "High" Current PA0 → PA7, CA2, PB0 → PB7, CB1, CB2	-100			µA	V_{IN} = 2.4V
	I_{ILV}	Input "Low" Current PA0 → PA7, CA2, PB0 → PB7, CB1, CB2			-1.6	mA	V_{IN} = 0.4V
	V_{OHV}	Output "High" Voltage PA0 → PA7, CA2 PB0 → PB7, CB1, CB2	2.4			V	I_L = -100 µA
	V_{OLV}	Output "Low" Voltage PA0 → PA7, CA2 PB0 → PB2, CB1, CB2			0.4	V	I_L = 1.6 mA
	I_{OHV}	Output "High" Current (Sourcing)	-100			µA	V_{OH} = 2.4V
			-1.0			mA	V_{OH} = 1.5V (PB0 → PB7)
	I_{OLV}	Output "Low" Current (Sinking)	1.6			mA	V_{OL} = 0.4V
	I_{OFF}	Output Leakage Current $\overline{IRQ}$ (Off State)			10	µA	
	C_{IN}	Input Capacitance PA0 → PA7, CA1, CA2, PB0 → PB7			7	pF	1 MHz
		Idem CB1 and CB2			10	pF	1 MHz (Φ2, E)
	C_{OUT}	Output Capacitance			10	pF	1 MHz
USART	V_{ILU}	Input Voltage "Low Level" any Input Pin	-0.3		0.8	V	
	V_{IHU}	Input Voltage "High Level" any Input Pin	2.0			V	
	V_{OLU}	Output Voltage "Low Level" any Output Pin			0.4	V	I_{OL} = 1.6mA
	V_{OHU}	Output Voltage "High Level" any Output Pin	2.4			V	I_{OH} = -100µA
	I_{ILU}	Input Leakage Current any Input Pin			10	µA	V_{IN} = 0 to +5.5V

WARNING

VIA's and USART contain circuitry to protect the inputs against damage due to static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these circuits.


CIRCUIT DIAGRAM B.E.M - SBC3X
©1987 BRUTECH ELECTRONICS
6809 CPU
6522 VIA-3
6522 VIA-2
6522 VIA-1
RAM/EPROM (CMOS/NMOS 8KBYTE)
RAM/EPROM (CMOS/NMOS UP TO 32KBYTE)
EPROM (UP TO 32KBYTE)
MM 58274 REAL TIME CLOCK
2651/2661 USART
7621 PROM
74LS42
74LS00
74HCU04
4060
7705A
POWER ON RESET
WATCH DOG TIMER
TIMING
TRIGGER SOURCE
POWER DOWN CONTROLLER & BATT. BACKUP
ADDRESS DECODER
MAP SELECT
EXT. RESET SWITCH
4.000MHz
5.0688MHz
32.768kHz

MEMORY MAP AND REGISTER ADDRESSES

Two practical memory map configurations can be selected with the standard PROM decoder (2XA), simply by changing the position of a jumper plug (J22). The drawing to the right shows both maps in detail. Custom map configurations are possible within the limits of the design. Please contact factory or nearest representative for details and cost.

Several memory configurations are possible. EPROM/ROM or RAM devices may be applied in the sockets 1 and 2. Socket 3 is generally reserved for read only devices (EPROM/ROM) containing not only the program but in particular the vector addresses at the top locations of the memory map. At least one socket must contain RAM (stack and variable storage). In case of the B.E.M-SBC2X the lowest part of the map must contain RAM (direct page and stack are fixed). In case of the SBC3X, RAM may be located almost anywhere in the map. Only JEDEC JC-42 compatible devices can be applied on the B.E.M-SBC2X & SBC3X single board computers. The basic memory type limitations are listed below. Jumper settings can be found in the next chapter.

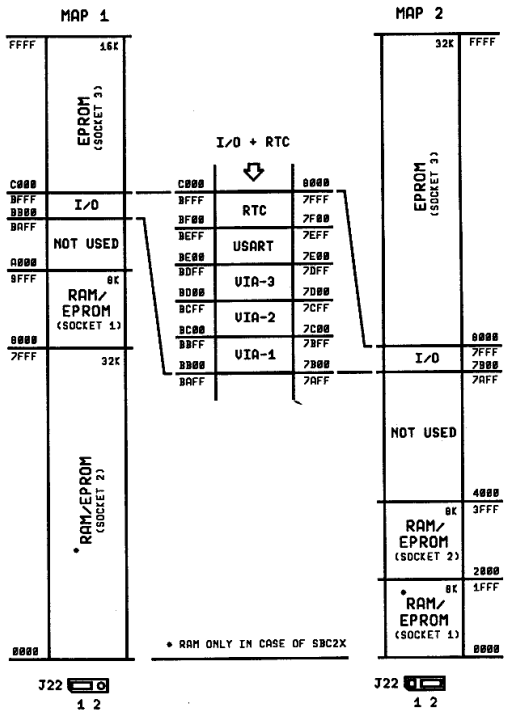
MEMORY SOCKET 1 : Jumper J6 is used to select battery backup or not for this socket. Battery backup is intended to be used only with a CMOS RAM (e.g. TC5564) in this socket. Jumper J4 is strapped (standard version) to accept a 8 kbyte RAM. However, the strap can be removed and rewired in the opposite position to allow the application of a 2 kbyte RAM (e.g. TC5517) in this socket. Without backup, also an EPROM can be applied (e.g. 2764 but also a 4 kbyte 2732 may be used). 2716/2516 EPROM types (2 kbyte) can not be used, not even with J4 in the 2k position.

MEMORY SOCKET 2: This socket can also be configured to accept many different devices (jumpers J7 and J9), backed up by battery or not (J8). With battery backup, a 8 kbyte (e.g. TC5564) or 32 kbyte (e.g. TC55257) CMOS RAM can be applied. Without backup, also a 4 kbyte (e.g. 2732), 8 kbyte (e.g. 2764) or 16 kbyte (e.g. 27128) EPROM can be installed.

MEMORY SOCKET 3: This socket is designed to accept only read only devices of 8kbyte (e.g. 2764), 16 kbyte (e.g. 27128) up to 32 kbyte (e.g. 27256), selected by jumper J10.

The absolute addresses of VIA's, USART and RTC are dependent on the selected map configuration. Each device occupies 1 page (256 bytes). Therefore the register map of each device will be echoed at several locations within that particular page. The absolute addresses of the I/O devices are respectively:

SBC2X/SBC3X MEMORY MAP
(WITH 2XA STANDARD DECODER PROM)



DEVICE	MAP 1	MAP 2
RTC	$BFXR	$7FXR
USART	$BEXR	$7EXR
VIA-3	$BDXR	$7DXR
VIA-2	$BCXR	$7CXR
VIA-1	$BBXR	$7BXR

X = HEX value 0 → F

R = relative address (see table below)

DEVICE	RELATIVE ADDRESS	FUNCTION/REGISTER		
		NAME	WRITE	READ
VIA	0	ORB/IRB	Output Register Port "B"	Input Register Port "B"
	1	ORA/IRA	Output Register Port "A"	Input Register Port "A"
	2	DDRB	Data Direction Register Port "B"	
	3	DDRA	Data Direction Register Port "A"	
	4	T1L/C-L	T1 Low-order Latch	T1 Low-order counter
	5	T1C-H	T1 High-order Counter	
	6	T1L-L	T1 Low-order Latch	
	7	T1L-H	T1 High-order Latch	
	8	T2L/C-L	T2 Low-order Latch	T2 Low-order Counter
	9	T2C-H	T2 High-order Counter	
	A	SR	Shift Register	
	B	ACR	Auxilliary Control Register	
	C	PCR	Peripheral Control Register	
	D	IFR	Interrupt Flag Register	
	E	IER	Interrupt Enable Register	
	F	ORA/IRA	Same as address 1, except no "handshake"	

DEVICE	RELATIVE ADDRESS				FUNCTION/REGISTER		
					NAME	WRITE	READ
USART	0	4	8	C	THR/RHR	Transmit Holding Register	Receive Holding Register
	1	5	9	D	SSDR/SR	SYN 1 / SYN 2 / DLE Register *	Status Register
	2	6	A	E	MR	Mode Register 1/2 *	
	3	7	B	F	CR	Command Register	

* **NOTE:** Each time a WRITE is made to the SYN 1 / SYN 2 / DLE address and a WRITE or READ is made to or from the Mode Registers 1/2, an internal counter is incremented. The counters are wrapped around. For programming the Mode Registers 1/2 this has some consequences in case of the B.E.M-SBC2X (6502 CPU). The instruction "STA (INDIRECT),Y" will put the same address twice on the bus if no page crossing occurs. A dummy READ operation is performed before each WRITE operation. As a result the internal counter is incremented before the WRITE operation really takes place. A write operation to the Mode Registers in the indirect indexed mode (***and no page crossing***) can be done in the following way:

```
EXAMPLE  (ADDR = base address of USART)

LDY #3
LDA (ADDR),Y   ;CLEAR INTERNAL COUNTERS
LDA #MODE2
DEY
STA (ADDR),Y   ;WRITE MODE REGISTER 2
LDA (ADDR),Y   ;INCREMENT INTERNAL COUNTER
LDA #MODE1
STA (ADDR),Y   ;WRITE MODE REGISTER 1
```

SUMMARY OF MM58274A (REAL TIME CLOCK) ADDRESS DECODING AND INTERNAL REGISTERS

MM58274A REGISTER TABLE

RELATIVE ADDRESS	REAL TIME CLOCK COUNTER/REGISTER FUNCTIONS
0	Read / Write Control Register
1	**Read only** Tenths of seconds Register
2	Read / Write Units of seconds Register
3	Read / Write Tens of seconds Register
4	Read / Write Units of minutes Register
5	Read / Write Tens of minutes Register
6	Read / Write Units of hours Register
7	Read / Write Tens of hours Register
8	Read / Write Units of days Register
9	Read / Write Tens of days Register
A	Read / Write Units of months Register
B	Read / Write Tens of months Register
C	Read / Write Units of years Register
D	Read / Write Tens of years Register
E	Read / Write Day of week Register
F	Read / Write Clock Setting Register / *
	Read / Write Interrupt Control Register

* Determined by interrupt select bit in the control register.

INTERRUPT CONTROL REGISTER
(relative address $F, Read / Write mode)

FUNCTION		D3	D2	D1	D0
No Interrupt	* 1	x	0	0	0
0.1 sec. intervals	* 2	0/1	0	0	1
0.5 sec. intervals		0/1	0	1	0
1 sec. intervals		0/1	0	1	1
5 sec. intervals		0/1	1	0	0
10 sec. intervals		0/1	1	0	1
30 sec. intervals		0/1	1	1	0
60 sec. intervals		0/1	1	1	1

NOTES:

D3 = x, Don't care
D3 = 0, Single interrupt
D3 = 1, Repeated interrupts

* 1 Interrupt output cleared, start/stop bit set to 1 (see also "control register bit allocation" table).

* 2 Basic accuracy: single interrupt ± 1 msec., also ± 1 msec. for initial timeout in case of repeated interrupts, but thereafter synchronous with first interrupt (i.e. timing errors do not accumulate).

CONTROL REGISTER BIT ALLOCATION
(relative address $0, split Read and Write)

DATA	READ	WRITE
D0	Interrupt flag 0 = No interrupt 1 = Interrupt	Interrupt start/stop 0 = Interrupt run 1 = Interrupt stop
D1	0	Interrupt select 0 = Clock setting register 1 = Interrupt register
D2	0	Clock start/stop 0 = Clock run 1 = Clock stop
D3	Data change flag 0 = No change 1 = Changed	Test bit, 0 = Normal 0 = Normal 1 = Test mode

CLOCK SETTING REGISTER BIT ALLOCATION
(relative address $F, Read / Write mode)

FUNCTION	D3	D2	D1	D0
Leap year counter 0 = leap year	x	x		
12 / 24 Hour select bit 0 / 1 = 12 / 24 hour mode				x
AM / PM Bit (12 hour mode), 0 = AM, 1 = PM 0 in 24 hour mode			x	

NOTES: The 2-bit binary leap year counter changes state as time rolls over from 23:59 on December 31 to 00:00 on January 1. The counter should be loaded with the number of years since the last leap year e.g., if 1984 was the last leap year, for 1986 the value 2 (10 binary) must be stored in the leap year counter. Hours mode and AM/PM bits can not be set in the same write operation.

MM58274A APPLICATION NOTES

1) For detailed description, the original data sheet of the National Semiconductor MM58274A Real Time Clock IC is recommended. However, if the software examples are strictly followed, generally no problems will arise.

2) The MM58274A operates via a 4-bit databus. The lower 4 bits of the 8-bit card databus are used for this purpose. When reading data from the RTC, the highest nibble must be ignored.

3) In the test mode, the MM58274A provides a buffered crystal frequency output, accessed via the local interrupt of the card. Be sure that interrupts from other sources are disabled during the calibration procedure.

4) The Data Change Flag (DCF) is used to test the validity of read data, it will be set when a register is changed. The following procedure should be used to read data correctly: **[A]** Read control register to clear the DCF. **[B]** Read all necessary time/date registers. **[C]** Read control register and check DCF. **[D]** If the flag is set, go to **[B]** and continue from there. If the flag is not set, data will be correct.

5) Interrupts ar initiated and serviced in the following way: **[A]** Write 3 to the control register (clock timing continuous, interrupt register selected and interrupt timing stopped). **[B]** Select interval by writing the interrupt register (relative address $F). **[C]** Write 0 or 2 to the control register (time and interrupt both running). **[D]** On interrupt: read the control register and test the interrupt flag (automatically cleared after read operation). In the repeat mode no further action will be required. In the single interrupt mode, a new interval will be started by writing again 0 or 2 to the control register. **[E]** Interrupts can be stopped by writing a 1 to bit 0 of the control register.

6) Interrupts from the RTC are not disabled during power-on and reset. The interrupt can be set during power down (assuming the RTC is backed up by battery). If interrupts are enabled the time the power is removed, they still are enabled at power-on and the interrupt is probably set at that time. Be aware that the interrupt line may be active directly after power-on. Resetting or disabling the RTC interrupt before the interrupts are enabled by the processor (CLI) is good practice.

7) The software examples are listed in 65xx assembler langauge only. Translation to 6809 assembler language will be easy.

RTC SOFTWARE EXAMPLES

READ TIME : Read hours, minutes and seconds from RTC and save them in RAM. The six values are stored in the lower nibble of six RAM locations (TIME → TIME+5). The DCF flag is checked and must be correct within 3 retries, otherwise the last readed data is copied. It is assumed that the total read operation of the six registers is done within the internal update time of the clock (if not the DCF flag will always be set). In case interrupts are used in the system, they must be disabled during the clock read procedure or the interrupt handling time must be shorter than the DCF interval. RTC is the clock base address.

```
RTIME   LDA #3          3 retries
        STA LOOP        Retry counter
        LDA RTC         Clear DCF
RTIME1  LDX #5          6 registers
RTIME2  LDA RTC+2,X     Index to Units Seconds
        STA TIME,X      Save value
        DEX
        BPL RTIME2      Repeat 6 times
        LDA RTC         Read Control register
        AND #8          Get DCF
        BEQ RTDONE      Not set
        DEC LOOP
        BNE RTIME1      3 retries
RTDONE  RTS
```

SET TIME : Six values from RAM are written in six RTC registers for hours, minutes and seconds. The RTC is stopped first and the test mode bit is reset. The 24 hours mode will be selected and the clock is started after the registers are written.

```
WTIME   LDA #5          Stop, exit test, interrupts stopped
        STA RTC         Write control register and select CSR at $F
        LDA RTC+15      Read CSR
        AND #$C0        Preserve leap year bits
        ORA #1          Select 24 hour mode
        STA RTC+15      Write CSR
        LDX #5          Six registers
WTIME1  LDA TIME,X
        STA RTC+2,X     Write relative to Units Seconds
        DEX
        BPL WTIME1      Repeat 6 times
        LDA #3          Start clock, interrupts stopped
        STA RTC         ICR selected
        RTS
```

JUMPERS

The B.E.M-SBC2X/3X cards are provided with many jumpers to adapt the cards to almost any user requirements. Most jumpers are provided with jumper plugs for quick and simple modifications. However, some are strapped in a preferential position. The jumper functions will be described below in consecutive order. Correct positions of jumper plugs will be found in the mechanical lay-outs on page 10.

The jumpers **J1**, **J2** and **J3**, each located near the parallel I/O header of the corresponding VIA (J1 for VIA-1 etc.) are used to connect pin 23 of the header individually to the local interrupt line on the card. The local interrupt line is directly connected to $\overline{IRQ}$ in case of the B.E.M-SBC2X but to $\overline{IRQ}$ or $\overline{FIRQ}$ (dependent on jumper J23) in case of the B.E.M-SBC3X.

Jumper **J4**, located to the left of memory socket 1, is strapped for 8 kbyte. Cutting the strap and rewiring the jumper in the opposite position will allow the application of a 2 kbyte RAM (e.g. TC5517) in this socket. J4 is implemented to maintain compatibility with the older SBC2/SBC3 designs.

The jumpers **J5**, **J6** and **J8**, located near the upper card edge, are used to select battery backup for respectively the RTC (Real Time Clock) and the memory sockets 1 and 2.

The jumpers **J7** and **J9**, located respectively near pin 1 of memory socket 2 and pin 1 of socket 3, are used to prepare socket 2 to accept either a 32 kbyte RAM or a smaller device (J7). J9 is used further to select between 8 kbyte (RAM or EPROM) or higher (e.g. a 16 kbyte EPROM or 32 kbyte RAM).

Jumper **J10** is used to prepare memory socket 3 to accept either a 32 kbyte EPROM (e.g. 27256) or a smaller device (16 kbyte or 8 kbyte EPROM, e.g. 27128 or 2764).

Jumper **J11** is used to connect either VCC (strapped) or $\overline{DSR}$ from the USART to pin 5 of the serial I/O header CN6.

The jumpers **J12**, **J13** and **J14** are respectively used to connect the $\overline{TxRDY}$, $\overline{RxRDY}$ and $\overline{TxEMT/DSCHG}$ interrupt sources from the USART to the local interrupt line.

The jumper array **J15 up to J21** is used to set the watchdog parameters. The jumpers J15, J16 and J17 select respectively the delay time multiplication factors 1x, 2x and 4x of the time base (approx. 1.25 sec.). With the jumper plug in position J18, the watchdog timer is switched-off. The retrigger source for the watchdog timer can be selected with the jumper locations J19, J20 and J21. These jumper locations select respectively CA2 of VIA-2, CB2 of VIA-2 and TxD of the USART as a retrigger source. Retriggering of the watchdog timer (must occur before time-out of the timer) is done by a short positive going pulse at the input of the timer. In case TxD of the USART is used as a source, an inverter takes care to provide the correct pulse conditions. TxD, as a source, will generally be used in those applications where data is transmitted via the serial port in a more or less continuous stream.

Jumper **J22** is used to select one of two useful memory map configurations (see also memory map section for details)

Finally jumper **J23** (B.E.M-SBC3X only) is used to connect the local interrupt line either to $\overline{IRQ}$ or $\overline{FIRQ}$ of the processor.

THE WATCHDOG TIMER

See general description on page:2 and the J15 up to J21 jumper array description in the previous chapter.

NOTES

1) For detailed description of the 6502/6809 CPU's, 6522 VIA, 2651/ 2661 USART's and the RTC, the data sheets of the original manufacturer or second source manufacturer is recommended.

2) In the circuit diagrams on the pages 4 and 5, the numbers within a circle refer to the position of the IC in the mechanical lay-outs on page 10.

3) An external RESET switch, profiting the anti-bounce characteristics of the on-board POWER-ON-RESET circuit, can be connected between the pins 9 and 10 of the external control header (CN5). The user supplied switch must be of the "normal open" type.

4) The RAM and EPROM sockets are 28-pin types. The pins are therefore numbered from 1 to 28. These numbers are used in the circuit diagrams to denote memory device pin numbers. In case 24-pin memory devices are used in a socket, pin 1 of the device must correspond with pin 3 of the socket.

MECHANICAL SPECIFICATIONS

1) PRINTED CIRCUIT: 1.6 mm. Epoxy glass fiber reinforced in Euro Card format (100 x 160 mm.). Double sided metallized with plated through holes, covered with an epoxy mask on both sides and finished with a component lay-out in white epoxy overprint.

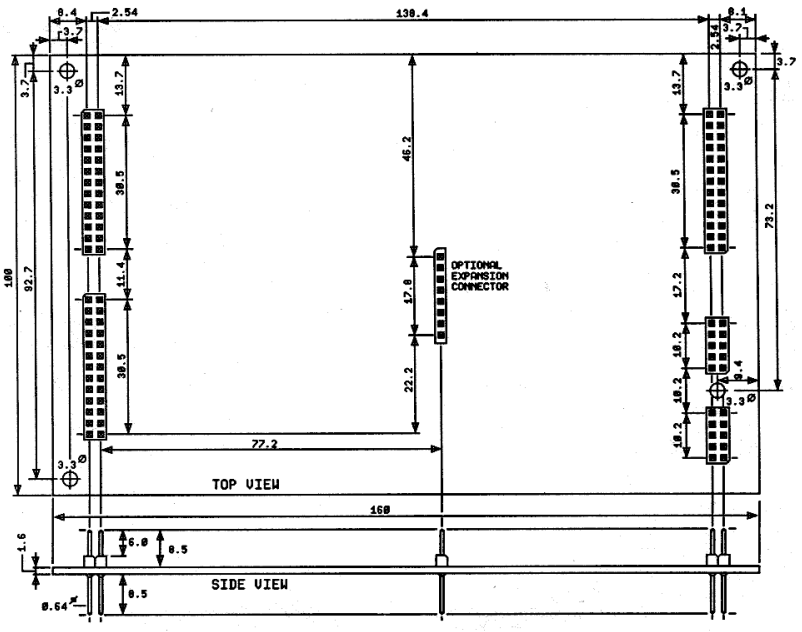
2) HEADERS: 3 x 26-pin and 2 x 10-pin straight double row BERGSTICK headers, accepting standard female socket connectors designed for flat cable with 0.05" (1.27 mm.) conductor spacing. Extended pins at the solder side for add-on applications.

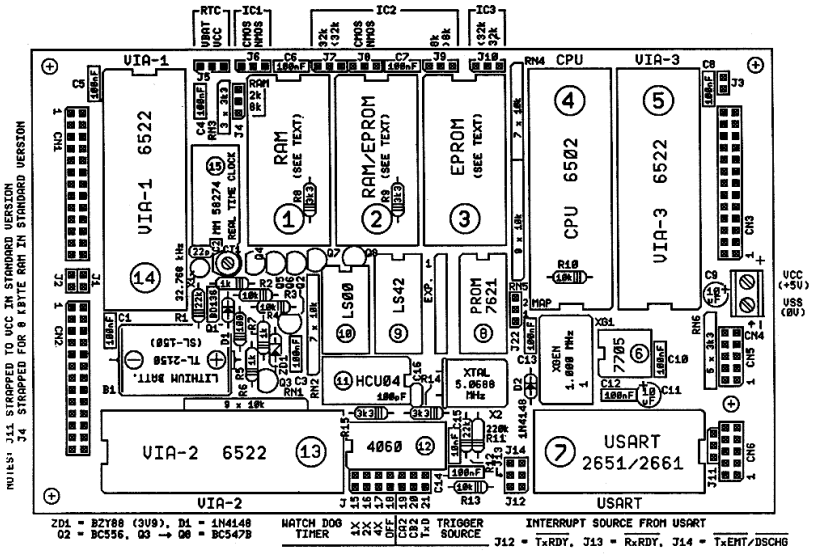
3) STANDARD version with high quality machine tooled sockets.

4) MAXIMUM THICKNESS:
   * All versions: 20.2 mm.
     Solder side: – 8.5 mm.
   * Component side: +10.0 mm.

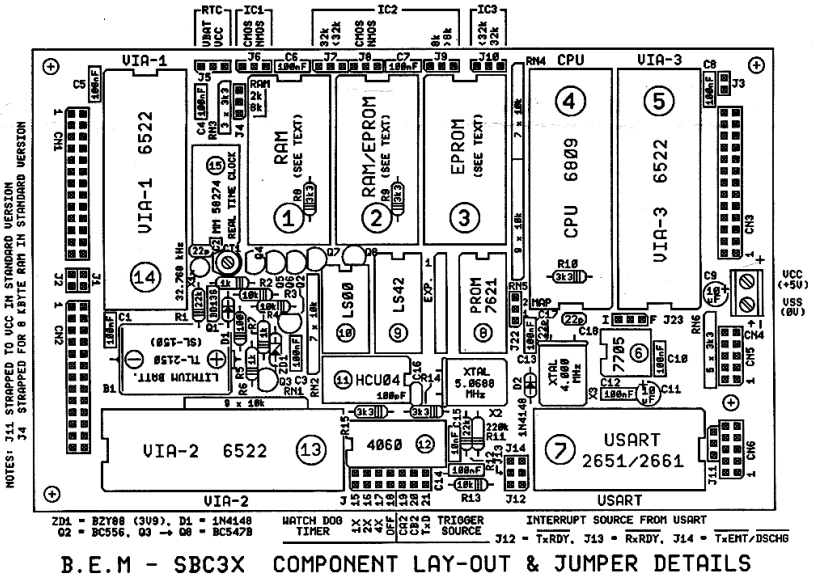
   * add 4.0 mm. for Lithium battery

B.E.M-SBC2X / SBC3X CONNECTOR LOCATIONS (DIMENSIONS IN MM.)





B.E.M - SBC2X COMPONENT LAY-OUT & JUMPER DETAILS



B.E.M - SBC3X COMPONENT LAY-OUT & JUMPER DETAILS

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ALL CARDS ARE FULLY TESTED AND BURNED-IN BEFORE SHIPMENT