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Dear Sir,

I have the pleasure to inform you of the availability of the new Workshop Engineer Manual:

W E MANUAL VOL. 4 (SECONDARY STORAGE CO'S)

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In this (new) volume all Secondary Storage Controllers have been put. The information is updated to the state of the art. Most of them come from the old volume 1, which is now dedicated to PMU Boards. Some new controllers have been added.

Best Regards,

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FIXC05 EXERCISE - SCSI COMMANDS

1. Start the system. Access the fixed drive (for example DIR:a)

2. ., run the Monitor program and load the SCSI program via which you can issue SCSI commands.
(See HO SCSI)

3. Run the SCSI program and do the "Test Unit Ready" command.

WARNING: Before you issue an SCSI command, ensure that you use the right Bus Device ID (FIXC08 Device ID = 80 hex). A wrong Bus Device ID could erase data of another Bus Device, e.g. of a tape unit. Ensure also that the data on disc can be erased.

4. Check the status byte returned after the command. It should be: 02 (hex), error occurred. (Note: This is not a real error. The error indication is given due to the reset.)

5. Do "Request Sense" command to get four status bytes returned by DMA.

6. Check the status byte which is returned immediately after the command. It should be: 00 (hex), no errors occurred.

7. Display the four status bytes which are returned to the DMA area in the host's memory. These should be:

   0F Question: What does 0F mean?
   00)
   00)- No meaning
   00)

8. What is the firmware revision number of the FIXC08 used?

9. Do command "Rezero Unit".

10. Write one data block, which e.g. contains your own name, onto disc. Read the data block back, after you have first cleared the DMA area in the memory.

11. What is the "number of sectors per track" .

12. Try now other commands.

SCSI PROGRAM - FIXCO 5 AND TAPCO-Q W.E. COURSES

The SCSI Program allows you to send command bytes to disc and tape controllers, which are connected to the SCSI bus. So, you can play the role of the host computer. The SCSI program runs under the Monitor program. By means of Monitor directives (commands), you can edit data in the host's memory.

HOW TO USE THE SCSI PROGRAM?

The SCSI Program is started as follows:

PROMPT	ENTER	DESCRIPTION
0A>	master	Attach your workstation (operator's console) to the Master MPU. Note that the prompt 0A is an example (0 = User Nbr.; A = disc A).
0A>	buffers n2	
0A>	monitor	Run the Monitor program.
*	l b:scsi.com	Load SCSI program from disc B (B is example)
*	g 100	Run SCSI Program (Go to address 100)

The SCSI program structure is as follows:

1. Enter Device ID. For FIXCO 5 80(hex); for TAPCO-Q: 08(hex).
2. Enter Command Byte 0.
3. Other bytes zero?
   Yes: go to step 6.
   No : continue.
4. Enter Command Bytes 1 to 5.
5. Enter direction. Direction of the DMA transfer: from or to the host's memory.
6. The program transmits the six-bytes command string.
7. If data must be transferred during command execution, it is read from or written into the current host's DMA address.
8. After command execution, the program displays the Status Byte. You can continue with step 2.

OTHER PROGRAM INFORMATION

- Start address of SCSI program is 100(hex).
- Entering a Q (Quit) terminates the Monitor program (back to Monitor).
- The DMA base address in the host's memory is 1000(hex).
- When you choose "other bytes zero? - yes", then the direction of the DMA data transfer is set to: "write to host's memory".

MONITOR Command

The MONITOR command provides various facilities under Z80 TurboDOS useful to programmers who have the need to debug or patch programs and files.

Syntax

```
MONITOR
```

Explanation

The MONITOR command operates in an interactive mode. You are prompted by an asterisk * to enter a series of directives from the console. The Q directive (quit) terminates the MONITOR command.

In the directive descriptions that follow, all addresses and other numeric arguments are in hexadecimal, and all file names ("fn") are entered as {d:}filename{.typ}:

Directives

Directive	Explanation
C v1,v2	Calculates the sum and difference of two hex values.
D a1,a2	Dumps the area of memory between the two given addresses in hex. Pause with space, resume with RETURN.
E a	Examines memory starting at the given address. You may substitute a new hex value for each displayed byte of memory. Enter space or RETURN to go on to the next byte, or ESC to exit examine mode.

HO SCSI 2

Directives (Continued)

Directive	Explanation
F a1,a2[,v[,r]]	Fills the area of memory between the two given addresses with the given value v (or 0 if no value is given). If a repetition factor r is given, the operation is repeated r times (useful with some PROM programmers).
G a	Goes (jumps) to the instruction at the given address.
H	Help menu is displayed, listing all MONITOR directives.
I p	Inputs a byte from I/O port p and displays its hex value.
L fn [a]	Loads the named file into memory starting at the given address (or 0100H if no address is given).
M a1,a2,a3[,r]	Moves the block of memory between a1 and a2 into the area starting at a3. If a repetition factor r is given, the operation is repeated r times (useful with some PROM programmers).
O p,v	Outputs the hex value v to I/O port p.
P a	Puts succeeding typed ASCII data into memory starting at the given address. Terminate by typing CTRL-D (ASCII EOT).

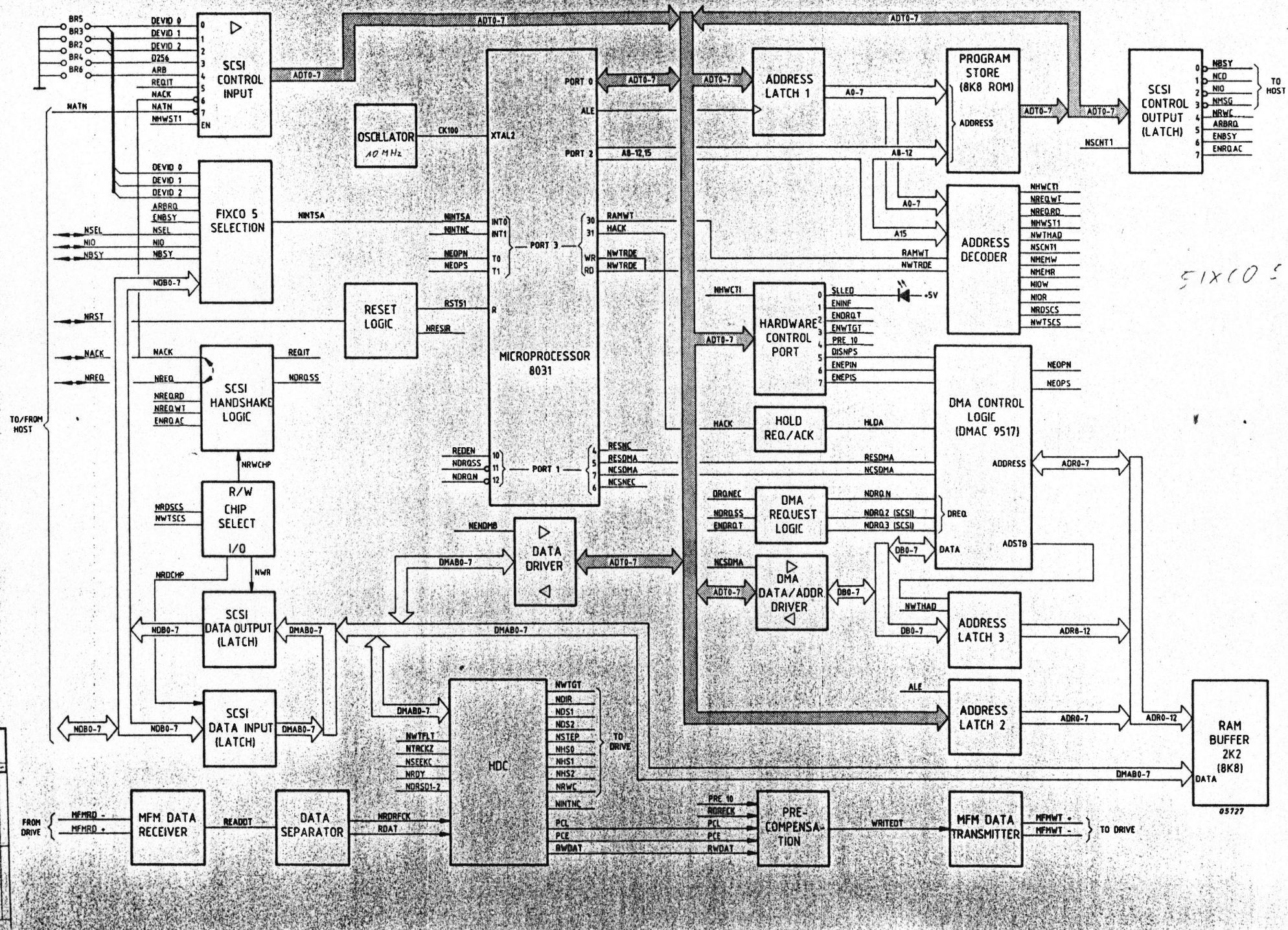
Directives (Continued)

Directive	Explanation
Q	Quits the monitor command.
R a1,a2	RAM area between a1 and a2 is tested, and memory errors are diagnosed. Typing ESC aborts the test early.
S fn (a1,a2)	Saves the area of memory between the given addresses in the named file. If no memory addresses are given, then the bounds from the last L (Load) directive are used.
T a1,a2	Types the area of memory between the given addresses in ASCII. Pause with space, resume with RETURN.
V a1,a2,a3	Verifies that the block of memory from a1 to a2 is identical to the area starting at a3. Any descrepancies are diagnosed.
W v1,...,vN	Scans all of memory for occurrences of the given byte string, and displays Where each occurrence is found.
Y	Displays the highest available address in memory (below TurboDOS and the MONITOR command code).

HO SCSI 4

NMEMW	Memory Write
MFMRD1+	Modified Frequency Modulated Read 1 +
MFMRD1-	
MFMRD2+	
MFMRD2-	
MFMWT1+	Modified Frequency Modulated Write 1 +
MFMWT1-	
MFMWT2+	
MFMWT2-	
NMSG	Message
NIND	Index
PRE10	
NPSEN	Program Store Enable
NRDDMB	Read DMA Bus
RDRFCK	
NRDSCS	Read SCSI Data Input
NRDY	Ready
REDEN	Read Enable
NREQ	Request
REQIT	Request Internal
NREQRD	Request Read
NREQWT	Request Write
RESDMA	Reset DMA Controller
NRESIR	Reset Internal
RESNC	Reset NC
NRST	Reset
RST51	Reset
NRWC	Read/Write Command
RWDAT	Read/Write Data
RWDATS	
NSCNT1	SCSI Control 1
NSEEKC	Seek Command
NSEL	Select
SELED	Selected
SELIR	Select Internal
NSTEP	Step
TERMP	
NTRCKZ	Track Zero
WONA	Won Arbitration
NWTFLT	Write Fault
NWTGT	Write Gate
WTGT	
NWTHAD	Write High Address (of RAM)
NWTSCS	Write SCSI (Data Output)

HO WE 3


SCSI CONTROL INPUT
DEVID 0
DEVID 1
DEVID 2
D256
ARB
REQIT
NACK
NATN
NHWST1
BR5
BR3
BR2
BR4
BR6
ADT0-7
OSCILLATOR
10 MHz
CK100
XTAL2
MICROPROCESSOR 8031
PORT 0
ALE
PORT 2
A8-12,15
PORT 3
PORT 1
INT0
INT1
T0
T1
WR
RD
NINTSA
NINTNC
NEOPN
NEOPS
RAMWT
HACK
NWTRDE
RESNC
RESDMA
NCSDMA
NCSNEC
REDEN
NDRQSS
NDRQN
FIXCO 5 SELECTION
NSEL
NIO
NBSY
NDB0-7
RESET LOGIC
RST51
NRESIR
NRST
SCSI HANDSHAKE LOGIC
REQIT
NDRQSS
NREQ
NREQRD
NREQWT
ENRQAC
NRWCHP
R/W CHIP SELECT I/O
NRDSCS
NWTSCS
NRDCHP
NWR
NENDMB
DATA DRIVER
DMAB0-7
SCSI DATA OUTPUT (LATCH)
SCSI DATA INPUT (LATCH)
HDC
NWTGT
NDIR
NDS1
NDS2
NSTEP
NHS0
NHS1
NHS2
NRWC
NINTNC
TO DRIVE
NWTFLT
NTACKZ
NSEEKC
NRDY
NDRSD1-2
FROM DRIVE
MFMRD -
MFMRD +
MFM DATA RECEIVER
READDT
DATA SEPARATOR
NRDRFCK
RDAT
PRE 10
RDRFCK
PCL
PCE
RWDAT
PRE-COMPENSATION
WRITEDT
MFM DATA TRANSMITTER
MFMWT +
MFMWT -
TO HOST
NBSY
NCD
NIO
NMSG
NRWC
ARBRQ
ENBSY
ENRQAC
SCSI CONTROL OUTPUT (LATCH)
NSCNT1
ADDRESS LATCH 1
A0-7
A8-12
A15
PROGRAM STORE (8K8 ROM)
ADDRESS
ADDRESS DECODER
NHWCTI
NREQWT
NREQRQ
NHWST1
NWTHAD
NSCNT1
NMEMW
NMEMR
NIOW
NIOR
NRDSCS
NWTSCS
HARDWARE CONTROL PORT
SLLED
ENINF
ENDRQT
ENWTGT
PRE 10
DISNPS
ENEPIN
ENEPIS
+5V
HOLD REQ/ACK
HLDA
DMA CONTROL LOGIC (DMAC 9517)
NEOPN
NEOPS
RESDMA
NCSDMA
ADDRESS
ADR0-7
DRQNEC
NDRQSS
ENDRQT
DMA REQUEST LOGIC
NDRQN
NDRQ2 (SCSI)
NDRQ3 (SCSI)
DREQ
DATA
ADSTB
DB0-7
NCSDMA
DMA DATA/ADDR DRIVER
ADDRESS LATCH 3
ADR8-12
ADDRESS LATCH 2
ALE
RAM BUFFER 2K2 (8K8)
DATA
05727
TO/FROM HOST
FIXCO 5

INTRODUCTION TO FIXCO 5

The FIXCO5 is a fixed-disc controller which can control up two 5 1/4" Fixed Disc Drives of the Rodime 200 series or the Seagate 400 series. The function of the FIXCO5 is to take over responsibility from a host computer for fixed disc control.

The connection to the host computer is made via the Small Computer System Interface (SCSI bus), see Figure 1.1. Up to eight bus devices, such as disc controllers, tape controllers and host computers, can be connected to the SCSI bus.

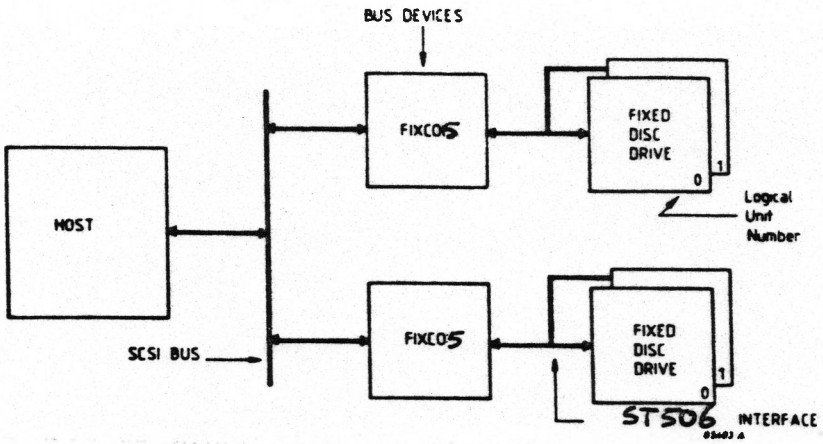


Figure 1.1 FIXCO5 CONFIGURATION

Communication between the FIXCO5 and the drive is done via the standard ST506 interface.

The FIXC05 design is based on the 8031 microprocessor and the 7261 hard-disc controller (HDC). When the host has work to be done, it first sends a command string of 6 bytes to the microprocessor.
In case of a read command, the microprocessor programs the HDC for receiving data. Then under control of the HDC readdata is transferred from the drive to the FIXC05, where it is stored in a RAM-buffer under control of a DMA (Direct Memory Access) controller.
Datatransfer to and from the RAM Buffer from or to the Host is also controlled by the DMA Controller.

In case of a write command, the data flow is from Host to RAM Buffer, and from the RAM Buffer to the drive.

When the FIXC05 has carried out the command, it sends one "Completion Status" byte and one "Command Complete Message" byte to the Host.
The "Completion Status" byte informs the host wether the command has been carried out successfully or not. If it was carried out sucessfully, the FIXC05 has no further status bytes available. In the other case the Host will send a command "Request Sense" and then receive four status bytes from the FIXC05.
These status bytes, called "Sense Bytes", inform the host which errors occured.

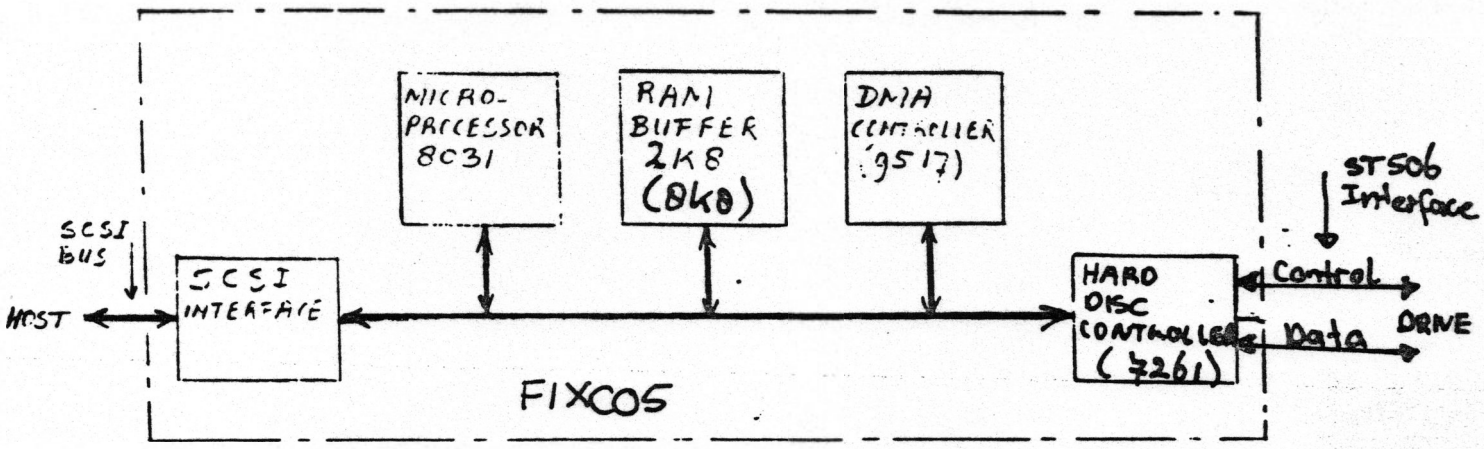


Figure 1.2 FIXC05, SIMPLIFIED BLOCKDIAGRAM

The FIXC05 consists of one Printed Circuit Board (size 5 1/4-inch), which contains five connectors; one for the interface to the host computer
one for the disk control lines
two for disk data lines
one for the DC power supply

SUMMARY OF THE RODIME DRIVE

The drive to be controlled is an 5 1/4" Winchester disc drive (RODIME 202E. or 204E).
This microprocessor controlled drive has two (202E) or four (204E) discs with a total of four or eight magnetic surfaces. (See Figure 1.3)

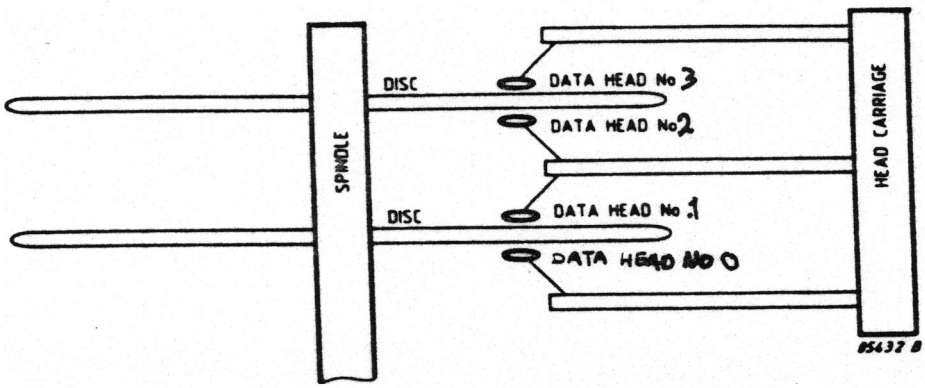


Figure 1.3 SERVO AND DATA SURFACES

The storage capacities are as follows:

- 26.66 MB unformatted for the RO 202E
- 53.33 MB unformatted for the RO 204E

The drive is soft sectored and is connected to the host system via the FIXCO5 which is responsible for formatting, MFM encode and decode, block address decode, CRC generation and verification and so on.
The drive receives and transmits MFM (Modified Frequency Modulation) data. It seeks the appropriate track in response to STEP commands across the disc control interface.

Via the Drive Select and Head Select lines the desired drive and head are selected. A signal Ready indicates the discs are up to speed and ready for writing or reading. Depending on the signal Write Gate, data can be read or written.

1.2.2 PHYSICAL CONNECTIONS BETWEEN DRIVE AND FIXCO5 (FIGURE 1.4)

The control lines may be daisy-chained, but the data lines must be individually connected to the FIXCO5

The functions of the ST506 interface signals are as follows:

- Drive Select Lines (NDS 1-4)
  Select one out of four drives. (The FIXCO5 can control up to two drives, so only NDS1 and NDS2 are used.)

- Step (NSTEP)
  This input signal is used in conjunction with Direction In to move the stepper motor. NSTEP is used to clock an internal 10 bit counter. This counter is reset prior to each seek.
  Once the first STEP pulse is received, the processor issues stepper motor phase changes until the number of changes equals the value in the counter. At this point the seek is terminated and Seek Complete is true after final step damping.

- Direction In (NDIR)
  This input line defines the direction of motion of the stepper motor. Once the first STEP of any seek has been received, the microprocessor samples this input, and internally stores the result. The input is then ignored until the next seek.

- Head Select Lines (NHS 2-0)
  Selects one of the eight heads. In the RODIME 202E there are only 4 heads.
- Write Gate (NWTGT)
  Active low during writing to the drive.

- Reduced Write Current (NRWC)
  A signal used to enable RWC. RWC is switch on (if enabled) at track 210.

- Seek Complete (NSEEKC)
  This line is driven by a S-R flipflop. STEP resets the flip-flop false. It's set after a compleet seek.

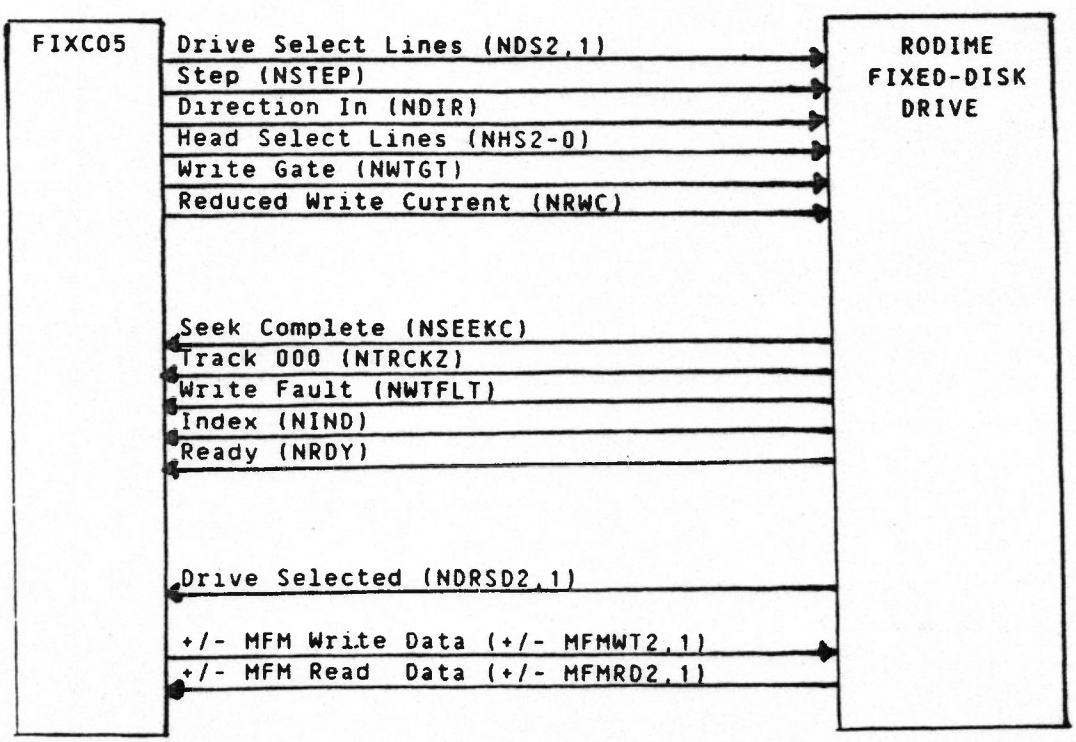


Figure 1.4

- Track 000 (NTRACKZ)
  This status line is set true when the read/write heads are positioned, with correct stepper motor phase, over track zero.

- Write Fault (NWTFLT)
  The fault conditions: Moter speed outside +/- 1% , at end of power up sequence.
  Motor speed outside +/- 10%, during normal operation.
  No index.
  Motor not up to speed.
  generate a Write Fault to the interface.

- Index (NIND)
  Indicates a fixed reference point, relative to the disk.

- Ready. (NRDY)
  Indicates that all checks and calibrations on the drive are successful.

- Drive Selected. (NDRSD2,1)
  Indicates that DRIVE SELECT signal from FIXCO5 correspond with the drive select switch setting on the RODIME, and that the drive is READY.

- +/- MFM Write Data. (+/- MFMWT 2,1)
  Two differential-driven lines which carry Write data from FIXCO5 to RODIME.

- +/- MFM Read Data. (+/- MFMWT 2,1)
  Two differential-driven lines which carry Read data from RODIME to FIXCO5

TRACK AND SECTOR FORMAT

A track is divided in a number of sectors. The number of sectors per track depends on the datasize of a sector, and will be:

32 sectors/track datafieldlength/sector: 256 bytes
17 sectors/track datafieldlength/sector: 512 bytes

Depending on Jumper 84 on the FIXC05 a datafieldlength of 256 or 512 bytes is choosen.

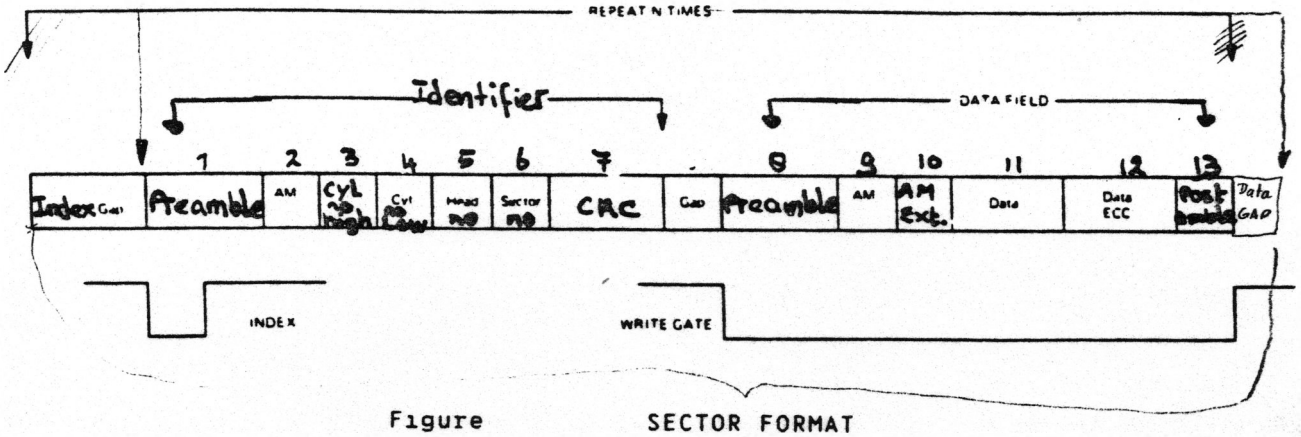


Figure SECTOR FORMAT

Name	No. of Bytes	Value (HEX)
Index Gap	16	4E
Identifier		
1. Preamble	13	00
2. Address Mark	1	A1
3. Cylinder No High	1	xx
4. Cylinder No Low	1	xx
5. Head No	1	xx
6. Sector No	1	xx
7. CRC	2	xx (1)
Identifier Gap	3	00
Datafield		
8. Preamble	13	00
9. Address Mark	1	A1
10. Address Mark Ext.	1	F8
11. Data	256/512	E5
12. ECC	4	xx (2)
13. Postamble	3	00
Data Gap	15/37	00
Track Gap	288/302	4E

35 Sect / 1 sector

Track

(1) The CRC will be generated using the polynomial $X^{16} + X^{12} + X^{5} + 1$
(2) The ECC will be generated using the polynomial $(X^{21} + 1)(X^{11} + X^{2} + 1)$

Index Gap: Allows head switching recovery, so that sequential sectors may be read without losing a complete disk revolution.
Track Gap: This gap provides a spindle speed tolerance buffer for the whole track.
Preamble: Preamble bytes are used by the PLL (Phase-Locked Loop) on the FIXC05 to synchronize the NRDRFCK with the incoming data.
Address Mark: Identifies beginning of address/data field.

The sector number written in the identifier does not necessary correspond to the physical sector location. For example it is possible to designate the sectors as shown in Figure . Skipping one or more sectors is called interleaving.

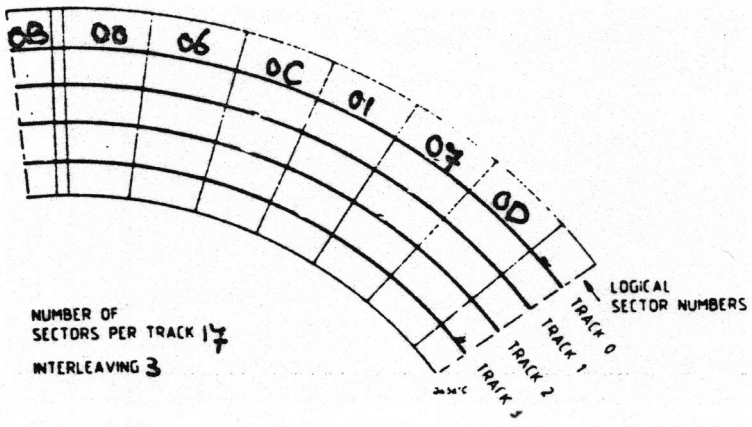


Figure: (Interleave 3)

The "Interleave" points out, that physical sector which contains the next following logical sector, relative to the actual position.
Any Interleave between zero and number of sectors/track - 1 will be valid.

1.3 SCSI BUS

Next a brief description of the SCSI bus follows. For more information refer to the bus specification: Small Computer System Interface (SCSI), ANSC X3T9.2 (American National Standard).

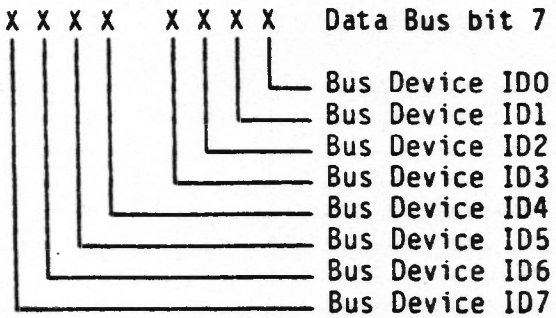
1.3.1 INTRODUCTION

The Small Computer System Interface is a local I/O Bus which can be operated at data rates up to an estimated 4 megabytes per second, depending upon circuit implementation choices. The primary objective of the interface is to provide host computers with device independence, within a class of devices. Thus, disk drives, tape drives, printers and even communication devices, of different types, can be added to the host computer(s) without requiring modifications to generic system hardware or software. Provision is made for the ready addition of non-generic features and functions.

The interface uses "logical" rather than "physical" addressing for all data structures. All data is addressed as logical blocks up to the maximum number of blocks in a device; and, each device can be interrogated to determine how many blocks it contains.
Provision is made for cable lengths up to 15 meters using differential drivers and receivers. An in-cabinet mounting using cable lengths up to six meters and single ended drivers and receivers is also available.

The interface protocol includes provision for the connection of multiple initiators (Bus Devices capable of initiating an operation) and multiple targets (Bus Devices capable of responding to a request to perform an operation). Arbitration (i.e., bus-contention logic) is built into the architecture of SCSI.
A logical priority system awards interface control to a Bus Device that wins arbitration.

Communication on the SCSI BUS is allowed between only two BUS DEVICES at any given time. There is a maximum of eight (8) BUS DEVICES. Each port is attached to a BUS DEVICE (e.g., peripheral device controller or host computer). Each BUS DEVICE has a DEVICE ID bit assigned as follows:



When two BUS DEVICES communicate on the bus, one acts as an Initiator and the other acts as a Target. The Initiator (typically a host computer) originates an operation and the Target (typically a peripheral device controller) performs the operation. A BUS DEVICE will usually have a fixed role as an Initiator or Target, but some may be able to assume either role

An Initiator may address up to eight (8) peripheral I/O devices that are connected to a Target. (e.g. eight disc units connected to a disc controller). An option allows the addressing of up to 2,048 devices per Target. Three sample system configurations are shown in Figure 1.7.

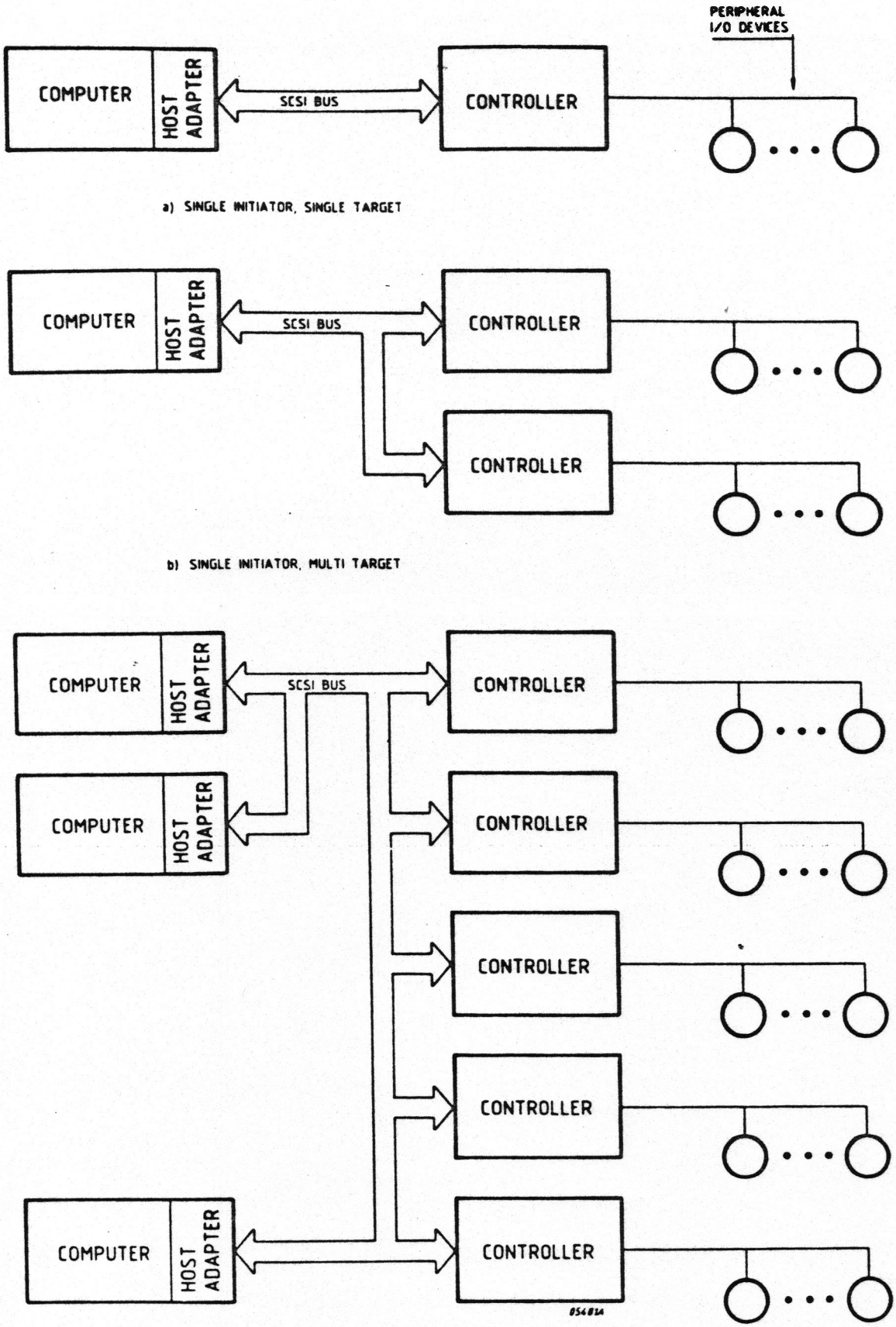


Figure 1.7 SAMPLE SCSI CONFIGURATIONS

1.3.2 SCSI PHYSICAL CONNECTIONS

The SCSI bus has nine control signals and nine data signals (including parity), which have the following functions (see Figure 1.8):

Note: N preceding a signal name means that the signal is low-active. All signals are signal-ended (unbalanced) and terminated with 220 Ohms to +5V and 330 Ohms to ground.

NRST (RESET)	An "or-tied" signal which indicates the RESET condition.
NDB(7-0), (DATA BUS)	Eight data bit signals, plus a parity bit signal which form a DATA BUS. DB(7) is the most significant bit and has the highest priority during the ARBITRATION phase. Bit number significance and priority decrease downward to DB(0). Data parity DB(P) is odd. The use of parity is a system option. In the TAPCO-Q(-2) tne parity signal is not used. Each of the eight data signals DB(7) through DB(0) is uniquely assigned as a Target or Initiator's own BUS address (i.e., BUS DEVICE ID). This BUS DEVICE ID would normally be assigned and strapped in a BUS DEVICE during system configuration. During the ARBITRATION phase, a BUS DEVICE that desires the use of the BUS asserts its assigned data bit (BUS DEVICE ID) but leaves the other data bits in the passive (non-driven) state.
NSEL (SELECT)	A signal used by an Initiator to select a Target or by a Target to reselect an Initiator.
NBUSY (BUSY)	An "or-tied" signal which indicates that the bus is being used.
NC/D (CONTROL/DATA)	A signal driven by a Target; it indicates whether CONTROL or DATA information is on the data bus. True indicates CONTROL.
NI/O (INPUT/OUTPUT)	A signal driven by a Target which controls the direction of data movement on the data bus with respect to an initiator. True indicates INPUT to the Initiator.
NREQ (REQUEST)	A signal driven by a Target to indicate a request for a REQ/ACK data transfer handshake.
NACK (ACKNOWLEDGE)	A signal driven by an Initiator to indicate an acknowledgement for a REQ/ACK data transfer handshake.

NMSG (MESSAGE) A signal driven by a Target during the MESSAGE phase.

NATN (ATTENTION) A signal driven by an initiator to indicate the ATTENTION condition.

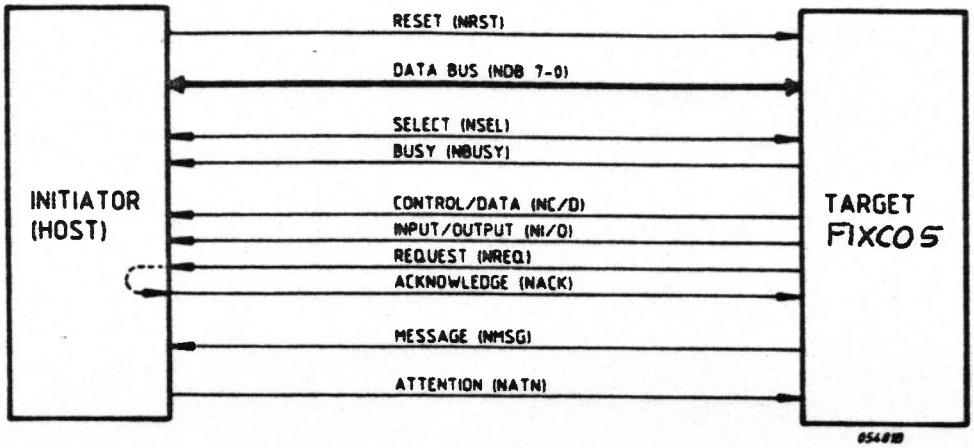


Figure 1.8 SCSI PHYSICAL CONNECTIONS

1.3.3 SCSI BUS PHASES

The SCSI bus has a number of operational phases, which are used in a prescribed sequence. There are two types of phase sequences:

- a phase sequence in systems with no arbitration;
- a phase sequence in systems with arbritration.

In the FIXCOS both phase sequences are possible. The desired phase sequence can be chosen by a strap.

NON-ARBITRATING SYSTEMS (Figure 1.9)

For complete execution of a command, e.g. a read or write command, the typical phase sequencing "with no arbitration" is as follows:

1. Bus Free phase.
2. Selection phase: the initator (host) connects a certain target (controller) to it.
3. Command phase: the initiator sends a string of 6 command bytes to the target.
4. Data phase: read or write data is transferred.
5. Status phase: one "Completion" status byte to the initiator.
6. Message phase: one "Command Complete" message byte to the initiator.
7. Bus Free phase.

The Command, Data, Status and Message phases are called Information Transfer phases.

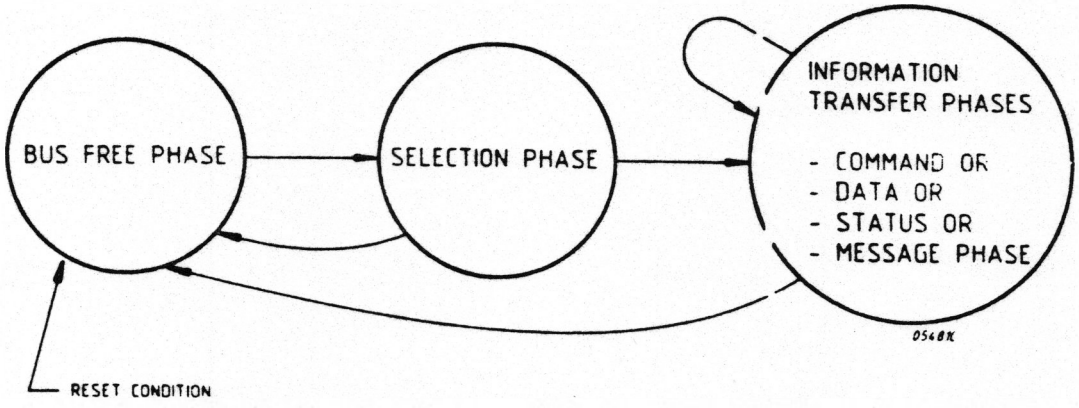


Figure 1.9 PHASE SEQUENCING IN NON-ARBITRATING SYSTEMS

ARBITRATING SYSTEMS (Figure 1.10)

For complete execution of a command, e.g. a read or write command, the typical phase sequencing "with arbitration" is as follows:

1. Bus Free phase.
2. Arbitration phase: the initiator (host) tries to gain control of the bus.
3. Selection phase: the initiator connects a certain target (controller) to it.
4. Command phase: the initator sends a string of 6 command bytes to the target.
5. Bus Free phase.

6. Arbitration phase: the target tries to gain control of the bus.
7. Reselection phase: the target connects the initiator to it.
8. Data phase: read or write data is transferred.
9. Bus Free phase.

10. Steps 6 to 9 repeated as many times a necessary.

11. Arbitration phase: the target tries to gain control of the bus.
12. Reselection phase: the target connects the initiator to it.
13. Status phase: one "Command" status byte to the initiator.
14. Message phase: one "Command Complete" message byte to the initiator.
15. Bus Free phase.

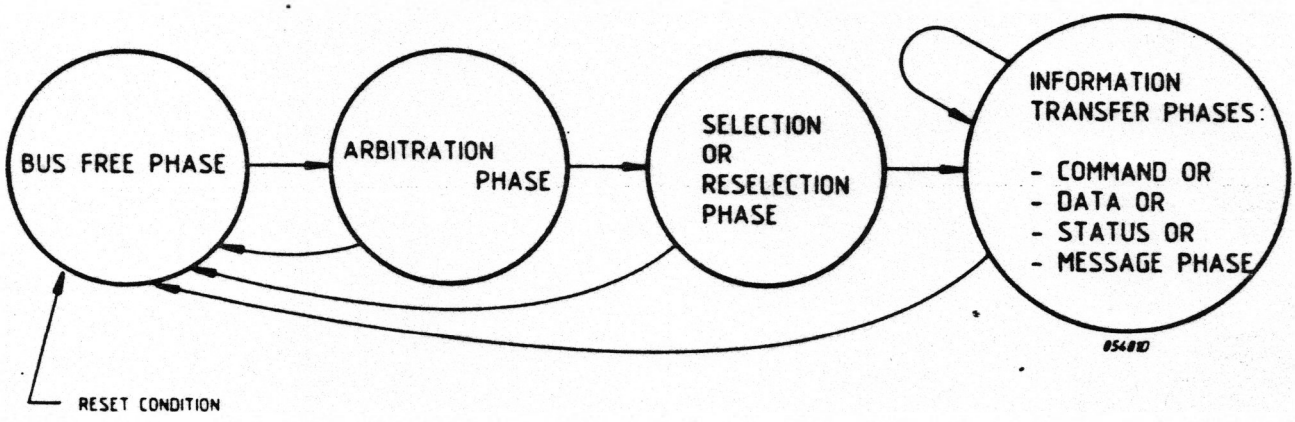


Figure 1.10 PHASE SEQUENCING IN ARBITRATING SYSTEMS

- The COMMAND, DATA, STATUS and MESSAGE phases can all be grouped together as the INFORMTION TRANSFER phases because they are all used to transfer data or control information via the DATA BUS. The actual contents of the information is beyond the scope of this section.

The NC/D, NI/O and NMSG signals are used to distinguish between the different INFORMATION TRANSFER phases. See Table 1.4. The Target drives these three signals and therefore controls all changes from one phase to another. The INITIATOR can request a MESSAGE OUT phase by asserting NATN, while the Target can cause the BUS FREE phase by releasing NMSG, NC/D, NI/O and NBSY.

SIGNAL			PHASE NAME	DIRECTION OF TRANSFER	COMMENT
MSG	C/D	I/O			
0	0	0	DATA OUT PHASE	INIT to TARGET	) DATA
0	0	1	DATA IN PHASE	INIT from TARGET	) PHASES
0	1	0	COMMAND PHASE	INIT to TARGET	
0	1	1	STATUS PHASE	INIT from TARGET	
1	0	0	Not Used		
1	0	1	Not Used		
1	1	0	MESSAGE OUT PHASE	INIT to TARGET	) MESSAGE
1	1	1	MESSAGE IN PHASE	INIT from TARGET	) PHASES

Notes: 0 = False, 1 = True
INIT = Initiator

Table 1.4 INFORMATION TRANSFER PHASES (SCSI)

ALL SYSTEMS

There are no restrictions on the sequencing between Information Transfer phases (Command, Data, Status and Message phases). A phase may even follow itself (e.g., a Data phase may be followed by another Data phase).

PHASE DESCRIPTIONS:

- The BUS FREE phase is used to indicate that no BUS DEVICE is actively using the bus and that the bus is available for subsequent users. All bus signals are released.
- The ARBITRATION phase allows one BUS DEVICE to gain control of the bus so that the device can assume the role of an Initiator or Target.

  Note: Implementation of the ARBITRATION phase is a system option. Systems which do not implement this option can have only one Initiator. The ARBITRATION phase is required for systems which use the RESELECTION phase.
  The procedure for a BUS DEVICE to obtain control of the bus is as follows:

  1. Wait till BUS FREE phase occurs (all signals released).
  2. Assert NBSY and own Bus Device ID bit on the Data Bus.
  3. Examine the Data Bus. Any higher priority Bus Device also arbitrating?.
     . YES. Arbitration lost; return to step 1.
     . NO. Arbitration won; assert NSEL.

- The SELECTION phase allows an Initiator to select a Target for the purpose of initiating some Target function(s), (e.g. read or write data):

  1. The Initiator (host) asserts the desired Target's ID bit on the Data Bus.
  2. The Initiator asserts NSEL (already done in Arbitration systems).
  3. The Target asserts NBSY (already done in Arbitration systems).
  4. The Initiator releases NSEL and its ID bit on the Data Bus.

  Note: During the SELECTION phase the I/O signal shall be deasserted so that this phase can be distinguished from the RESELECTION phase.

- RESELECTION is an optional phase which allows a TARGET to reconnect to an INITIATOR for the purpose of continuing some operation that was previously started by the INITIATOR but was suspended by the TARGET (i.e., the TARGET disconnected by allowing a BUS FREE phase to occur before the operation was complete). RESELECTION can only be used in systems that have ARBITRATION phase implemented:

  1. Target (controller) asserts NI/O (to distinguish from SELECTION).
  2. Target asserts the Initiator's (host's) ID bit and own ID bit on the Data Bus.
  3. Target releases NBSY.
  4. Initiator detects: its ID bit on the bus, NSEL = true, NI/O = true, NBSY = false.
  5. Initiator asserts NBSY.
  6. Target also asserts NBSY.
  7. Target releases NSEL.

1.3.4 SCSI TIMING (FIGURE 1.11 and 1.12)

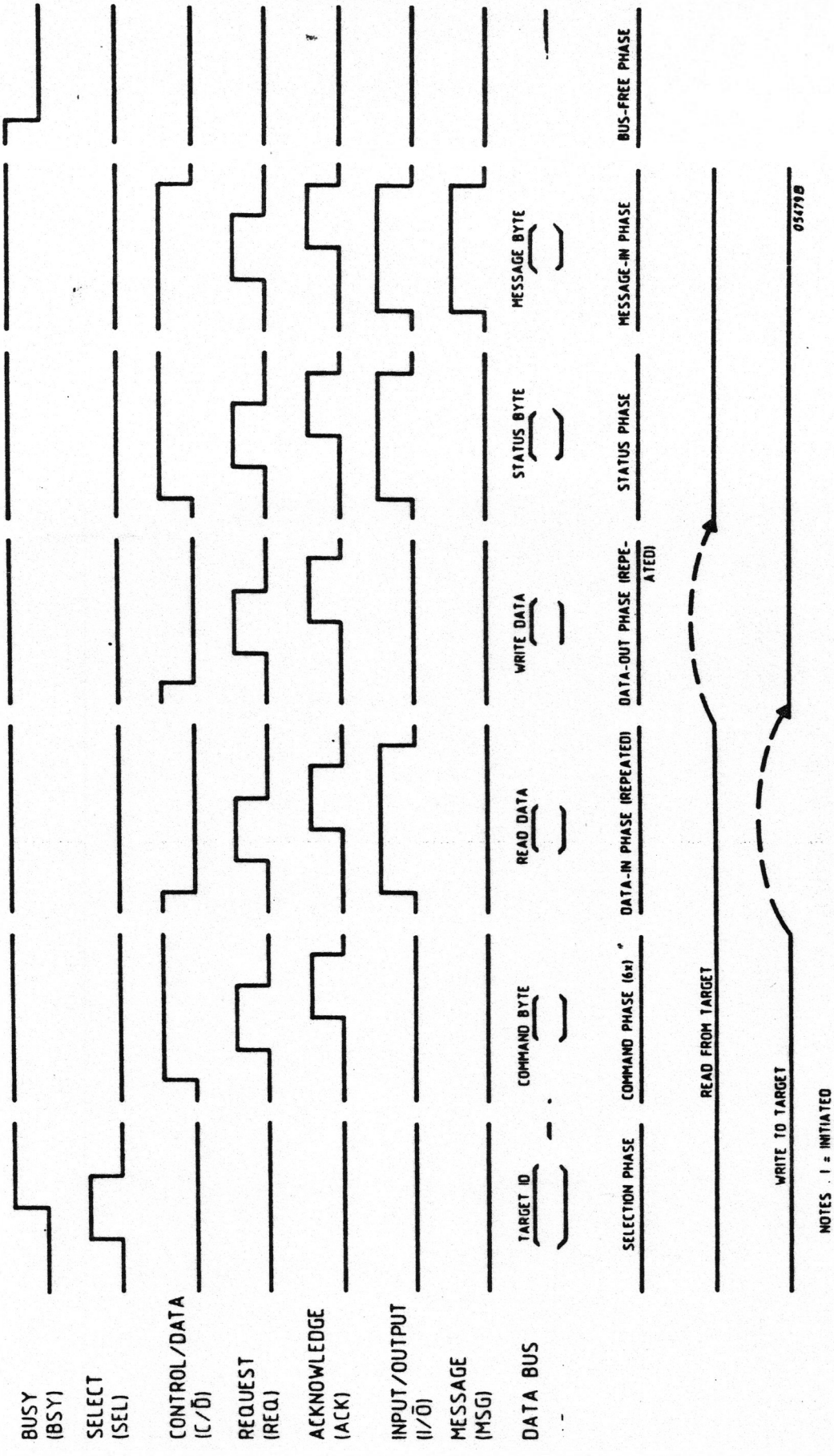
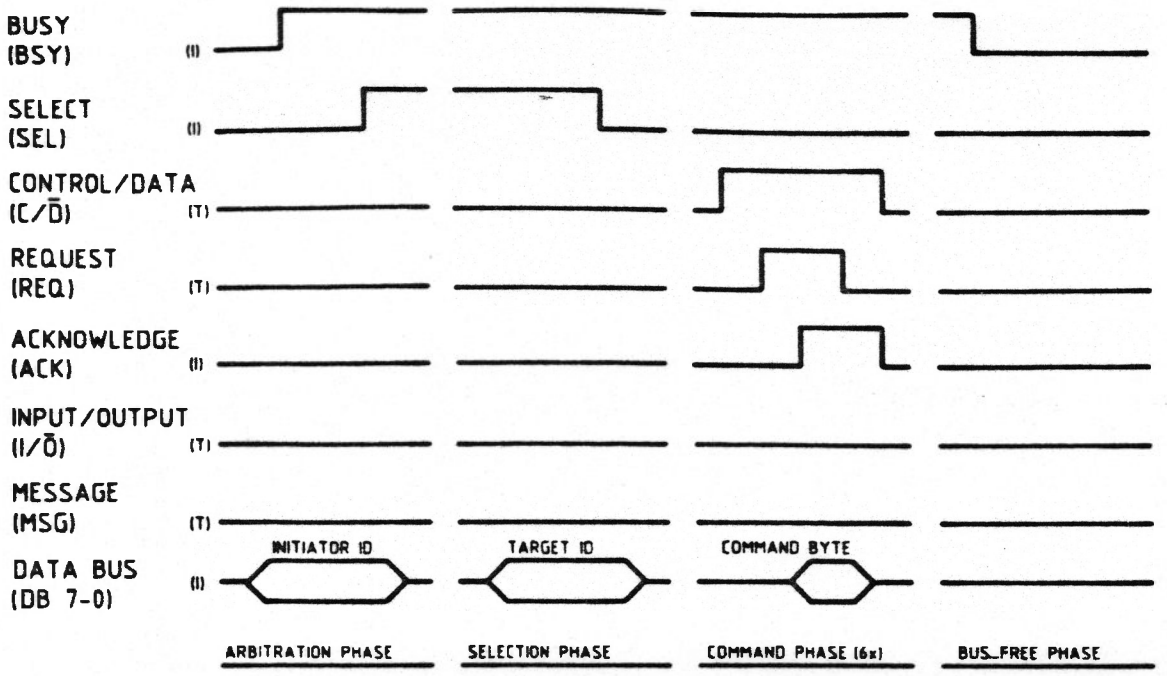
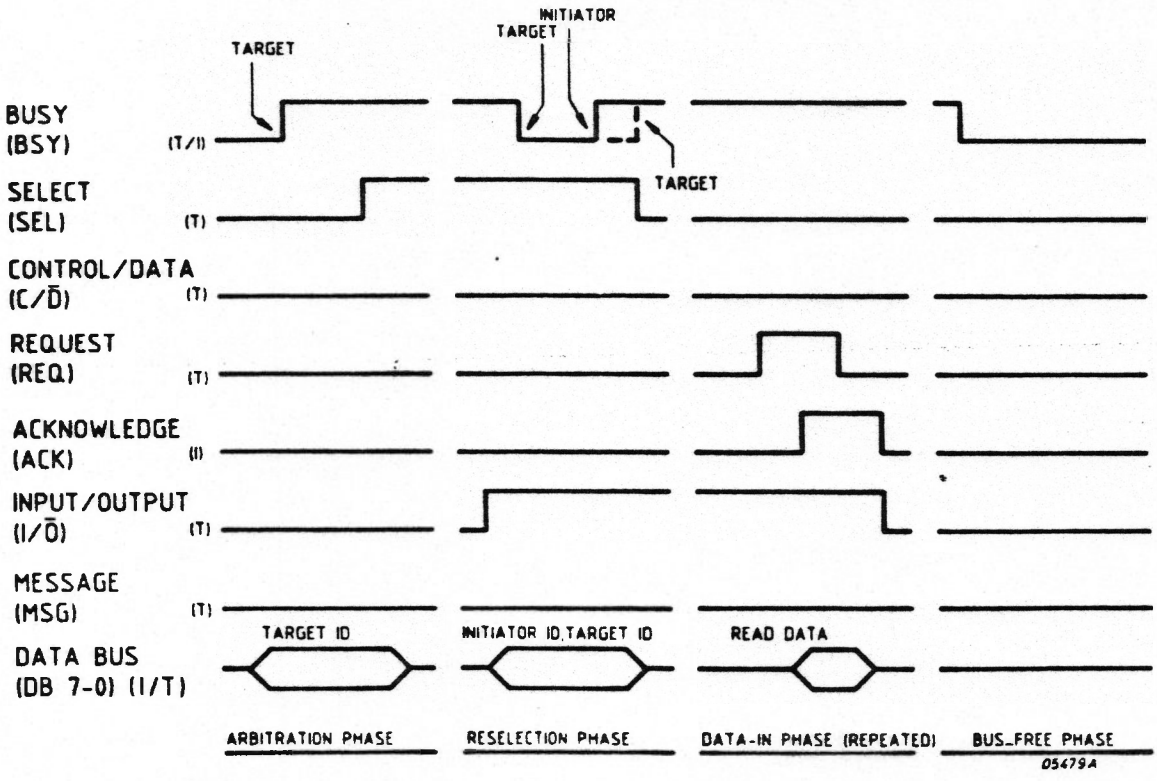


Figure 1.11 SCSI TIMING IN NON-ARBITRATING SYSTEMS



BUS TRANSACTION STARTED BY INITIATOR (COMMAND TRANSFER)



BUS TRANSACTION STARTED BY TARGET (READ DATA TRANSFER)

NOTES I = INITIATOR
T = TARGET

Figure 1.12 SCSI TIMING IN ARBITRATING SYSTEMS

1.3.5 SCSI BUS CONDITIONS

The bus has two asynchronous conditions:

- ATTENTION Condition.

- RESET Condition

These conditions cause certain BUS DEVICE actions and can alter the bus phase sequence.

ATTENTION CONDITION

The ATTENTION Condition allows an initiator to inform a Target that the initiator has a Message ready. The Target may get this message at its convenience by performing a MESSAGE OUT phase.

The Initiator creates the ATTENTION Condition by asserting NATN at any time except during the ARBITRATION or BUS FREE phases.

The Target may respond with the MESSAGE OUT phase.

The Initiator shall keep NATN asserted if more than one byte is to be transferred.

The Initiator may deassert the NATN signal at any time except is shall not deassert the NATN signal while the NACK signal is asserted during a MESSAGE OUT phase.

RESET CONDITION

The RESET Condition is used to immediately clear all BUS DEVICES from the bus. This condition shall take precedence over all other phases and conditions. Any BUS DEVICE may create the RESET condition by asserting NRST for a minimum of a Reset Hold Time. During the RESET condition, no bus signal except NRST is guaranteed to be valid.

All BUS DEVICES shall release all bus signals (except NRST) whithin a Bus Clear Delay of the transition of NRST to True. The BUS FREE phase always immediately follows the RESET condition.

1.3.6 SCSI COMMAND, STATUS AND MESSAGE FORMATS

A number of fourteen different commands are implemented in the FIXC05, these being:

- Test Unit Ready
- Rezero Unit
- Request Sense
- Format Unit
- Read
- Write
- Seek
- Initialize Characteristics
- Read Error Burst Length
- Test Controller RAM
- Send FW Revision
- Test Drive
- Test Controller
- Read for Test

Note: For a complete description of the FIXC05 command set, refer to the system Hardware Software Interface (HSI) description.

Any FIXC05 operation is started by a six-byte Command Descriptor Block (CDB).

The general format is as follows:

	BITS 7	6	5	4	3	2	1	0
Byte 0	Command Group			Opcode				
Byte 1	Logical Unit = 0							
Byte 2				No. of Blocks (MSB)				
Byte 3	No. of Blocks							
Byte 4	No. of Blocks (LSB)							
Byte 5	Control Field							

MSB = Most Significant Bits
LSB = Least Significant Bits

After execution, the FIXC05 provides the "Completion Status" byte and the "Command Complete Message" byte:

	BITS 7	6	5	4	3	2	1	0
Status Byte 0	0	0	d	0	0	0	e	0

	7	6	5	4	3	2	1	0
Message Byte 0	0	0	0	0	0	0	0	0

e = Error. Host must answer by the "Request Sense" command.
d = Logical unit number, the status information belongs to.

3LOCK DIAGRAM

RESET LOGIC

The Reset Logic resets the Microprocessor and some other circuits when the SCSI Reset Line (NRST) is active low, or when power comes up.

OSCILLATOR

The Oscillator drives the microprocessor with 10 MHz. It also provides other circuits with clocksignals of 10 MHz devided by 2 or 3.

MICROPROCESSOR

The microprocessor has the overall controll of the FIXC05.
When the host has work to be done, the "FIXC05 Selection" interrupts the processor via NINTSA. During the Command Phase the microprocessor stores the Commmand Descriptor Block (CDB) from the host in its internal RAM.

During the Data Phase the microprocessor writes a certain command string in the DMA Controller and the Hard Disc Controller (HDC). Now we can read from, or write to the fixed disc.
During a read command the DMA Control Logic transfers data blocks from the HDC to the RAM Buffer, and from the RAM Buffer to the SCSI Bus. Each time when a programmed number of bytes (block) has been transferred, the microprocessor is interrupted by "End of Process" (EOP) signal from the DMA Control Logic; signal NEOPS for the SCSI channel, and NEPN for the (NEC) (HDC) channel.
In case of a write command, the microprocessor programs the DMA Control Logic to transfer data in opposite direction.

If Arbitration and Reselection are used, the SCSI bus can be released temporary when no data is being transferred.
Signal NINTSA then interrupts the microprocesor at the end of the Arbitration Phase and at the end of the Reselection Phase.
The microprocessor is also interrupted with NINTNC by the HDC after termination of a disc command.

ADDRESS LATCH 1 AND 2

The microprocessor port 0 is a multiplexed address and data bus. Therefore, the low-order byte of an address must be stored temporary in a latch. Anytime when the microprocessor does an external memory access or a memory mapped I/O, strobe ALE (Address Latch Enable) automatically loads the low-order address byte in Address Latch 1 and 2. Address Latch 1 stores the the low-order address byte for the Program Store and the Address Decoder. Address Latch 2 stores the low-order address byte when the microprocessor accesses the RAM Buffer, and it stores four address bits when the microprocessor accesses the DMA Controller. (The DMA Controller is a programmable chip, which is the main component of the DMA Control Logic

PROGRAM STORE

The Program Store is an 8K8 Read-Only Memory (ROM), which contains the program to be carried out by the microprocessor.

ADDRESS DECODER

The Address Decoder selects registers, drivers etc. for microprocessor input and output transfers.

DATA DRIVER

The Data Driver allows the microprocessor to access the DMA bus (DMAB0-7) for the following purposes:

- To write data into and to read data from the RAM Buffer for test purposes.
- To read data (command bytes) from the SCSI Data Input or to write data (status or message bytes) into the SCSI Data Output.
- To write data (command bytes) into the HDC or to read data (status bytes) from the HDC.

DMAC DATA/ADDRESS DRIVER

The DMA Controller (DMAC) Data/Address Driver allows the microprocessor:

- To write control data into and to read status data from the DMA Controller. The DMA Controller is a programmable chip, which forms the main component of the DMA Control Logic.
- To write a high-order address byte in Address Latch 3, after which the microprocessor can access the RAM Buffer.

HARDWARE CONTROLPORT

The Hardware Controlport is a register which controls:
- The DMA Control Logic
- Switches on or off the error indicator LED
- Enables control signals from HDC to Fixed drive.

RAM BUFFER

The RAM Buffer stores temporary data to be written onto disc or data to be read from disc on a First-In First-Out (FIFO) basis. The buffer capacity used is 2K bytes. (The hardware allows a capacity of 8K bytes).
2K equals to 4 data blocks of 512 bytes.
During normal operation, the DMA control logic transfers data directly from the SCSI interface to the RAM Buffer, and from the RAM Buffer to the HDC or vice versa. The microprocessor will access the RAM Buffer for test purposes only.

DMA CONTROL LOGIC

The main component of the DMA Control Logic is the DMA Controller. The DMA controller is a chip, which can be programmed by the microprocessor to transfer blocks of data to and from the RAM Buffer. Three channels of the DMA Controller are used.

- Channel 0 to transfer data between the HDC and the RAM Buffer.
- Channel 2 and 3 for data transfer between the SCSI interface and the RAM Buffer.

When the microprocessor wants to have transferred a block of data, it simply sends to the DMA Controller:
- The DMA channel number
- Whether it is a memory read or write operation
- The RAM Buffer base address from which or to which the first data byte is to be transferred.
- The number of bytes to be transferred.

ADDRESS LATCH 3

The DMA Controller is designed to be used in conjunction with an external 8-bit address latch. Anytime when necessary, the DMA Controller automatically loads the high-order byte of the address in Address Latch 3 by issueing strobe ADSTB (Address Strobe). Address Latch 3 can also be loaded by the microprocessor, when it wants to access the memory for test purposes.

DMA REQUEST LOGIC

The DMA Request Logic sets up the DMA requests (NDRQ 0, 2 or 3) for the DMA Cntroller. For each byte to be transferred, one request is issued.

SCSI DATA INPUT (LATCH)

Via the SCSI Data Input (latch) the FIXC05 takes from the SCSI Bus:
- Command bytes
- Data bytes to be written onto tape

SCSI DATA OUTPUT (LATCH)

Via the SCSI Data Output (latch) the FIXC05 puts on the SCSI bus:
- Status bytes
- Message bytes
- Data bytes read from from tape

FIXC05 SELECTION

The "FIXC05 Selection" block controls the interface to the SCSI bus during the Selection Phase, Arbitration Phase and Reselection Phase.

SCSI HANDSHAKE LOGIC

The SCSI Handshake Logic controls the data transfer to and from the SCSI bus during the Command Phase, Data Phase, Status Phase and Message Phase (Information Transfer Phases).

SCSI CONTROL INPUT

Via the SCSI Control Input the microprocessor can read:

- The status of the straps BR2, BR3 and BR5. By means of these straps you can choose the bus address (0-7) of the FIXC05. The microprocessor has to know the bus address when the FIXC05 is used in an "Arbitration System".

- The state of strap BR6. By means of this strap you can select whether the FIXC05 is used in a "Non -Arbitration System" or an "Arbitration System".

- The Request Internal (REQIT) signal, which indicates the SCSI Request Flip-Flop (part of SCSI Handshake Logic) is set.

- The SCSI signal Acknowledge (NACK).

- The SCSI signal Attention (NATN).

SCSI CONTROL OUTPUT

Via the SCSI Control Output (latch) the microprocessor can set the SCSI Control lines: Busy (NBSY), Control/Data (NCD), Input/Output (NIO) and Message (NMSG). The other bits are used to control the "FIXC05 Selection" and the "DMA Request Logic".

HDC INTERFACE CIRCUITS

MFM DATA RECEIVER

The differential signals MFMRD + and - are translated into the signal READDT.

DATA SEPARATOR

READDT is a composite signal of both data and clock pulses. After locking on to the frequency of READDT, READDT is separated into synchronized data (RDAT) and the clock signal (NRDRFCK).

HARD DISC CONTROLLER

The HDC provides all control signals for interfacing the HDC with a Seagate floppy-like drive.
By using a DMA controller, the microprocessor needs only to load a few command bytes into the HDC and all data transfers (read,write,format) are done by the HDC and the DMA controller.

The HDC provides:
- Serial to parallel and parallel to serial conversion
- CRC and ECC generation and checking
- MFM data decoding and encoding
- Write precompensation
- Address mark detection and generation
- ID verification

An eight byte FIFO is used for loading command parameters, and obtaining command results.
It is also used for buffering data during DMA read/write operations.

PRE-COMPENSATION

Spacing between the data bits written to disc in MFM mode can vary between 200 and 600 nS (5MHz and 1 2/3 MHz). The heads, which are inductive circuits, respond differently at different frequencies. The bit pattern therefore, affects read timing with some bits being read early and others late, depending on the bit pattern.

Write pre-compensation is simply a method of writing early or late those bits which without WP would be read or early respectively. Thus the read error is corrected in advance.

Depending on the bit pattern of the Write Data, the FDC sets a special code on the lines PCL (Precomp Late) and PCE (Precomp Early) for each write data bit. Depending on the data on the lines PCL, PCE and PRE10 the Writedata is modified.

MFM-DATA TRANSMITTER

In this circuit WRITEDT is transelated in two differential signals, MFMWT+ and MFMWT-.

20.48 FIXCOS

SECTION 20.48.1 INTERCONNECTIONS FIXCOS

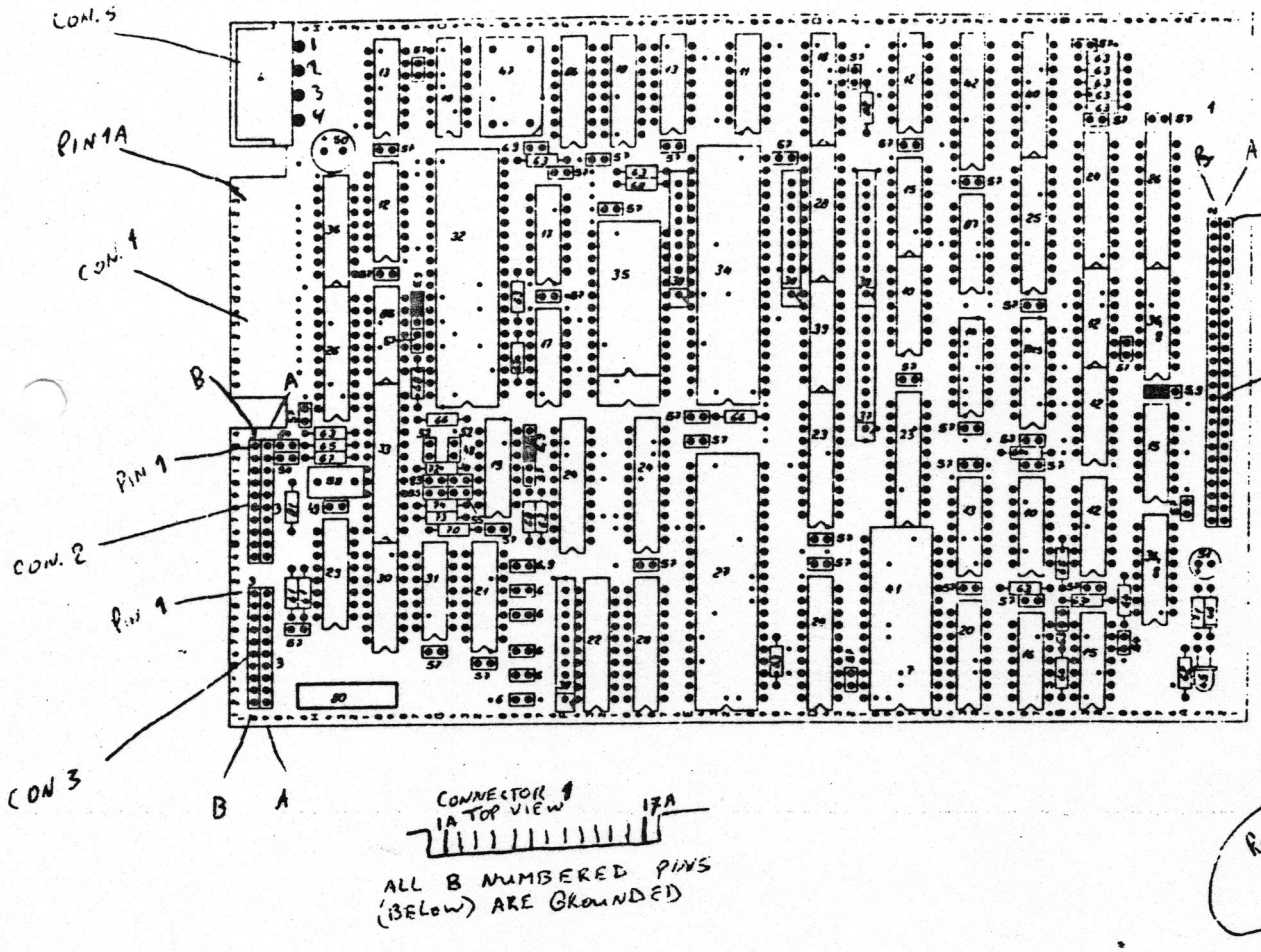
20.48.2 STRAP SETTING FIXCOS

20.48.3 MODIFICATION HISTORY FIXCOS

20.48 FIXCOS

20.48.1 INTERCONNECTIONS FIXCOS

0557 6 A



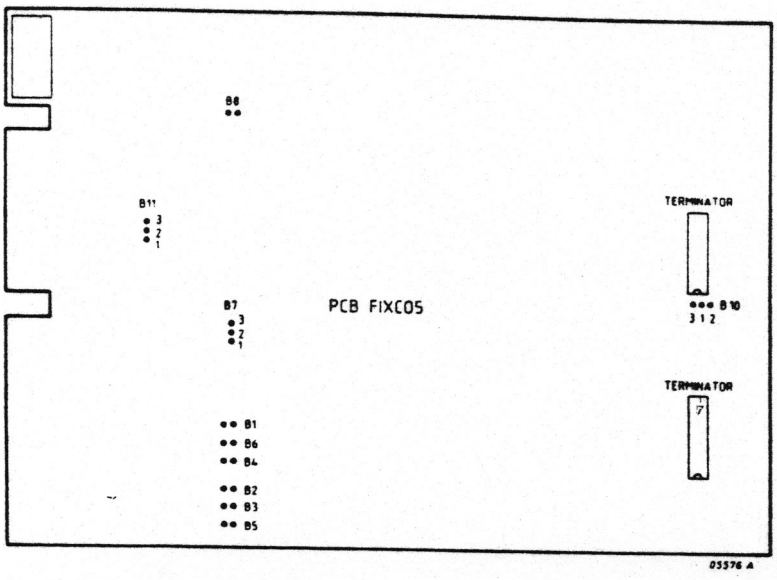
Connector 2 (1ST FXD)

	a	b
1	0V	NDRSDI
2	0V	
3	0V	
4	0V	
5		
6	0V	0V
7	MFMWT1-	MFMWT1+
8	0V	0V
9	MFMRDI-	MFMRDI+
10	DUMMY	0V

Connector 3 (2nd FXD)

	a	b
1	0V	NDRSD2
2	0V	
3	0V	
4	0V	
5		
6	0V	0V
7	MFMWT2-	MFMWT2+
8	0V	0V
9	MFMRD2-	MFMRD2+
10	DUMMY	0V

20.48.2 STRAP SETTING FIXCOS



STRAP Nr.	FUNCTION		STRAP 1-2	STRAP 2-3
B1	Microprocessor :			
	- internal memory		N	-
	- external memory	(default)	Y	-
B2	Refer to next Table			
B3	Refer to next Table			
B4	Datafield 512 bytes	(default)	Y	-
	Datafield 256 bytes		N	-
B5	Refer to next Table			
B6	No arbitration and reselection on SCSI-bus	(default)	Y	-
	Arbitration and reselection on SCSI-bus		N	-
			1-2	1-3
B7	2K8 RAM (4 blocks of 512 bytes)	(default)	Y	N
	8K8 RAM (4 blocks of 512 bytes)		N	Y
B8	Test Strap (enable clock µP)	(default)	Y	-
B10	Power Terminator			
	- from Fixcos	(default)	N	Y
	- from SCSI-bus		Y	N
			1-2	2-3
B11	New Version 7261		Y	N
	Current Version 7261	(default)	N	Y

Controller Select

	B2	B3	B5
Controller Select 0	Y	Y	Y
Controller Select 1	Y	Y	N
Controller Select 2	Y	N	Y
Controller Select 3	Y	N	N
Controller Select 4	N	Y	Y
Controller Select 5	N	Y	N
Controller Select 6	N	N	Y
Controller Select 7 (default)	N	N	N

= 80 H Swi Bus

2048.3 MODIFICATION HISTORY

FIXCOS 5112 291 8071*

LEVEL *	PAL E7B6	PAL E6C1	ROM C8D3	ROM A2C5	SI-NR
2	800221	800341	800311	00332	

Connector 3 (FXD Drive(s))

	a	b
1	NRWC	0V
2	NHS2	0V
3	NWTGT	0V
4	NSEEKC	0V
5	NTRCKZ	0V
6	NWTFLT	0V
7	NHS0	0V
8		0V
9	NHS1	0V
10	NIND	0V
11	NRDY	0V
12	NSIEP	0V
13	NDS1	0V
14	NDS2	0V
15		0V
16		0V
17	NDIR	0V

KEY

Connector 4 (SCSI-bus)

	a	b	
1	NDB0	0V	1
2	NDB1	0V	2
3	NDB2	0V	3
4	NDB3	0V	4
5	NDB4	0V	5
6	NDB5	0V	6
7	NDB6	0V	7
8	NDB7	0V	8
9	NDBP	0V	9
10	0V	0V	10
11	0V	0V	11
12	0V	0V	12
13	TERMP		13
14	0V	0V	14
15	0V	0V	15
16	NATN	0V	16
17	0V	0V	17
18	NBSY	0V	18
19	NACK	0V	19
20	NRST	0V	20
21	NMSG	0V	21
22	NSEL	0V	22
23	NCD	0V	23
24	NREQ	0V	24
25	NIO	(Dummy)	25

Connector 5 (Back panel)

1	NC
2	NC
3	0V
4	+5V

Menge	Einheit	Benennung	Norm	Codenummer	UN-D 578	Pos	IND
1	13	PRINT FIXC05/02		5112 212 08903		1	
1	13	STIFTLEISTE 50POL		2422 025 03694		2	
4	13	STIFTLEISTE 10POL		5112 211 03261		3	
1	13	STIFTLEISTE 4POL		2422 025 04227		4	
3	13	STIFTLEISTE 3POL		5112 211 03271		5	
87	13	STIFTLEISTE 2POL		5112 211 06041		6	
1	13	IC-FASSUNG 28POL		2422 549 13644		7	
2	13	IC-FASSUNG 16POL		2422 549 13656		8	
5	13	BUCHSENSTECKER 2POL	SOW-37-871-30	2422 024 88003		9	
3	13	IC-SCHALTUNG SN74LS08N	SOA-42-112-00	9332 735 20772		10	
1	13	IC-SCHALTUNG N74S08N	SOA-42-112-00	9332 876 90602		11	
5	13	IC-SCHALTUNG SN74LS14N	SOA-42-245-00	9332 759 70772		12	
3	13	IC-SCHALTUNG N74LS32N	SOA-42-112-00	9332 870 90602		13	
1	13	IC-SCHALTUNG N74S32N	SOA-42-112-00	9332 877 20602		14	
3	13	IC-SCHALTUNG N74S38N	SOA-42-112-00	9332 920 50602		15	
1	13	IC-SCHALTUNG SN74LS74AN	SOA-42-111-00	9334 451 50682		16	
2	13	IC-SCHALTUNG 74F74PC	SOA-42-111-00	9336 154 00682		17	
2	13	IC-SCHALTUNG N74LS112N	SOA-42-111-00	9332 873 00602		18	
1	13	IC-SCHALTUNG SN74LS126AN		9335 087 30682		19	
1	13	IC-SCHALTUNG SN74S138N	F/138	9332 788 30682		20	
1	13	IC-SCHALTUNG 74F151PC		9335 890 50682		21	
1	13	IC-SCHALTUNG SN74LS244N	SOA-42-212-00	9334 538 30682		22	
2	13	IC-SCHALTUNG SN74LS273N	SOA-42-111-00	9333 948 70772		23	
4	13	IC-SCHALTUNG SN74LS373N	SOA-42-142-00	9334 534 00772		24	
1	13	IC-SCHALTUNG SN74LS374N	SOA-42-111-00	9334 005 60772		25	
2	13	IC-SCHALTUNG SN74LS642-1N		9336 724 20682		26	
1	13	IC-SCHALTUNG P8031		9335 779 70682		27	

CLASS

PRINT FIXC05

1984 09. 25.

5112 291 80713

IND	KM	Datum
	2580	830520
	4745	840608
	5298	840920

NAME 3230 | Ersatz für 5112 291 80712 -3 | Blätter 18 | GR 120 | BL 1

PHILIPS DATA SYSTEMS 5900 SIEGEN 31 | Kontr. | Datum 840920 | A4

Menge	Einheit	Benennung	Norm	Codenummer	UN-D 578	Pos	IND
2	13	IC-SCHALTUNG DP8304BN	INS 8208	9334 929 40682		28	✓
1	13	IC-SCHALTUNG DS3486N	SOA-42-241-00	9335 396 70682		29	
1	13	IC-SCHALTUNG DS3487N	SOA-42-212-00	9335 615 10682		30	
1	13	IC-SCHALTUNG PE21197		9360 049 20682		31	
1	13	IC-SCHALTUNG UPD7261AD-V2		8212 221 07571		32	*
1	13	IC-SCHALTUNG DP8460-4N		9337 049 40682		33	
1	13	IC-SCHALTUNG P8237A-5	AM9517	9336 330 70682		34	✓
1	13	IC-SCHALTUNG HM6116P-4		9335 585 60682		35	✓
3	13	IC-SCHALTUNG 898-5-R220/330		2122 118 00083		36	✓
1	13	IC-SCHALTUNG ERC1179A	910R	5112 209 01651		37	✓
4	13	IC WID-NETZWERK	2443	5112 209 11541		38	✓
1	13	IC N82S123N/FIXC05S		5112 208 00311		39	
1	13	IC N82S185F/FIX8-6		5112 208 00221		40	
1	13	IC D2764-2/FIXC05S	2	5112 208 00332		41	2*
1	13	IC PAL16R8CNSHRP/FIXC05S		5112 208 00341		42	
1	13	DIODE SLED16		9332 589 00000		45	✓
1	13	DIODE 1N4446	SOA-41-210-00	9331 126 60112		46	✓*
1	13	OSZILLATOR 20MHZ		2722 171 08012		47	
1	13	KER-KO X7R/2 10N/10 50		8212 221 06961		48	✓
1	13	KER-KO X7R/2 100N/10 50		8212 221 06971		49	✓
1	13	AL-KO 100U/25	SOA-45-151-12	2222 035 86101		50	✓
1	13	EL-KO 4U7/10	SOW-45-152-32	2012 198 04478		51	✓
2	13	KER-KO N150/1B 47P/2 63	SOA-45-162-42	2222 682 34479		52	✓
2	13	EDRU-KO N750/1B 220P/2 63	SOW-45-161-42	2222 641 58221		53	✓
2	13	EDRU-KO 2R/2 560P/10 63	SOW-45-162-42	2222 630 05561		54	✓
2	13	MKT-KO 10N/20/50		2012 310 03223		55	✓
39	13	KDPU-KO 100N/20 50		2022 552 00524		57	✓*

CLASS			IND	KM	Datum
	PRINT FIXC05	5112 291 80713		2580	830520
				4745	840608
				5298	840920

NAME 3230	Ersatz für 5112 291 80712 -	Blätter 1	GR 120	BL 2
	PHILIPS DATA SYSTEMS 5900 SIEGEN 31	Kontr.	Datum 840920	A 4

Menge	Einheit	Benennung	Norm	Codenummer	UN-D 578	Pos	IND
1	13	MKT-KO 1U0/10 63		2222 371 11105		58	
2	13	ME-WID 0,4/70 100R/1	SOW-45-522-11	2322 151 51001		61	
1	13	ME-WID 0,4/70 182R/1	SOW-45-522-11	2322 151 51821		62	
14	13	ME-WID 0,4/70 221R/1	SOW-45-522-11	2322 151 52211		63	
3	13	ME-WID 0,4/70 332R/1	SOW-45-522-11	2322 151 53321		64	
2	13	ME-WID 0,4/70 562R/1	SOW-45-522-11	2322 151 55621		65	
2	13	ME-WID 0,4/70 1K0/1	SOW-45-522-11	2322 151 51002		66	
1	13	ME-WID 0,4/70 909R/1	SOW-45-522-11	2322 151 59091		67	
3	13	ME-WID 0,4/70 2K74/1	SOW-45-522-11	2322 151 52742		68	
1	13	ME-WID 0,4/70 4K75/1	SOW-45-522-11	2322 151 54752		70	
1	13	ME-WID 0,4/70 56K2/1	SOW-45-522-11	2322 151 55623		71	
1	13	ME-WID 0,4/70 200R/1	SOW-45-522-11	2322 151 52001		72	
1	13	ME-WID 0,4/70 11K/1	SOW-45-522-11	2322 151 51103		73	
1	13	ME-WID 0,4/70 2K21/1	SOW-45-522-11	2322 151 52212		74	
1	13	CCA-AUFKLEBER CCA-LABEL		5112 211 46511		80	
1	13	ME-WID 0,4/70 150R/1	SOW-45-522-11	2322 151 51501		81	
1	13	ME-WID 0,4/70 3K32/1	SOW-45-522-11	2322 151 53322		82	
1	13	KER-KO N150/1B 150P/2 63	SOA-45-162-42	2222 682 34151		83	
1	13	KER-KO K2000/2 470P/10 63	SOA-45-164-42	2222 630 18471		84	
1	13	IC-SCHALTUNG SN74LS04N	SOA-42-211-00	9332 316 00772		85	
1	13	IC-SCHALTUNG N74S175N	SOA-42-111-00	9332 879 20602		86	
1	13	IC-SCHALTUNG SN74S04N	SOA-42-211-00	9331 915 00772		87	

CLASS

PRINT FIXCOS

1984 09. 25.

5112 291 80713

IND	KM	Datum
	2580	830520
	4745	840608
	5298	840920

NAME 3230 | Ersatz für 5112 291 80712 | 3 Blätter | 1 | GR 120 | BL 3

PHILIPS DATA SYSTEMS 5900 SIEGEN 31 | Kontr. | Datum 840920 | A4

Menge	Ein-heit	Benennung	Norm	Codenummer	UN-D 578	Pos	IND
1	13	PRINT FIXCO5		5112 291 80713		1	*

CLASS			IND	KM	Datum
	PRINT FIXCO 5	5112 291 93691		4800	840619
	1984 09. 25.		01	5298	840920

NAME 3140	Ersatz für	1 Blätter	1	GR 120	BL 1	
PHILIPS DATA SYSTEMS 5900 SIEGEN 31		Kontr.	Datum 840920			A4

Menge	Einheit	Benennung	Norm	Codenummer	UN-D 578	Pos	IND
1	13	IC-SCHALTUNG D2764-2		9336 526 90682		1	

CLASS		IND	KM	Datum
	IC D2764-2/FIXC05S		4814	840625
	1984 09. 25.		5298	840920

5112 208 00332

NAME 3230	Ersatz für 5112 208 00331	1 Blätter	18 GR 120	BL 1
	PHILIPS DATA SYSTEMS 5900 SIEGEN 31	Kontr.	Datum 840920	A4

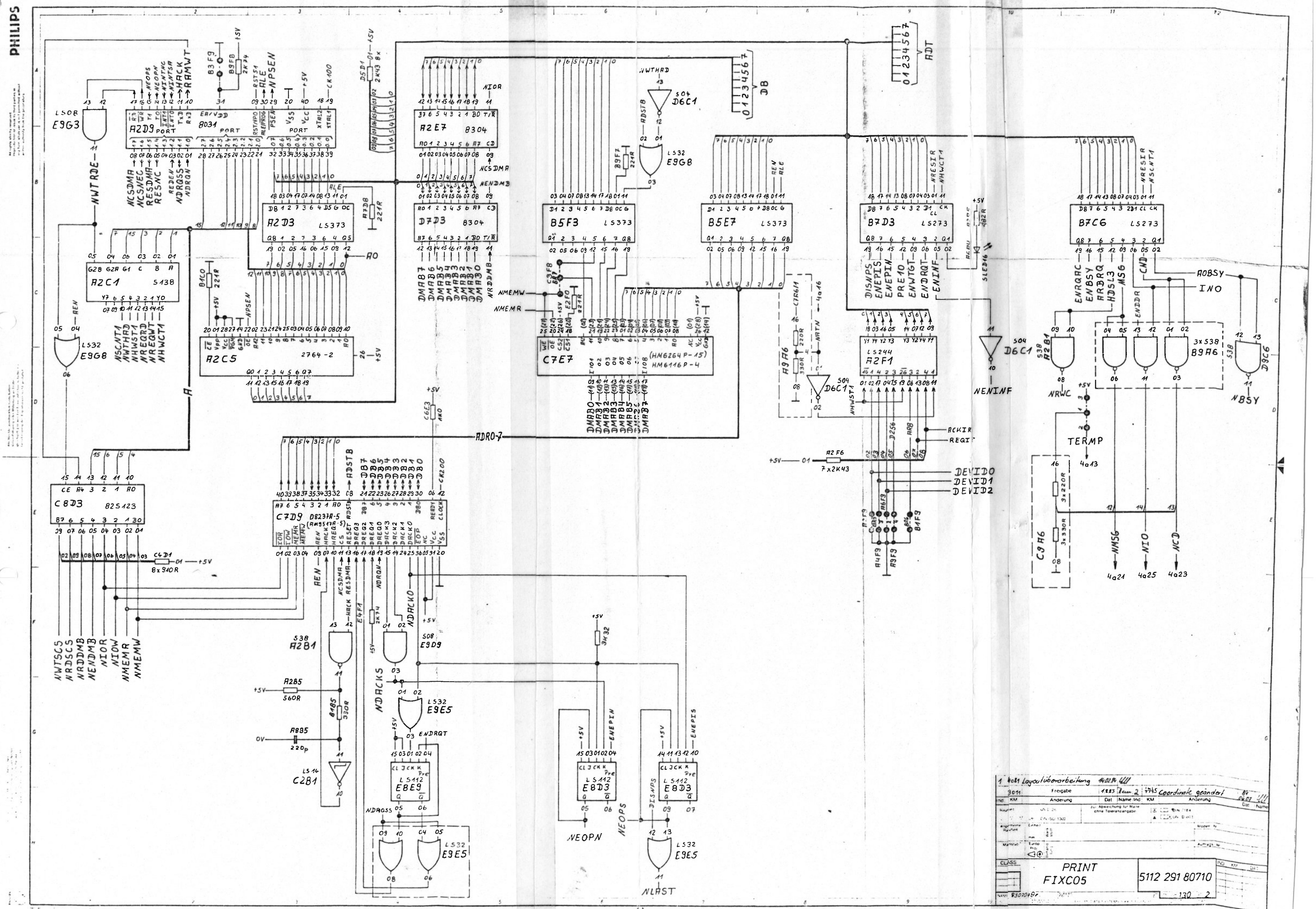
24 x
11 x
1 x
13 x
1 x
2 x
3 x
54

Lage beachten:

Pos 46 — Kathode

Pos 38, 37 — Pin 1

	52.98	Freigabe	18.9.84						
Ind.	KM	Änderung	Dat.	Name	Ind.	KM	Änderung	Dat.	Name
Rauheit		UN - D 28	zul. Abweichung für Maße ohne Toleranzangabe			DIN 7184			
		DIN ISO 1302				UN - D 603			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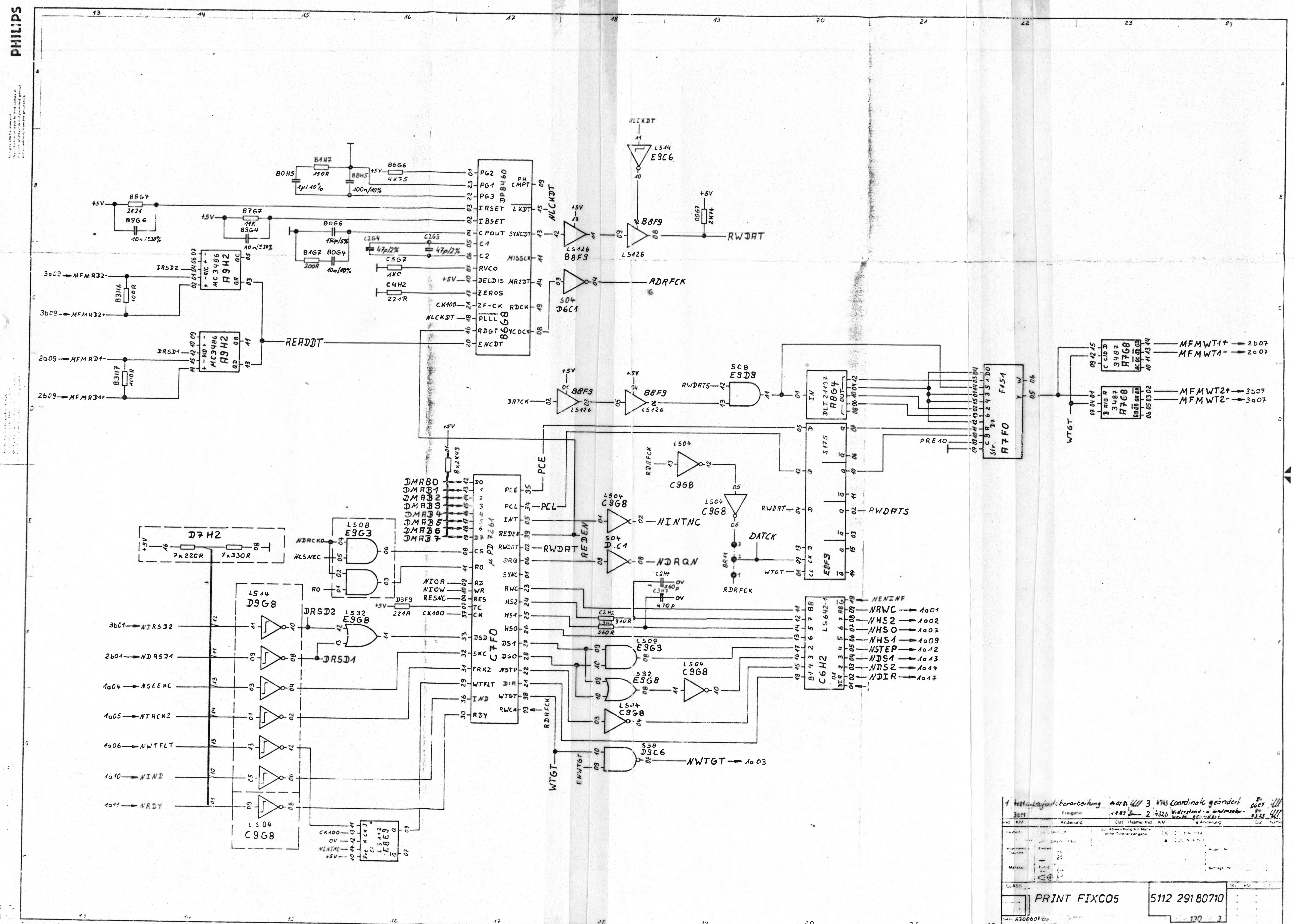
A2E7 8304
D7D3 8304
A2D3 LS373
B5F3 LS373
B5E7 LS373
B7D3 LS273
B7C6 LS273
A2C1 S138
A2C5 2764-2
C7E7 (HM6264P-15) HM6116P-4
C8D3 82S123
C7D9 D8237A-5
A2F1 LS244
E9G3
E9G8
D6C1
B9A6
D9C6
A2B1
E9D9
E9E5
C2B1
E8E9
E8D3
C9A6
A9A6
DB
ADT
ADR0-7
NWTRDE
NWTSCS
NRDSCS
NRDDMB
NENDMB
NIOR
NIOW
NMEMR
NMEMW
NEOPN
NEOPS
NLAST
NDACKS
NDACKO
NDRQSS
NENINF
NRWC
NBSY
NMSG
NIO
NCD
ROBSY
INO
TERMP
DEVID0
DEVID1
DEVID2
ACKIR
REQIT
1 4081 Layoutüberarbeitung
3011 Freigabe
2 4745 Coordinate geändert
PRINT
FIXC05
5112 291 80710
130 2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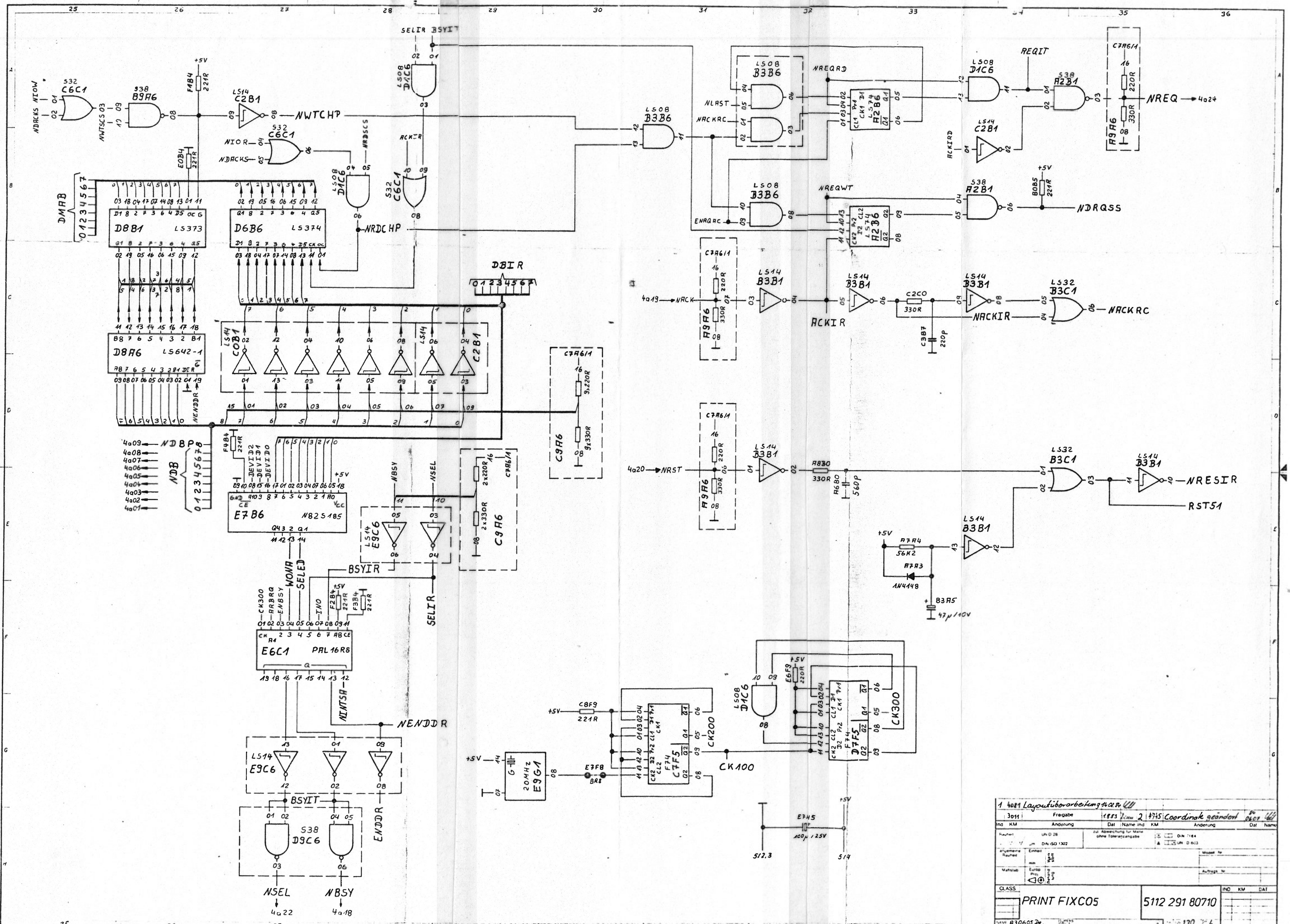
DP8460
B6G8
READDT
RWDAT
RDRFCK
MC3486
A9H2
μPD 7261
C7F0
D7H2
D9G8
C9G8
E9G3
E9G8
C6H2
E8F3
A7F0
F151
A7G8
DLI 24177
A8G4
MFMWT1+
MFMWT1-
MFMWT2+
MFMWT2-
NINTNC
NDRQN
NWTGT
NRWC
NHS2
NHS0
NHS1
NSTEP
NDS1
NDS2
NDIR
PRINT FIXCO5
5112 291 80710
130 3



PHILIPS
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NRDCHP
DMAB
DBIR
NDB
NDBP
NREQ
NDRQSS
NACKRC
NACKIR
NRESIR
RST51
NENDDR
BSYIT
BSYIR
SELIR
NSEL
NBSY
CK100
CK200
CK300
20MHz
PRINT FIXC05
5112 291 80710

S T U E C K L I S T E >5112 291 77422< SESCO

LF	MENGE	ME	CODE NUMMER	POS	BENENNUNG	NORBE	FRA
1	1	13	5112 212 07030	001	PRINT SESCO/02		27
2	1	13	2422 025 89283	002	STIFTLEISTE 96POL		17
3	2	13	5112 209 18870	003	STIFTLEISTE 49POL		23
4	1	13	5112 209 04800	004	STIFTLEISTE 33POL		17
5	1	13	5112 209 04760	005	STIFTLEISTE 15POL		17
6	2	13	5112 209 04730	006	STIFTLEISTE 5POL		25
7	1	13	5112 211 03270	007	STIFTLEISTE 3POL		17
8	2	13	5112 211 06040	008	STIFTLEISTE 2POL		17
9	2	13	2422 024 88003	009	BUCHSENSTECKER 2POL		23
10	2	13	5112 200 06890	010	ROHRNIET A2,5X0,3X9,5-MS		17
11	1	13	9332 315 90772	012	IC-SCHALTUNG SN74LS00N		17
12	3	13	9332 886 70602	013	IC-SCHALTUNG N74LS02N		17
13	4	13	9332 316 00772	014	IC-SCHALTUNG SN74LS04N		17
14	4	13	9332 735 20772	015	IC-SCHALTUNG SN74LS08N		17
15	1	13	9332 869 70602	016	IC-SCHALTUNG N74LS10N		17

FC = NEUE SEITE FB = NEUE FUNKTION FA = ENDE >

S T U E C K L I S T E >5112 291 77422<

LF	MENGE	ME	CODE NUMMER	POS	BENENNUNG	NORBE	FRA
1	1	13	9332 746 70682	017	IC-SCHALTUNG SN74LS11N		17
2	3	13	9332 759 70772	018	IC-SCHALTUNG SN74LS14N		17
3	2	13	9332 870 90602	019	IC-SCHALTUNG N74LS32N		17
4	2	13	9332 871 10602	020	IC-SCHALTUNG N74LS38N		17
5	1	13	9332 871 30602	021	IC-SCHALTUNG N74LS42N		17
6	6	13	9332 316 50772	022	IC-SCHALTUNG SN74LS74N		17
7	1	13	9332 873 00602	023	IC-SCHALTUNG N74LS112N		17
8	1	13	9332 747 50772	024	IC-SCHALTUNG SN74LS153N		17
9	3	13	9334 451 20772	025	IC-SCHALTUNG SN74LS163AN		17
10	2	13	9332 874 40602	026	IC-SCHALTUNG N74LS164N	SOW	23

S T U E C K L I S T E >5112 291 77422< SESCO

LF	MENGE	ME	CODE NUMMER	POS	BENENNUNG	NORBE	FRAKM6
1	1	13	5112 212 07030	001	PRINT SESCO/02		2776
2	1	13	2422 025 89283	002	STIFTLEISTE 96POL		1745
3	2	13	5112 209 18870	003	STIFTLEISTE 49POL		2385
4	1	13	5112 209 04800	004	STIFTLEISTE 33POL		1745
5	1	13	5112 209 04760	005	STIFTLEISTE 15POL		1745
6	2	13	5112 209 04730	006	STIFTLEISTE 5POL		2570
7	1	13	5112 211 03270	007	STIFTLEISTE 3POL		1745
8	2	13	5112 211 06040	008	STIFTLEISTE 2POL		1745
9	2	13	2422 024 88003	009	BUCHSENSTECKER 2POL		2385
10	2	13	5112 200 06890	010	ROHRNIET A2,5X0,3X9,5-MS		1745
11	1	13	9332 315 90772	012	IC-SCHALTUNG SN74LS00N		1745
12	3	13	9332 886 70602	013	IC-SCHALTUNG N74LS02N		1745
13	4	13	9332 316 00772	014	IC-SCHALTUNG SN74LS04N		1745
14	4	13	9332 735 20772	015	IC-SCHALTUNG SN74LS08N		1745
15	1	13	9332 869 70602	016	IC-SCHALTUNG N74LS10N		1745

FC = NEUE SEITE FB = NEUE FUNKTION FA = ENDE >

S T U E C K L I S T E >5112 291 77422<

LF	MENGE	ME	CODE NUMMER	POS	BENENNUNG	NORBE	FRAKM6
1	1	13	9332 746 70682	017	IC-SCHALTUNG SN74LS11N		1745
2	3	13	9332 759 70772	018	IC-SCHALTUNG SN74LS14N		1745
3	2	13	9332 870 90602	019	IC-SCHALTUNG N74LS32N		1745
4	2	13	9332 871 10602	020	IC-SCHALTUNG N74LS38N		1745
5	1	13	9332 871 30602	021	IC-SCHALTUNG N74LS42N		1745
6	6	13	9332 316 50772	022	IC-SCHALTUNG SN74LS74N		1745
7	1	13	9332 873 00602	023	IC-SCHALTUNG N74LS112N		1745
8	1	13	9332 747 50772	024	IC-SCHALTUNG SN74LS153N		1745
9	3	13	9334 451 20772	025	IC-SCHALTUNG SN74LS163AN		1745
10	2	13	9332 874 60602	026	IC-SCHALTUNG N74LS164N	SOW	2385

LF	MENGE	ME	CODE NUMMER	POS	BENENNUNG	NORBE	FRAKM6
13	2	13	9334 005 50772	029	IC-SCHALTUNG SN74LS241N		1745
14	4	13	9333 948 70772	030	IC-SCHALTUNG SN74LS273N	SOW	1745
15	1	13	9334 534 00772	031	IC-SCHALTUNG SN74LS373N		1745

FC = NEUE SEITE FB = NEUE FUNKTION FA = ENDE >

S T U E C K L I S T E >5112 291 77422<

LF	MENGE	ME	CODE NUMMER	POS	BENENNUNG	NORBE	FRAKM6
1	2	13	9336 110 10682	032	IC-SCHALTUNG SN74LS640N		1745
2	1	13	8212 221 05050	033	IC-SCHALTUNG SN74LS642-1N		1745
3	1	13	8212 221 05060	034	IC-SCHALTUNG SN74LS646N		1745
4	1	13	9331 719 20772	035	IC-SCHALTUNG SN7438N		1745
5	3	13	9332 920 50602	036	IC-SCHALTUNG N74S38N		1745
6	2	13	9336 200 00682	037	IC-SCHALTUNG SN74S161N		1745
7	1	13	9335 845 40682	038	IC-SCHALTUNG 74F00PC		1745
8	1	13	9336 203 30682	039	IC-SCHALTUNG 74F04PC		1745
9	2	13	9336 180 30682	040	IC-SCHALTUNG 74F157PC		1745
10	1	13	9336 329 30682	041	IC-SCHALTUNG 74F175PC		2385
11	1	13	5112 208 00080	042	IC PAL16L8CNSHRP/SESCO-1		2385
12	1	13	5112 208 00090	043	IC PAL16L8CNSHRP/SESCO-2		2385
13	1	13	5112 209 19490	044	IC-SCHALTUNG N82S123N/SASI-1		2385
14	1	13	5112 209 18850	045	IC-SCHALTUNG N82S123N/FLEXCO-2		2385
15	1	13	9336 075 10682	046	IC-SCHALTUNG AM9517A-4PC		1745

FC = NEUE SEITE FB = NEUE FUNKTION FA = ENDE >

S T U E C K L I S T E >5112 291 77422<

LF	MENGE	ME	CODE NUMMER	POS	BENENNUNG	NORBE	FRAKM6
1	1	13	9336 660 60682	047	IC-SCHALTUNG UPD765AC		2385
2	1	13	9332 201 50902	048	IC-SCHALTUNG MC4024P		1745
3	1	13	9332 394 40902	049	IC-SCHALTUNG MC4044P		1745
4	1	13	9332 996 00602	050	IC-SCHALTUNG MUA7805CU	SOW	1745
5	1	13	2722 171 08002	052	OSZILLATOR 16MHZ		1745
6	1	13	2322 151 51001	055	ME-WID 0,4/70 100R/1		1745
7	1	13	2322 151 52001	056	ME-WID 0,4/70 200R/1		1745
8	7	13	2322 151 52211	057	ME-WID 0,4/70 221R/1		2570
9	1	13	2322 151 53011	058	ME-WID 0,4/70 301R/1		1745
10	1	13	2322 151 53921	059	ME-WID 0,4/70 392R/1		1745
11	2	13	2322 151 55111	060	ME-WID 0,4/70 511R/1		1745
12	1	13	2322 151 59091	061	ME-WID 0,4/70 909R/1		1745
13	2	13	2322 151 51002	062	ME-WID 0,4/70 1KO/1		2570
14	1	13	2322 151 51502	063	ME-WID 0,4/70 1K5/1		1745
15	1	13	2322 151 52002	064	ME-WID 0,4/70 2KO/1		1745

FC = NEUE SEITE FB = NEUE FUNKTION FA = ENDE >

S T U E C K L I S T E >5112 291 77422<

LF	MENGE	ME	CODE NUMMER	POS	BENENNUNG	NORBE	FRAKM6
1	1	13	2322 151 54752	065	ME-WID 0,4/70 4K75/1		1745
2	1	13	2322 151 58252	066	ME-WID 0,4/70 8K25/1		1745
3	1	13	2322 151 52003	067	ME-WID 0,4/70 20K/1		1745
4	2	13	5112 291 02910	068	ME-WID-REIHE E96		1815
5	1	13	5112 209 17430	071	IC WID-NETZWERK 1361		1745
6	1	13	5112 209 17440	072	IC WID-NETZWERK 1362		1745
7	1	13	5112 209 11540	073	IC WID-NETZWERK 1106	SOW	1745
8	1	13	5112 209 12910	074	IC-SCHALTUNG NW1106		1745
9	4	13	5112 211 40230	075	KLOETZCHEN		1745
10	2	13	2522 643 02046	076	ROHRNIET A2X0,3X8-MS		1745

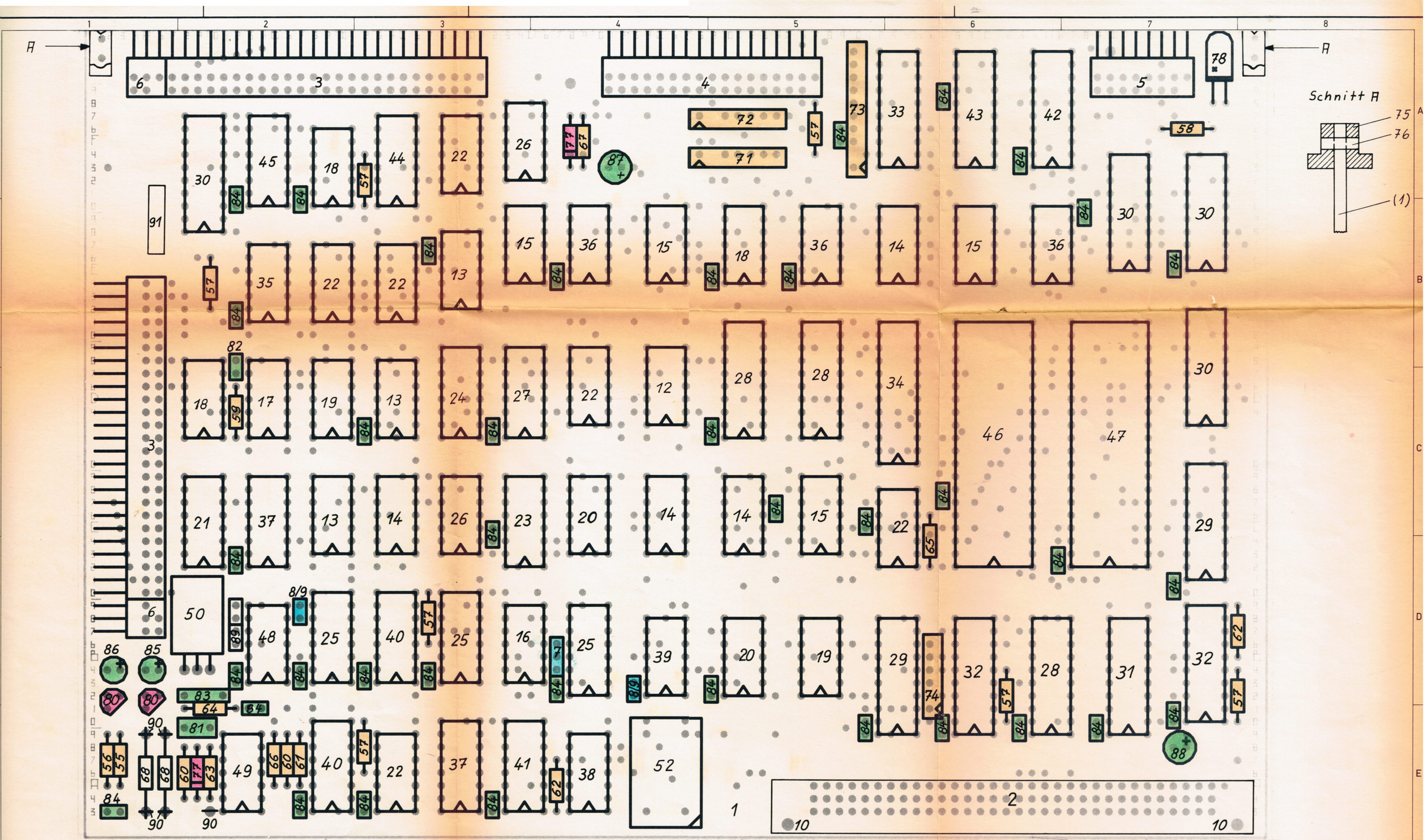
13	2	13	9331	976	20000	080	TRANSISTOR BC547A			1745
14	1	13	2012	324	03001	081	KP-KO 1N5/5 160			1745
15	1	13	2222	630	05472	082	EDRU-KO 2R/2 4N7/10 63			1745

FC = NEUE SEITE FB = NEUE FUNKTION FA = ENDE >

S T U E C K L I S T E >5112 291 77422<

LF	MENGE	ME	CODE NUMMER	POS	BENENNUNG	NORBE	FRAKM6
1	1	13	2012 310 03108	083	MKT-KO 33N/5 100		1745
2	38	13	2022 552 00524	084	KDPU-KO 100N/20 50		2385
3	1	13	2012 198 07337	085	EL-KO 330N/35		1745
4	1	13	2022 017 00072	086	EL-KO 2MU2/100		1745
5	1	13	2222 034 88478	087	EL-KO 4U7/63		1745
6	1	13	2020 002 90542	088	AL-KO 33U/25		1745
7	1	13	5112 291 45780	089	ABGLEICHKONDENSATOR OZ		1815
8	5	13	5112 209 17000	090	LOETSTIFT 5-MS SN		2385
9	1	13	5112 211 46510	091	CCA-AUFKLEBER		1745

FC = NEUE SEITE FB = NEUE FUNKTION FA = ENDE >



Lage beachten:

Pos. 77 — Kathode

83 04 27

37 x 14 pol.
14 x 16 pol.
15 x 20 pol.
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2 x 40 pol.
69

2570	Freigabe	4.5.83							
Ind.	KM	Änderung	Dat.	Name	Ind.	KM	Änderung	Dat.	Name

Rauheit UN - D 28 ✓ ▽ ▽ µm DIN ISO 1302

zul. Abweichung für Maße ohne Toleranzangabe: DIN 7184 / A UN - D 603

allgemeine Rauheit | Einheit mm | Werkstoff

Maßstab 1:1 | Europ. Proj. | Behandlung

Modell - Nr.

1983 Sep. 5

Auftrags - Nr.

CLASS

PRINT SESCO

Nur zur Information

5112 291 77422

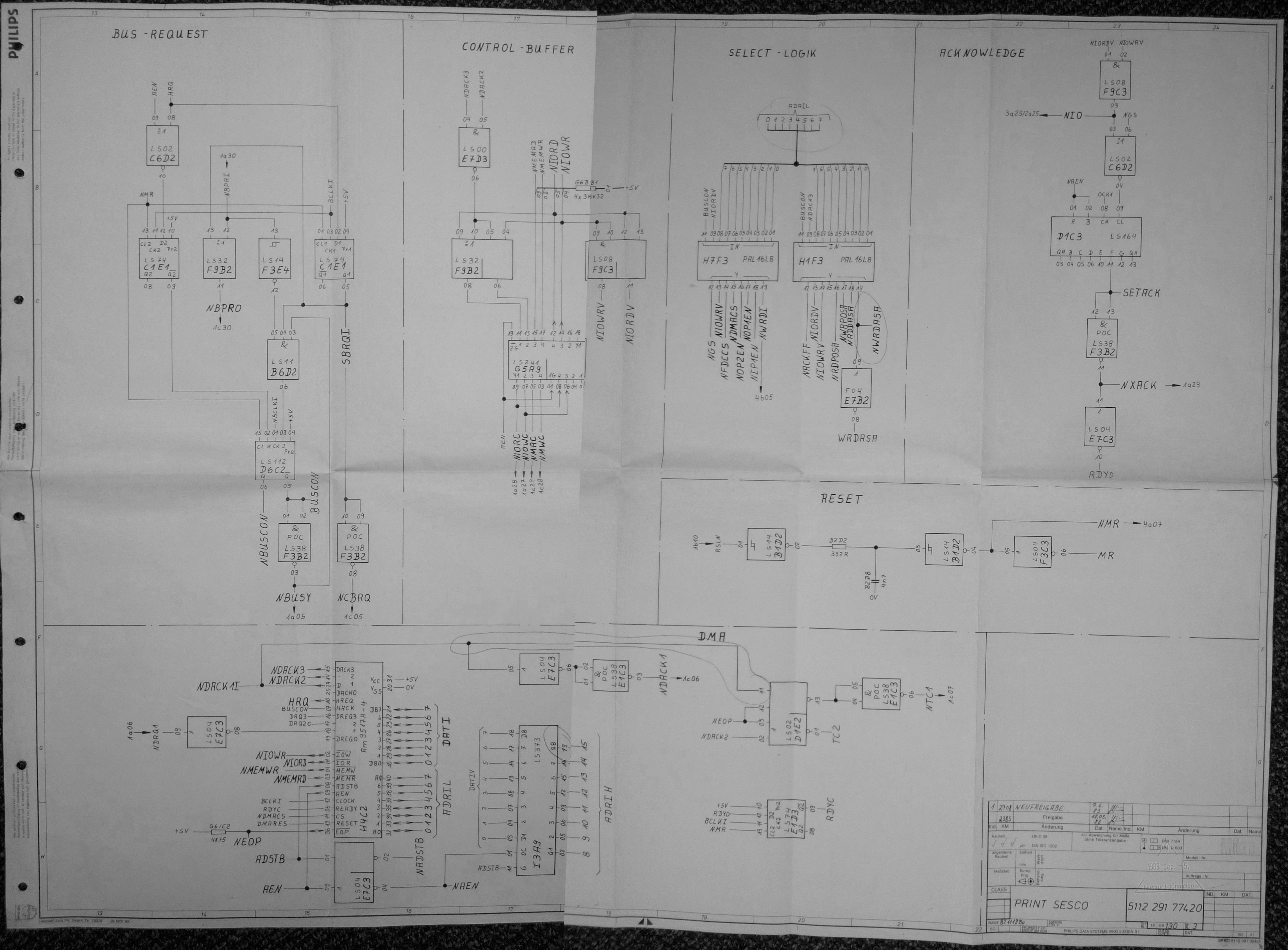
IND. | KM | DAT.

NAME 4.5.83 | SUPERS. | ERS. F. | SH. BL. 18 | GR 110 | SH.

SO | PROPERTY OF EIGENTUM VON: PHILIPS DATA SYSTEMS 5900 SIEGEN 31 | CHECK KONTR. | DAT. | SO | A2

5112 891 0022

BORN, 5912 Hilchenbach V 1168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NBPRO
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NIORDV
NIORD
NIOWR
SETACK
NXACK
RDYD
NMR
MR
NDACK1
NTC1
TC2
DATI
ADRIL
ADRIH
NEOP
ADSTB
AEN
NAEN
NADSTB
RDYC
WRDASA
NEUFREIGABE
PRINT SESCO
5112 291 77420
PHILIPS DATA SYSTEMS 5900 SIEGEN 21

PHILIPS

Blatt Nr.	Index	Lfd. Nr.	Index	Lfd. Nr.	Index	Lfd. Nr.	Index	Lfd. Nr.	Index	Lfd. Nr.	Index	Lfd. Nr.	Index	Lfd. Nr.	Index	Lfd. Nr.	Index	Lfd. Nr.
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3	0	0	1	1														
4	0	0	1	1														
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7																		
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Blatt Nr.	Index	Lfd. Nr.	Index	Lfd. Nr.	Index	Lfd. Nr.	Index	Lfd. Nr.	Index	Lfd. Nr.	Index	Lfd. Nr.	Index	Lfd. Nr.	Index	Lfd. Nr.	Index	Lfd. Nr.
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Lfd. Nr.	KM-Nr.	Lfd. Nr.	KM-Nr.	Lfd. Nr.	KM-Nr.	Lfd. Nr.	KM-Nr.	Lfd. Nr.	KM-Nr.	Lfd. Nr.	KM-Nr.	Lfd. Nr.	KM-Nr.	Lfd. Nr.	KM-Nr.	Lfd. Nr.	KM-Nr.	Lfd. Nr.	KM-Nr.
0	2385	2		4		6		8		10		12		14		16		18	
1	2708	3		5		7		9		11		13		15		17		19	

1983 Sep. 5

Nur zur Information

5112 291 77420

CLASS

PRINT SESCO

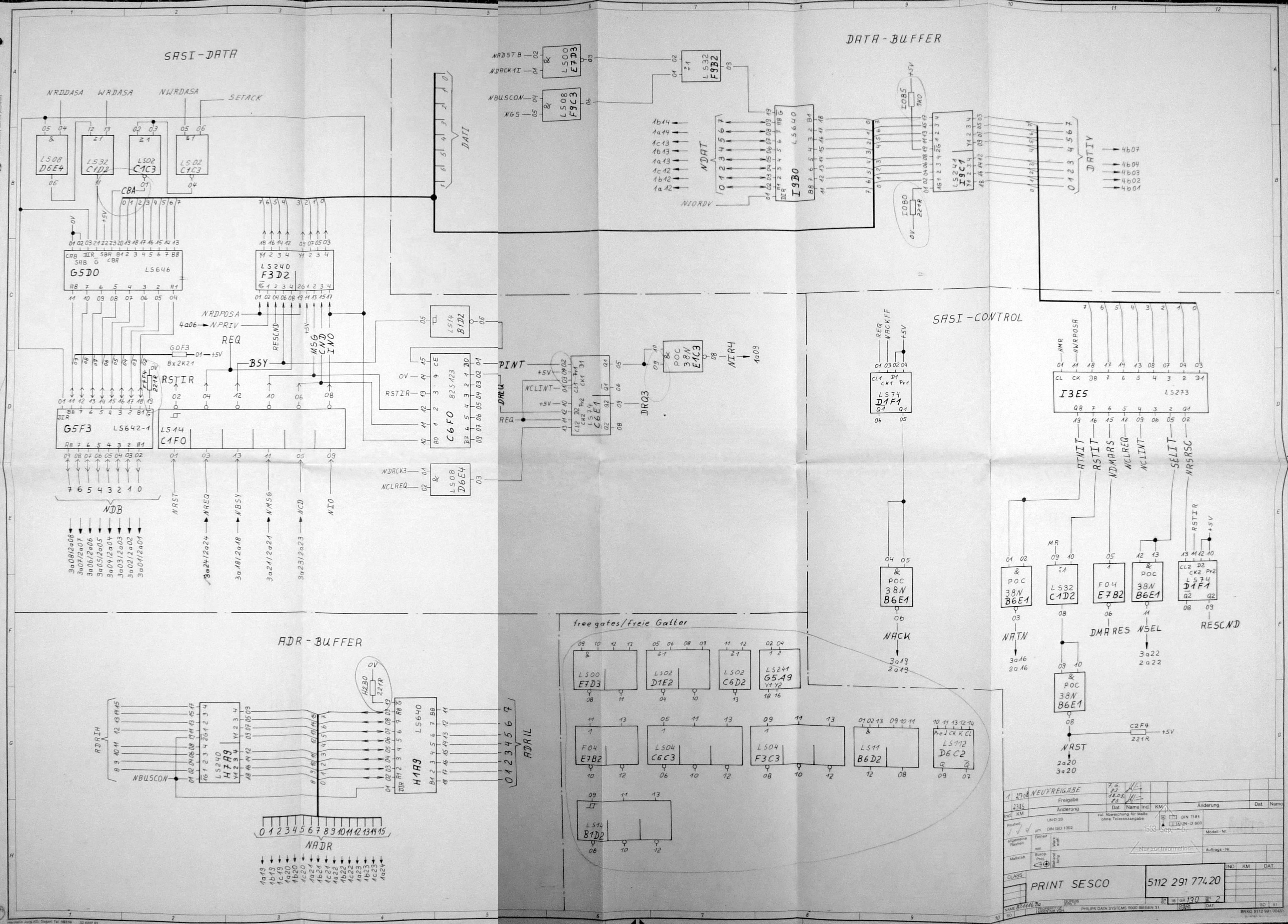
IND.	KM	DAT.
–	2385	83-03-30
1	2708	83-06-08

NAME 22.3.83 SUPERS. ERS. F. 1 SH. BL. 18 GR 130 SH. BL. 6

SO PHILIPS GMBH DATA SYSTEMS 5900 SIEGEN 31 CHECK KONTR. DAT. FORM A4

AHLBORN 5912 Hilchenbach V 443

5112 298 00220



PHILIPS
SASI-DATA
DATA-BUFFER
SASI-CONTROL
ADR-BUFFER
free gates/freie Gatter
NRDDASA
WRDASA
NWRDASA
SETACK
CBA
DATI
NDAT
DATIV
NIORDV
NADST B
NDACK1I
NBUSCON
NG5
G5D0 LS646
F3D2 LS240
G5F3 LS642-1
C1F0 LS14
C6F0 825123
C6E1 LS74
E1C3
I9B0 LS640
I9C1 LS241
I3E5 LS273
D1F1 LS74
B6E1
C1D2 LS32
E7B2 F04
H7A9 LS240
H1A9 LS640
NRDPOSA
NPRIV
REQ
BSY
RSTIR
RESCND
MSG
CND
INO
PINT
NCLINT
DRQ
DRQ3
NIR4
NDACK3
NCLREQ
NDB
NRST
NREQ
NBSY
NMSG
NCD
NIO
NACK
ATNIT
RSTIT
NDMARS
NCLREQ
NCLINT
SELIT
NRSRSC
NATN
DMARES
NSEL
RESCND
ADRIH
ADRIL
NADR
NBUSCON
NEUFREIGABE
Freigabe
Änderung
PRINT SESCO
5112 291 77420
PHILIPS DATA SYSTEMS 5900 SIEGEN 31
Nur zur Information

PHILIPS
BUS-REQUEST
CONTROL-BUFFER
SELECT-LOGIK
ACKNOWLEDGE
RESET
DMA
LS02 C6D2
LS74 C1E1
LS32 F9B2
LS14 F3E4
LS11 B6D2
LS112 D6C2
LS38 F3B2
LS00 E7D3
LS08 F9C3
LS241 G5A9
PAL16L8
H7F3
H1F3
F04 E7B2
LS164 D1C3
LS04 E7C3
LS14 B1D2
LS04 F3C3
LS373 I3A9
Am 9517A-4 H4C2
LS02 D1E2
LS38 E1C3
LS74 E1D3
NMR
NBPRI
BCLKI
NBPRO
SBRQI
NBUSCON
BUSCON
NBUSY
NCBRQ
NDACK3
NDACK2
NMEMRD
NMEMWR
NIORD
NIOWR
NIOWRV
NIORDV
AEN
NIORC
NIOWC
NMRC
NMWC
ADRIL
NGS
NFDCCS
NDMACS
NOP2EN
NOP1EN
NIP1EN
NWRDI
NACKFF
NRDPOSA
NWRPOSA
NWRDASA
WRDASA
NIO
SETACK
NXACK
RDYD
RSLN
392R
4n7
MR
NDACK1
NTC1
TC2
NEOP
HRQ
NDRQ1
ADSTB
NADSTB
AEN
NAEN
DATI
DATIV
ADRIH
RDYC
NEUFREIGABE
Freigabe
Änderung
PRINT SESCO
5112 291 77420
PHILIPS DATA SYSTEMS 5900 SIEGEN 31


FD-CONTROLLER
DATI
FD-OUTPUT PORTS
DATIV
INSIDE-TEST-HW
COCK
NWRP
NTRO
REDA
NREDA
NURDY
NIND
USOV
NUSOV
US1V
NUS1V
RWSV
HDSV
NUS2
NUS1
NUS3
NHDS
NSTP
FR/STEP
LWRC/DIR
NDIR
WDI
WREN
WRENI
NWRDA
NWREN
NWRIH
MR
NFDCR
DUNL2
DUNL1
ENINF
MIRN2
NIRN1
NINUL2
NINUL1
NMOT2
NMOT1
NWPCI
NTESLED
NRWTRES
NEUFREIGABE
Freigabe
Änderung
PRINT SESCO
5112 291 77420
PHILIPS DATA SYSTEMS


PHILIPS
SYNCRONISATION
PLL
WRITE - CLOCK - LOGIK
CLOCK - GENERATOR
PRE - COMPENSATION - LOGIK
RIX
NSTB
STB
CRE
VIX
RCK
NT
DATI
REDAX
UM
RGV
NBCLKI
BCLKI
NBCLK
ØCK7
CØCKF
ØCK1
RI
VI
RWD
ØCK8
ØCK6
ØCK2
ØCK3
ØCK5
ØCK4
NMFM
WCK
WRDAPS
LWRC/DIR
NWPCI
WRDA
WREN
PS0
PS1
MC4044
MC7805 CT
MC4024
BC547
1N4446
Pin 5 0Vsp
Pin 1 0Vsp
Pin 7 GND
Pin 14 Vcc
NEUFREIGABE
Freigabe
Änderung
PRINT SESCO
5112 291 77420
PHILIPS DATA SYSTEMS 5900 SIEGEN 21


PHILIPS
SYNCRONISATION
CLOCK - GENERATOR
PLL
WRITE - CLOCK - LOGIK
PRE - COMPENSATION - LOGIK
RIX
NSTB
STB
PU
CRE
VIX
RCK
NT
DATI
REDAX
UM
RGV
NBCLKI
BCLKI
NBCLK
ØCK7
CØCKF
ØCK1
RI
VI
RWD
ØCK8
ØCK6
ØCK2
ØCK3
ØCK5
ØCK4
NMFM
WCK
WRDAPS
LWRC/DIR
NWPCI
WRDA
WREN
PS0
PS1
NEUFREIGABE
Freigabe
Änderung
PRINT SESCO
5112 291 77420
PHILIPS DATA SYSTEMS 5900 SIEGEN 21

49 50 51 52 53 54 55 56

Stecker/plug 1

	c	b	a
1	+5V	+5V	+5V
2	0V	+5V	
3	0V	0V	0V
4			
5	NCBRQ	NBCLK	NBUSY
6	NDACK1		NDRQ1
7	NTC1		
8			
9			NIR4
10	NIR7	RSLN	
11	0V	0V	0V
12	NDAT2	NDAT1	NDAT0
13	NDAT5	NDAT4	NDAT3
14		NDAT7	NDAT6
15			
16			
17			
18	0V	0V	0V
19	NADR2	NADR1	NADR0
20	NADR5	NADR4	NADR3
21	NADR8	NADR7	NADR6
22	NADR11	NADR10	NADR9
23	NADR14	NADR13	NADR12
24			NADR15
25			
26			
27			NIOWC
28	NMWC		NIORC
29	NMRC		NXACK
30	NBPR0		NBPRI
31			+12V
32			-12V

Stecker/plug 2

	b	a
1	0V	NDB0
2	0V	NDB1
3	0V	NDB2
4	0V	NDB3
5	0V	NDB4
6	0V	NDB5
7	0V	NDB6
8	0V	NDB7
9	0V	
10	0V	
11	0V	
12	0V	
13	0V	
14	0V	
15	0V	
16	0V	NATN
17	0V	
18	0V	NBSY
19	0V	NACK
20	0V	NRST
21	0V	NMSG
22	0V	NSEL
23	0V	NCD
24	0V	NREQ
25		NIO

Stecker/plug 4

	b	a
1	DATIV0	0V
2	DATIV1	0V
3	DATIV2	0V
4	DATIV3	0V
5	NWRDI	0V
6		NPRIV
7	DATIV4	NMR
8		+5V

Stecker/plug 6

Stecker/plug 3

	b	a
1	+5V	+5V
2	+5V	
3		
1	0V	NDB0
2	0V	NDB1
3	0V	NDB2
4	0V	NDB3
5	0V	NDB4
6	0V	NDB5
7	0V	NDB6
8	0V	NDB7
9	0V	
10	0V	
11	0V	
12	0V	
13	0V	
14	0V	
15	0V	
16	0V	NATN
17	0V	
18	0V	NBSY
19	0V	NACK
20	0V	NRST
21	0V	NMSG
22	0V	NSEL
23	0V	NCD
24	0V	NREQ
25		NIO

Stecker/plug 5

	b	a
1	0V	NURDY
2	0V	NINU1
3	0V	NMOT2
4	0V	NIND
5	0V	NUS1
6	0V	NUS2
7	0V	NUS3
8	0V	NMOT1
9	0V	NDIR
10	0V	NSTP
11	0V	NWRDA
12	0V	NWREN
13	0V	NTR0
14	0V	NWRP
15	0V	NREDA
16	0V	NHDS
17		NINU2

Stecker/plug 7

	b	a
1	+5V	+5V
2	+5V	
3		

Ind.	KM	Änderung	Dat.	Name
1	2708	NEUFREIGABE	7.6.83	
	2385	Freigabe	18.03.83	

Rauheit UN-D 28 µm DIN ISO 1302 — zul. Abweichung für Maße ohne Toleranzangabe — DIN 7184 / UN - D 603

allgemeine Rauheit — Einheit mm — Werkstoff — Modell - Nr.

Maßstab — Europ Proj. — Behandlung — Auftrags - Nr.

CLASS

PRINT SESCO

5112 291 77420

IND.	KM	DAT.

NAME 94 821202 — SUPERS ERS F — SH BL 18 — GR 130 — SH BL 6

SO — PROPERTY OF EIGENTUM VON PHILIPS DATA SYSTEMS 5900 SIEGEN 31 — CHECK KONTR. — DAT — SO — A3

Abgleichanweisung für PCB SESCO/00

2.5.83

Abgleichanweisung für Print SESCO/00

1. Maßnahmen zum Abgleich

Zum Abgleich müssen dem Print SESCO/00 folgende Spannungen und Signale zugeführt werden:

RSLN = LOW (St 1 Pin 610)

0V

+5V ±2%

+12V ±2%

-12V ±2% (für Flexco)

Vor dem Abgleich muß der Print mindestens 2 Minuten an den Versorgungsspannungen liegen, so daß der spannungsgesteuerte Oszillator (IC B6B3) eine Arbeitstemperatur von ca. 30° - 35°C (gemessen an der Oberfläche) annimmt. Alle Messungen sind bei Raumtemperatur durchzuführen.

Nach Lötarbeiten in der Nähe des IC's B6B3 (MC4024) ist auf die Arbeitstemperatur des Bausteins zu achten.
Es ist darauf zu achten, daß die Brücken B7B8 und E3B2 während des Abgleichs gesteckt sind.

RA5A9 (301R) muß eingelötet sein.
RA7A9 darf nicht eingelötet sein.

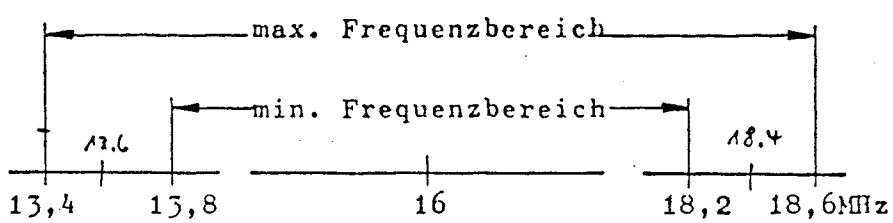
Erforderliche Meßgeräte

Multimeter PM 2403

Frequenzmesser, z.B. PM 6620; PM 6645

2. Durchführung des Abgleichs

Der Arbeitsfrequenzbereich beträgt 16MHz ±15% (13,6MHz - 18,4MHz).
Die Toleranz des Abgleichs beträgt ±0,2MHz.



MIKRO

CLASS	PRINT SESCO/00		IND.	KM	DAT.
			-	0075	810831

NAME SUPERS. SH. GR. 165 SH. 2

PCB

1-

2.1 Einstellen der oberen Grenzfrequenz

Frequenzmesser am Ausgang des VCO (B6B3 , Pin 8) anschließen. Mit Kondensator B2B3 die obere Grenzfrequenz auf 18,2 - 18,6MHz abgleichen.

Zu verwendende Kapazitätswerte:

C : 15pF; 22pF; 27pF; eventuell mit
1,0pF; 1,2pF; 1,5pF; 2,0pF; 2,2pF; 2,7pF; 3,3pF; 3,9pF; 4,7pF
5,6pF; 6,8pF parallel

2.2 Einstellung der unteren Grenzfrequenz

Punkt A7A3 und Punkt A5A9 mit einer Diode BAX18 überbrücken (Lage beachten; Blatt 4).
Mittels Widerstand A7A9 die untere Grenzfrequenz auf 13,4MHz - 13,8MHz einstellen.

Zu verwendende Widerstandswerte für A7A9: 158R - 825R (E96 Reihe)

Nach Frequenzabgleich ist die Diode zu entfernen.

2.3 Mittelspannungsabgleich

Multimeter (Meßbereich 3V) über einen Widerstand 200K an B0A3 legen. Mit dem Widerstand A5A9 die Spannung an diesem Punkt auf 2,45V - 2,55V abgleichen.

Zu verwendende Widerstandswerte für A5A9:
274R; 280R; 287R; 294R; 301R; 316R; 324R; 332R; 340R;
348R; 357R; 365R; 374R; 383R; 392R

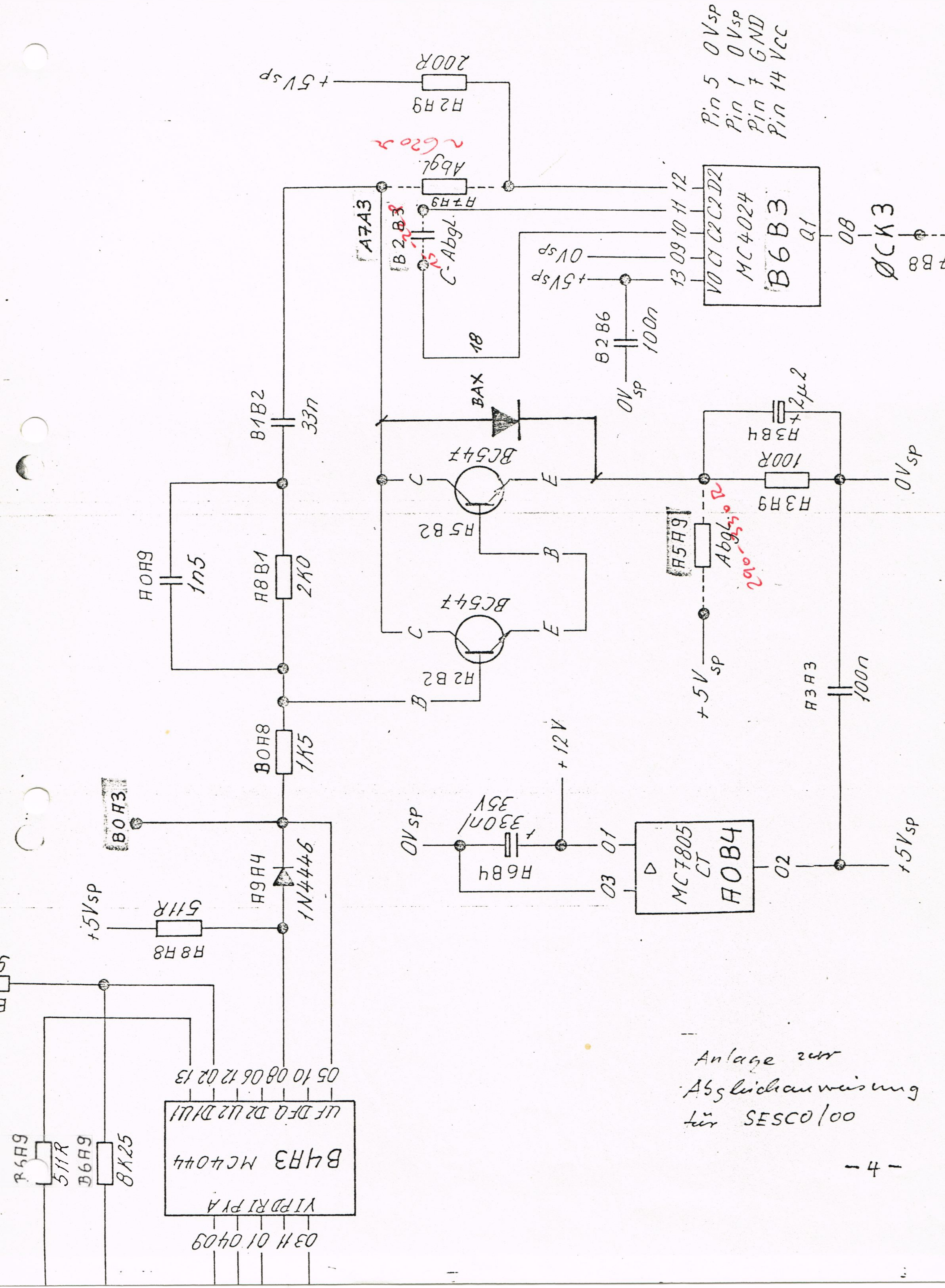
3. In der beigefügten Bestückung (Ausschnitt) ist die Bauteilbezeichnung angegeben (siehe Blatt 4).

4. Schaltplan

5112 291 77420-130

MIKRO

CLASS			IND.	KM	DAT.
	PRINT		–	0075	810831



Anlage zur
Abgleichanweisung
für SESCO100

Turbodos disk and directory layout

1. Physical disk layout

The physical disk layout is determined by the disk parameters. These parameters are a part of the disk specification table of the disk driver for that disk type.

The disk must be formatted in accordance with these parameters.

- The physical disk parameters are:

TRKDSK :: total tracks on the disk
RESTRK :: number of reserved tracks
SECTRK :: number of sectors per track
SECSIZ :: a number which represents the sector size (0-7)
RSECSIZ :: the real sector size in bytes, which can be calculated as follows: $2^{(SECSIZ + 7)}$ bytes

2. Logical disk layout

The logical disk layout describes that part of the disks which is used by the operating system after IPL (e.g. the non reserved tracks).

The minimum amount of disk space, which can be allocated is called the allocation block size.

- The logical disk parameters are:

BLKSIZ :: a number, which represents the allocation block size (3-7) 3≙2k, 4≙4k, 5≙8k
RBLKSIZ:: the real block size in bytes, which can be calculated as follows: $2^{(BLKSIZ + 7)}$ bytes

BLKPNT :: the address of a allocation block on a disk as used in the directory entry.
This pointer is 16 bits and can therefore address 64K blocks.
The most significant byte represents the least significant part of the address and the least significant part represents the most significant part of the address.

NMBBLKS:: total number of blocks on a disk with a size of RBLKISZ.

The total disk capacity used for directory and data is therefore:

NMBLKS * RBLKSIZ

3. Directory

The directory of a disk is allocated in the first block(s) on a disk.
The NMBDIR number of blocks are defined by the driver and choosen in such a way, that the directory has enough entries concerning the total disk space and the minimal file size, which is equal to the real allocation block size (RBLKSIZ).

The directory is build up out of directory entries each with a size of 32 bytes.
The toal disk capacity, which can be used for data is therefore: (NMBLKS-NMBDIR) * RBLKSIZ.

4. Directory entry layouts

There are three types of directory entries.

tupe 1 : volume label
type 2 : disk allocation map
type 3 : file description

4.1 Directory entry type 1.

byte 1 fixed 'E5'H simulated empty directory entry

byte 2-9 volume name
string filled up with spaces

byte 10-12 volume name extension
string filled up with spaces

byte 13-15 fixed '00'H unused or unknown

byte 16 fixed 'FF'H

byte 17-32 fixed '00'H unused. ← Philips - Jd ?

4.2 Directory entry type 2.

byte 1 fixed 'E5'H simulated empty directory entry

byte 2-15 bitmap for allocated disk blocks

byte 16 fixed 'FE'H

byte 17-32 bitmap for aloocated disk blocks

A directory entry of this type contains 30*8 = 240 bits each referring to an allocation block.

The bits in a byte are numbered 0-7 from least significant to most significant.

Example : Bit 2 of byte 8 of the first entry of this type refers to the allocation block with the address:

BLKPNT = 6*8+2=50
'1'B :: allocated
'0'B :: free

This bit map is always a multiple of 240 bits.
Because the disk space is hardly ever equal to a multiple of 240 blocks the bit map is filled up at the end by TURBODOS with ones for those blocks, which do not reside on the disk. When the disk is selected for the first time also those bits are set to one which refer to the directory space.

4.3 Directory entry type 3.

This type is almost equal to the CPM directory entry.

byte 1 'E5'H if this directory entry is empty
'usernumber' if this directory entry refers to one or more file extents

byte 2-9 file name
String filled up with spaces
Sign bits refer to file attributes f1-f8
f1 = F1F0 attribute
f2-f4 = unasigend, available to user
f5-f8 = interface attributes, reserved

byte 10-12 file name extension

String filled up with spaces
Sign bits refer to file attributes t1-t3
t1 = read only attribute
t2 = global attribute
t3 = archived attribute

byte 13 highest extent number in this directory entry

The size of an extent is 16K bytes and can be built up by one or more allocation blocks depending on their size.
A File Control Block can address 2^{13} = 8K extents and therefore the maximum file size is 134 Mbytes

Byte 17-33 of this entry can refer to 8 allocation blocks and therefore one directory entry can contains 1-8 extents depending on the size of an allocation block.

byte 14-5 unused or unknown = 128 byte

byte 16 number of records used in the last allocated block of this entry (maximal 7 bits used, '80'H if fully used).
A block can contain therefore maximal 128 records of 128 bytes. The maximum block size is therefore 16K bytes.

byte 17-32 8 pointers of 16 bits (BLKPNT see section 2)
They contain the logical address of an allocation block allocated by this directory entry.
The maximum number of disk blocks is therefore 16K.
Depending on the block size a disk can contains therefore minimal 134M bytes and maximal 1G bytes.

Record 00000

```
00:    E5 20 20 20 20 20 20 20 20 20 20 20 00 00 00 FF   e           ....
10:    00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
20: -  E5 FF FF FF FF FF FF 01 C0 0F 00 00 00 00 00 FE   e.......@......~
30:    00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
40:    E5 00 00 00 00 00 00 00 00 00 00 FF FF FF FF FE   e.............~
50:    FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF   ................
60:    00 42 41 53 43 4F 4D 20 20 43 CF 4D 00 00 00 80   .BASCOM  COM....
70:    04 00 05 00 06 00 07 00 08 00 09 00 0A 00 0B 00   ................
```

Record 00001

```
00:    00 42 41 53 43 4F 4D 20 20 43 CF 4D 01 00 00 80   .BASCOM  COM....
10:    0C 00 0D 00 0E 00 0F 00 10 00 11 00 12 00 13 00   ................
20:    00 42 41 53 43 4F 4D 20 20 53 D5 42 00 00 00 03   .BASCOM  SUB....
30:    14 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
40:    00 42 41 53 49 43 4C 49 42 52 C5 4C 00 00 00 02   .BASICLIBREL....
50:    15 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
60:    00 42 41 53 4C 49 42 20 20 52 C5 4C 00 00 00 80   .BASLIB  REL....
70:    16 00 17 00 18 00 19 00 1A 00 1B 00 1C 00 1D 00   ................
```

Record 00002

```
00:    00 42 41 53 4C 49 42 20 20 52 C5 4C 01 00 00 43   .BASLIB  REL...C
10:    1E 00 1F 00 20 00 21 00 22 00 00 00 00 00 00 00   .... .!."........
20:    00 42 43 4C 4F 41 44 20 20 20 A0 20 00 00 00 01   .BCLOAD     ....
30:    23 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   £...............
40:    00 42 52 55 4E 20 20 20 20 43 CF 4D 00 00 00 79   .BRUN    COM...y
50:    24 00 25 00 26 00 27 00 28 00 29 00 2A 00 2B 00   $.%.&.'.(.).*.+.
60:    00 46 49 4C 4C 52 41 54 45 43 CF 4D 00 00 00 12   .FILLRATECOM....
70:    2C 00 2D 00 00 00 00 00 00 00 00 00 00 00 00 00   ,.-.............
```

Record 00003

```
00:    00 4F 54 48 45 4C 4C 4F 20 C2 41 53 00 00 00 2C   .OTHELLO BAS...,
10:    2E 00 2F 00 30 00 00 00 00 00 00 00 00 00 00 00   ../.0...........
20:    E5 46 4F 52 4D 41 54 49 4E 43 CF 4D 00 00 00 73   eFORMATINCOM...s
30:    36 00 37 00 38 00 39 00 3A 00 3B 00 3C 00 3D 00   6.7.8.9.:.;.<.=.
40:    00 46 4F 52 4D 44 41 54 20 44 C5 46 00 00 00 0D   .FORMDAT DEF....
50:    3E 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   >...............
60:    00 46 4F 52 4D 44 41 54 20 44 D4 41 00 00 00 01   .FORMDAT DTA....
70:    3F 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ?...............
```

Record 00004

```
00:    00 46 4F 52 4D 44 41 54 20 4E C4 58 00 00 00 01   .FORMDAT NDX....
10:    40 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   @...............
20:    00 46 52 4F 4D 33 35 20 20 43 CF 4D 00 00 00 26   .FROM35  COM...&
30:    41 00 42 00 43 00 00 00 00 00 00 00 00 00 00 00   A.B.C...........
40:    E5 E5 E5 E5 E5 E5 E5 E5 E5 E5 E5 E5 E5 E5 E5 E5   eeeeeeeeeeeeeeee
50:    E5 E5 E5 E5 E5 E5 E5 E5 E5 E5 E5 E5 E5 E5 E5 E5   eeeeeeeeeeeeeeee
60:    E5 E5 E5 E5 E5 E5 E5 E5 E5 E5 E5 E5 E5 E5 E5 E5   eeeeeeeeeeeeeeee
70:    E5 E
```