NEC
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μPD72020
CMOS Graphics Display Controller

T-52-33-47

Description

The μPD72020 is an enhanced graphics display controller resulting from the implementation of CMOS technology on the μPD7220A.

In addition to the functions of the μPD7220A, the μPD72020 incorporates address space expansion, video RAM control, and write mask functions. It is suitable for a wide range of applications from simple display terminals to high-resolution graphics display devices.

This data sheet covers only functions additional to those of the μPD7220A. For further details of the μPD72020, refer to the μPD72020 User's Manual.

Features

- Enhanced functions compared with the μPD7220A
  - Video memory space: 2M bytes maximum (1M 16-bit words)
  - Control of dual-port RAM (video RAM)
  - Write-masking of any desired bit
  - Enhanced external synchronization function
  - CMOS technology
- μPD7220A-compatible functions
  - High-speed graphics drawing: 500 ns/dot (operating at 8 MHz)
  - Selection of drawing timing: flashless/flash mode
  - Drawing of straight lines, arcs, quadrilaterals, graphic characters
  - Any kind of line specifiable
  - Four different dot-correction modes
  - Enlarged drawing/enlarged display
  - Panning and scrolling
  - Automatic cursor shifting
  - Attributes assignable character by character
  - Interlaced/noninterlaced scanning
  - DRAM refreshing
  - Master/slave operation
  - Video memory control independent of main memory
  - 16 x 9-bit on-chip input/output FIFO
  - DMA control
  - Single +5-volt power supply

Applications

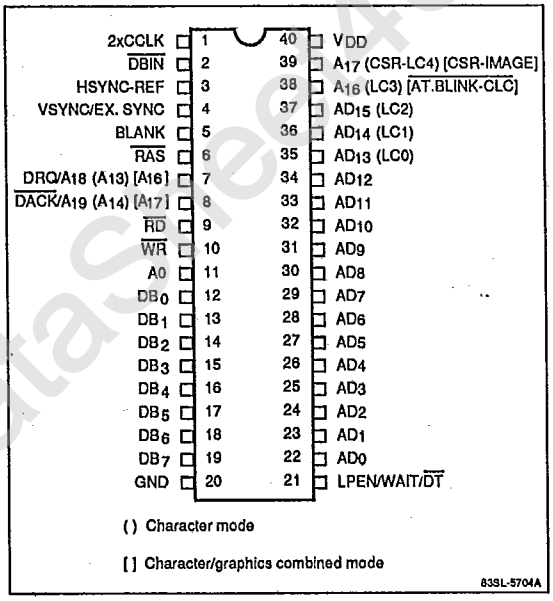
Some application functions implemented by use of this product in conjunction with other products may infringe on U.S. Patent No. 4,197,590 and Re. 31,200 etc. held by CADTRAK Corporation of the United States, and the corresponding patents in various countries. Problems may arise from such patents even when a different graphics display controller or discrete circuitry is used, and thus resolution on the basis of this product alone is not possible. Therefore, the user is requested to undertake as his or her own responsibility an investigation of measures to cope with this situation before designing an application system.

Ordering Information

Part No.	Package
μPD72020C-8	40-pin plastic DIP
μPD72020GC-8-3B6	52-pin plastic miniflat

Pin Configurations

40-Pin Plastic DIP



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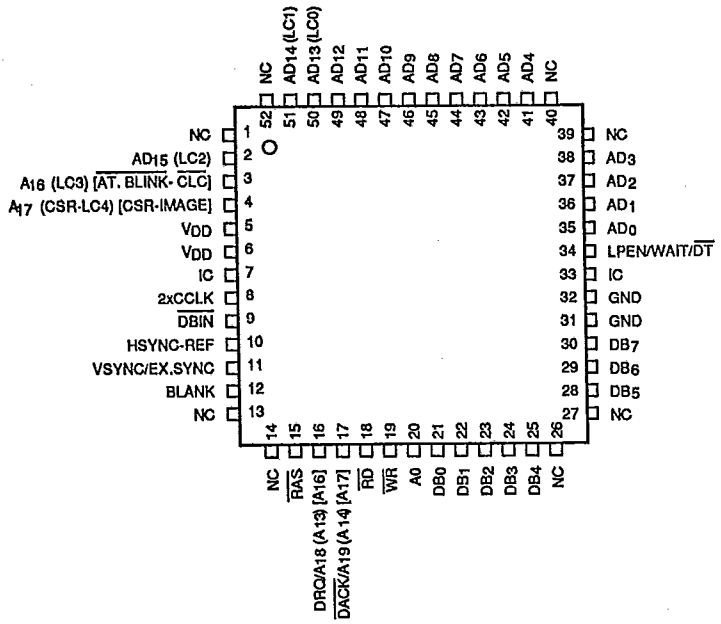
52-Pin Plastic Miniflat



( ) Character mode

[ ] Character/graphics combined mode

83SL5705B

Pin Identification

Symbol	Function
A0	Address select input for microprocessor interface
AD_0-AD_{12}	Address-data lines to display memory
AD_{13}/LC0, AD_{14}/LC1, AD_{15}/LC2	See text and table 3.
A_{16}/LC3/AT.BLINK-CLC, A_{17}/CSR-LC4/CSR-IMAGE	See text and table 3.
BLANK	CRT blanking output
$\overline{DACK}/A_{19}/A_{14}/A_{17}$	See text and table 1.
DB_0-DB_7	Bidirectional data bus to host microprocessor
$\overline{DBIN}$	Display memory read input flag
$DRQ/A_{18}/A_{13}/A_{16}$	See text and table 1.
HSYNC-REF	Horizontal video sync output

Symbol	Function
LPEN/WAIT/$\overline{DT}$	See text and table 2.
$\overline{RAS}$	Row address strobe
$\overline{RD}$	Read strobe input for microprocessor interface
VSYNC/EX.SYNC	Vertical video sync output or external VSYNC input
$\overline{WR}$	Write strobe input for microprocessor interface
2xCCLK	Clock input
GND	Ground
V_{DD}	+5-volt power supply
IC	Internal connection
NC	No connection

PIN FUNCTIONS

Pins on the μPD7220A and the μPD72020 have similar functions. Differences are described below.

Pins DRQ and $\overline{DACK}$

The functions of these pins depend on the setting of the PN bit by the WMASK command, which validates the address extension functions See table 1.

A_{13}, A_{14}, A_{16}-A_{19}. When the address extension function is selected by setting PN of the WMASK command, the upper 2 bits (of the extended address) are output in the video memory in each display/draw mode.

After the address extension function has been selected, the DMA-related functions cannot be used. Use the CHR and G bits of the SYNC command to set the display/draw mode (as with the μPD7220A).

DRQ (DMA Request). When the DMAR or DMAW command is executed, the DMA request signal is output. This signal is input to the DRQ pin of the DMA controller.

After the DMA-related functions have been selected, the address extension functions cannot be used.

$\overline{DACK}$ (DMA Acknowledge). A signal indicating DMA transfer is input. This signal is output from the $\overline{DACK}$ pin of the DMA controller.

Pin LPEN/WAIT/$\overline{DT}$

The functions of this pin depend on the setting of the DTE bit by the WMASK command, which validates the DT signal generation function. See table 2.

$\overline{DT}$ (Data Transfer). When the $\overline{DT}$ signal generation function is selected by setting DTE of the WMASK command, the $\overline{DT}$ signal is output to indicate the display address supply timings for the μPD41264-type video RAMs (VRAMs).

After the $\overline{DT}$ signal generation function has been selected, the LPEN and WAIT functions cannot be used.

LPEN (Light Pen Strobe). When the light pen detects a light input, the H-level signal is input.

After the LPEN function has been selected, the $\overline{DT}$ signal generation function cannot be used.

WAIT (Drawing Wait). When a signal that remains at the H-level for a period of at least four clocks is input in the drawing stop mode, the μPD72020 will stop drawing temporarily if it is executing drawing and output a display address.

After the WAIT function has been selected, the $\overline{DT}$ signal generation function cannot be used.

Pins AD_{13}-AD_{15}, A_{16}, and A_{17}

The functions of some other pins depend on the operating mode: character, graphics, or character/graphics combined. See table 3.

Table 1. Pin Functions Available Through Address Extension

Pin Symbol	PN Bit (WMASK Command)	Action	Mode	I/O	Pin Function
DRQ/A_{18}/A_{13}/A_{16}	0	Action similar to μPD7220A		Output	DRQ
	1	Address extension	Graphics	Output	A_{18}
			Character	Output	A_{13}
			Combined	Output	A_{16}
$\overline{DACK}$/A_{19}/A_{14}/A_{17}	0	Action similar to μPD7220A		Input	$\overline{DACK}$
	1	Address extension	Graphics	Output	A_{19}
			Character	Output	A_{14}
			Combined	Output	A_{17}

Table 2. Pin Functions Available Through $\overline{DT}$ Signal Generation

Pin Symbol	DTE Bit (WMASK Command)	Action	I/O	Pin Function
LPEN/WAIT/ $\overline{DT}$	0	Action similar to μPD7220A	Input	LPEN/WAIT
	1	$\overline{DT}$ signal generation	Output	$\overline{DT}$

Table 3. Multifunction Pins AD_{13}-AD_{15}, A_{16}, and A_{17}

Pin Symbol	Mode	I/O	Function
AD_{13}-AD_{15}	Graphics; combined	I/O	Address-data lines 13-15 to display memory
LC0-LC2	Character	Output	Line counter bits 0-2
A_{16}	Graphics	Output	Address bit 16
LC3	Character	Output	Line counter bit 3
$\overline{AT.BLINK}$-CLC	Combined	Output	Attribute blink and clear line counter
A_{17}	Graphics	Output	Address bit 17
CSR-LC4	Character	Output	Cursor and line counter bit 4
CSR-IMAGE	Combined	Output	Cursor and bit-map area flag

ADDED BLOCK FUNCTIONS

Refer to the μPD72020 Block Diagram and the System Configuration Diagram.

Video RAM Control

Additional blocks generate the $\overline{DT}$ signal, which indicates the display-address supply timings for the video RAMs. Data within the RAMs can be transferred to the serial register.

Pin Extension Control

The video memory address is extended 2 bits (with the address space extended fourfold) in each of the character, character/graphics combined, and graphics modes.

These bits are used for both $\overline{DACK}$ pin and DRQ pin in each mode: A_{14} and A_{13}; A_{17} and A_{16}; A_{19} and A_{18}.

WMASK Register

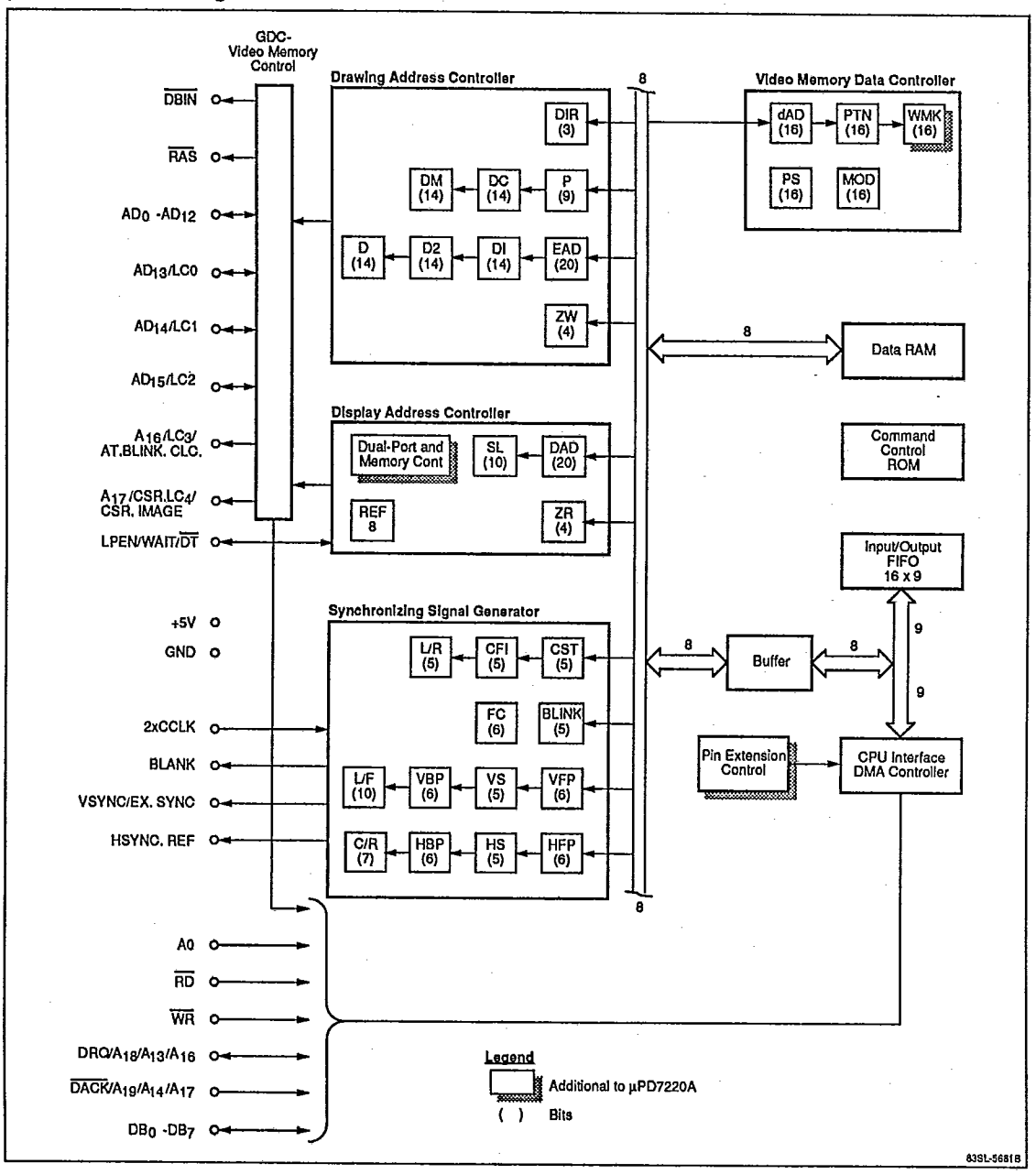
This 16-bit register is used to mask the data for multicolor synchronous drawing with one word in 8/4/2/1-bit configuration.

IMPROVED FUNCTIONS

The μPD72020 functions have been improved while maintaining compatibility with the μPD7220A in both hardware and software. Table 4 compares functions of the μPD72020 and the μPD7220A.

The μPD72020 is initialized by reset input so that it can function similarly to the μPD7220A.

μPD72020 Block Diagram



System Configuration Diagram; μPD72020 With Video RAM Control Signal $\overline{DT}$

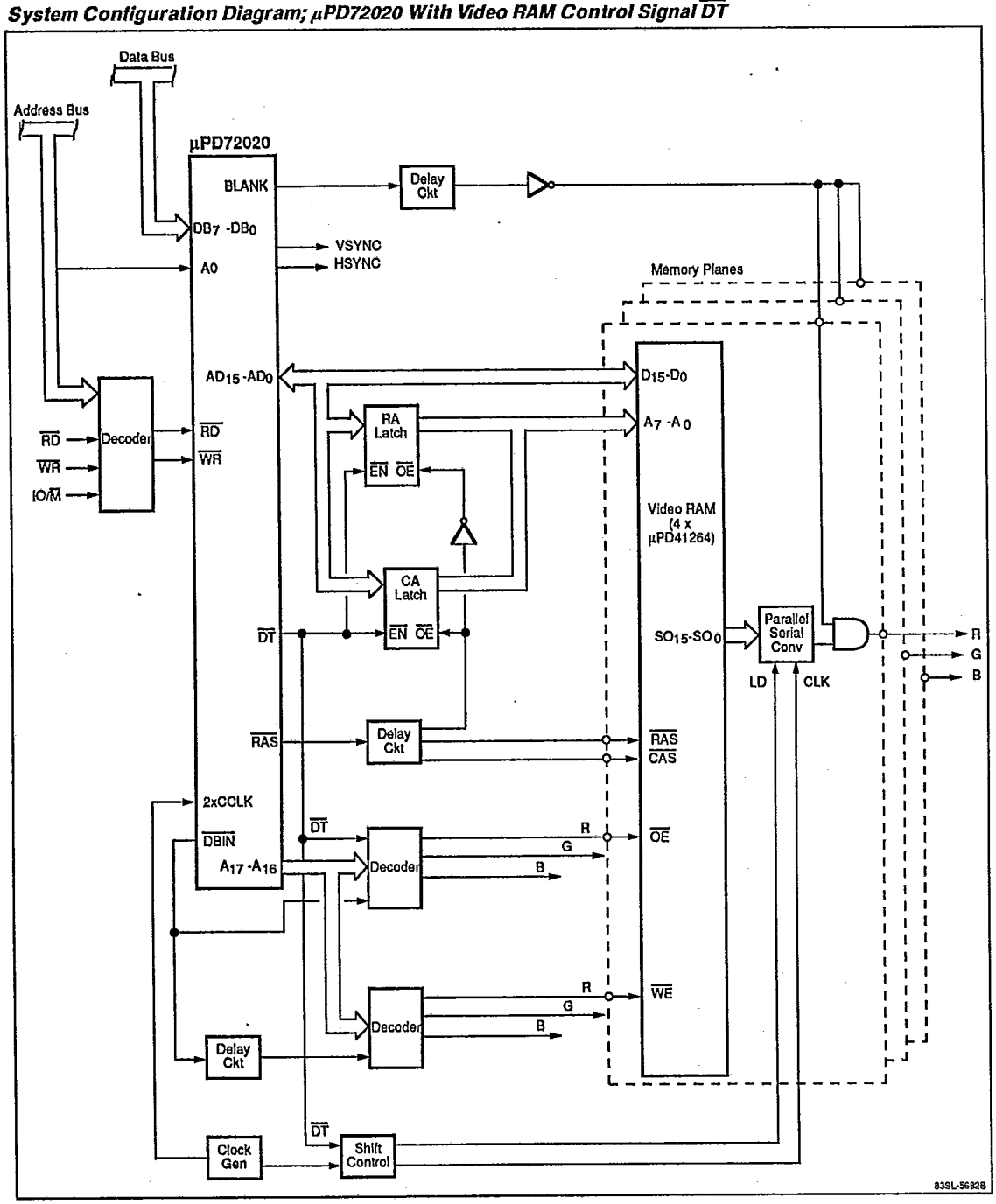


Table 4. Comparison of μPD72020 and μPD7220A Functions

μPD72020	μPD7220A
WMASK Command	
WMASK command is used to validate the new functions of the μPD72020.	WMASK command is not used.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	0	1	0	1	1	0	1	0
P1	WMKL							
P2	WMKH							
P3	PN	TM	DTE	CY1	CY0	0	0	0

WMK Sets the WMASK register value.

PN Sets the address extension function.

TM Changes the initializing timing of the horizontal synchronization counter in the slave mode for external synchronization, and sets the initializing function of the field counter.

DTE Sets the function of generating the $\overline{DT}$ signal.

CY Set the $\overline{DT}$ signal output mode and the BLANK signal mask.

LPEN Command

Light pen address (LAD) is extended 2 bits by setting PN of the WMASK command.

Light pen address (LAD) extension function is not available.

PN 0 Same as μPD7220A

1 EAD is extended 2 bits.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	1	1	0	0	0	0	0	0
D1	LADL							
D2	LADM							
D3	X	X	X	X	LADH			

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	1	1	0	0	0	0	0	0
D1	LADL							
D2	LADH							
D3	X	X	X	X	X	X	LADH	

CSRW Command

Draw execution address (EAD) is extended 2 bits by setting PN of the WMASK command.

Draw execution address (EAD) extension function is not available.

PN 0 Same as μPD7220A

1 EAD is extended 2 bits.

Character Mode

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	0	1	0	0	1	0	0	1
P1	EADL							
P2	0	EADH						

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	0	1	0	0	1	0	0	1
P1	EADL							
P2	0	0	0	EADH				

Table 4. Comparison of μPD72020 and μPD7220A Functions (cont)

μPD72020	μPD7220A

CSRW Command (cont)

Character/Graphics Combined Mode (Character Display)

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	0	1	0	0	1	0	0	1
P1	EADL							
P2	EADM							
P3	0	0	0	0	0	0	EADH	

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	0	1	0	0	1	0	0	1
P1	EADL							
P2	EADH							

Character/Graphics Combined Mode (Graphics Display/Drawing)

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	0	1	0	0	1	0	0	1
P1	EADL							
P2	EADM							
P3	dAD				0	0	EADH	
P4	WG	0	0	0	0	0	0	0

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	0	1	0	0	1	0	0	1
P1	EADL							
P2	EADH							
P3	dAD				WG	0	0	0

Graphics Mode

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	0	1	0	0	1	0	0	1
P1	EADL							
P2	EADM							
P3	dAD				EADH			
P4	WG	0	0	0	0	0	0	0

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	0	1	0	0	1	0	0	1
P1	EADL							
P2	EADM							
P3	dAD				WG	0	EADH	

CSRR Command

Draw execution address (EAD) is extended 2 bits by setting PN of the WMASK command.

PN 0 Same as μPD7220A

1 EAD is extended 2 bits.

Draw execution address (EAD) extension function is not available.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	1	1	1	0	0	0	0	0
D1	EADL							
D2	EADM							
D3	X	X	X	X	EADH			
D4	dADL							
D5	dADH							

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	1	1	1	0	0	0	0	0
D1	EADL							
D2	EADM							
D3	X	X	X	X	X	X	EADH	
D4	dADL							
D5	dADH							

Table 4. Comparison of μPD72020 and μPD7220A Functions (cont)

μPD72020	μPD7220A
SCROLL Command	
Display start address (SAD) is extended 2 bits by setting PN of the WMASK command. PN 0 Same as μPD7220A 1 SAD is extended 2 bits.	Display start address (SAD) extension function is not available.

Character Mode

Built-In RAM Map

	MSB						LSB
RA	Contents or RAM						
0	SAD1L						
1	0	SAD1H					
2	SL1L				0	0	0	0
3	*	0	SL1H				
4	SAD2L						
5	0	SAD2H					
6	SL2L				0	0	0	0
7	*	0	SL2H				
8	SAD3L						
9	0	SAD3H					
A	SL3L				0	0	0	0
B	*	0	SL3H				
C	SAD4L						
D	0	SAD4H					
E	SL4L				0	0	0	0
F	*	0	SL4H				

* DAD+2

	MSB						LSB
RA	Contents or RAM						
0	SAD1L						
1	0	0	0	SAD1H			
2	SL1L				0	0	0	0
3	*	0	SL1H				
4	SAD2L						
5	0	0	0	SAD2H			
6	SL2L				0	0	0	0
7	*	0	SL2H				
8	SAD3L						
9	0	0	0	SAD3H			
A	SL3L				0	0	0	0
B	*	0	SL3H				
C	SAD4L						
D	0	0	0	SAD4H			
E	SL4L				0	0	0	0
F	*	0	SL4H				

* DAD+2

Table 4. Comparison of μPD72020 and μPD7220A Functions (cont)

μPD72020	μPD7220A
SCROLL Command (cont)	

Character/Graphics Combined Mode (Character Display)

Built-In RAM Map

	MSB						LSB
RA	Contents of RAM						
0	SAD1L						
1	SAD1M						
2	SL1L			0	0	SAD1H	
3	*	0	SL1H				
4	SAD2L						
5	SAD2M						
6	SL2L			0	0	SAD2H	
7	*	0	SL2H				
8	SAD3L						
9	SAD3M						
A	SL3L			0	0	SAD3H	
B	*	0	SL3H				
C	SAD4L						
D	SAD4M						
E	SL4L			0	0	SAD4H	
F	*	0	SL4H				

* DAD+2

	MSB							LSB
RA	Contents of RAM							
0	SAD1L							
1	SAD1H							
2	SL1L				0	0	0	0
3	*	0	SL1H					
4	SAD2L							
5	SAD2H							
6	SL2L				0	0	0	0
7	*	0	SL2H					
8	SAD3L							
9	SAD3H							
A	SL3L				0	0	0	0
B	*	0	SL3H					
C	SAD4L							
D	SAD4H							
E	SL4L				0	0	0	0
F	*	0	SL4H					

* DAD+2

Character/Graphics Combined Mode (Graphics Display/Drawing)

Built-In RAM Map

	MSB							LSB
RA	Contents of RAM							
0	SAD1L							
1	SAD1M							
2	SL1L				0	0	SAD1H	
3	*	IM	SL1H					
4	SAD2L							
5	SAD2M							
6	SL2L				0	0	SAD2H	
7	*	IM	SL2H					

* DAD+2

	MSB							LSB
RA	Contents of RAM							
0	SAD1L							
1	SAD1H							
2	SL1L				0	0	0	0
3	*	IM	SL1H					
4	SAD2L							
5	SAD2H							
6	SL2L				0	0	0	0
7	*	IM	SL2H					

* DAD+2

Table 4. Comparison of μPD72020 and μPD7220A Functions (cont)

μPD72020	μPD7220A
Scroll Command (cont)	

Graphics Mode

Built-In RAM Map

	MSB						LSB
RA	Contents or RAM						
0	SAD1L						
1	SAD1M						
2	SL1L					SAD1H	
3	*	IM	SL1H				
4	SAD2L						
5	SAD2M						
6	SL2L					SAD2H	
7	*	IM	SL2H				

* DAD+2

	MSB						LSB
RA	Contents or RAM						
0	SAD1L						
1	SAD1M						
2	SL1L				0	0	SAD1H
3	*	IM	SL1H				
4	SAD2L						
5	SAD2M						
6	SL2L				0	0	SAD2H
7	*	IM	SL2H				

* DAD+2

COMMANDS

The μPD72020 supports all commands of the μPD7220A. Although command names are different, opcodes are the same. The μPD72020 can activate the software created for use with the μPD7220A.

The improved functions of the μPD72020 can be used by setting the new WMASK command. Once the RESET command is input, however, the WMASK command becomes inactive and the μPD72020 maintains the same functions as those of the μPD7220A.

This section describes the WMASK command as well as the SCROLL, LPEN, CSRW, and CSRR commands, which are affected by the setting of the WMASK command.

WMASK Command

This new command (figure 1) controls four new functions.

- WMASK register setting
- Address extension
- Selection of additional functions in the external slave mode
- $\overline{DT}$ signal generation

Figure 1. WMASK Command Format

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	0	1	0	1	1	0	1	0
P1	WMKL							
P2	WMKH							
P3	PN	TM	DTE	CY1	CY0	0	0	0

WMK Bit. The μPD72020 is equipped with the conventional MASK register and a 16-bit WMASK register. The WMK bit is used to set this WMASK register.

The 16-bit WMASK register is used for write mask of the multicolor, simultaneously-drawn data with one word set in 8-, 4-, 2- and 1-bit formats. Each bit of the WMASK register corresponds to each bit of the drawn data.

(1) When a WMASK register bit is set to 0 by the WMK, the drawn data bit corresponding to the WMASK register bit set to 0 is not affected by drawing.

(2) When a WMASK register bit is set to 1 by the WMK, operation is similar to the μPD7220A. Thus, the drawn data bit corresponding to the WMASK register bit set to 1 is affected by drawing.

When the RESET command is input, the μPD72020 is set to this mode.

PN Bit. PN is used to set the address extension function for the video memory.

(1) When PN = 0, operation is similar to the μPD7220A. Thus, the address extension function cannot be used.

When the RESET command is input, the μPD72020 is set to this mode.

(2) When PN = 1, the video memory address is extended 2 bits (with the address space expanded fourfold).

The DRQ/A_{18}/A_{13}/A_{16} pin and the $\overline{DACK}$/A_{19}/A_{14}/A_{17} pin output the upper 2 bits of the extended address. The DMA-related functions cannot be used.

The address to be output depends on the display and drawing modes. See table 1. The address space is shown in table 5.

Table 5. Address Space With Extended Address

	Character Mode	Character/Graphics Combined Mode	Graphics Mode
Address space	15 bits (32K words)	18 bits (256K words)	20 bits (1M words)

As the address space is expanded, the following command bits are also extended.

- LAD bit of LPEN command
- EAD bit of CSRW command
- EAD bit of CSRR command
- SAD bit of SCROLL command

Refer to the description of each command for details.

TM Bit. TM has been added to solve the following two problems with the μPD7220A.

- Because the vertical and horizontal counters are initialized at the start of VFP and HFP, respectively, when the external synchronizing signal is input to the μPD7220A, horizontal positioning cannot be readily done for synchronization with the μPD7220A by inputting a synchronizing signal from the external device.

- When the μPD7220A is operated in the interlace mode, input of the external synchronizing signal causes no effect on the field counter. Thus, if the synchronizing signal is unconditionally input from the external device when the μPD7220A is in the second field, the second and first fields are reversed in subsequent frames and the fields do not conform with the external device.

When the μPD72020 operates in the slave mode for external synchronization, the setting of the TM bit will cause the μPD72020 to operate differently from the μPD7220A in the following operations.

- The timing of initializing the horizontal synchronous counter is changed.
- The initializing function of the field counter is validated.

When TM = 0, the function similar to the external synchronizing function of the μPD7220A is carried out. When the RESET command is input, the μPD72020 is set to this mode.

When TM = 1, the following two operations differ from those of the μPD7220A.

(1) When the RESET command is executed or the EX.SYNC (external synchronizing signal) is input, the horizontal counter is reset at the rising edge of the HS. See figure 2.

(2) When the RESET command is executed in the interlace mode or the EX.SYNC signal is input, the field counter is unconditionally reset to the first field mode.

Thus, the VSYNC signal in the second field should be removed externally so that the synchronizing signal applied to the EX.SYNC pin serves as the VSYNC signal in the first field (in the interlace mode).

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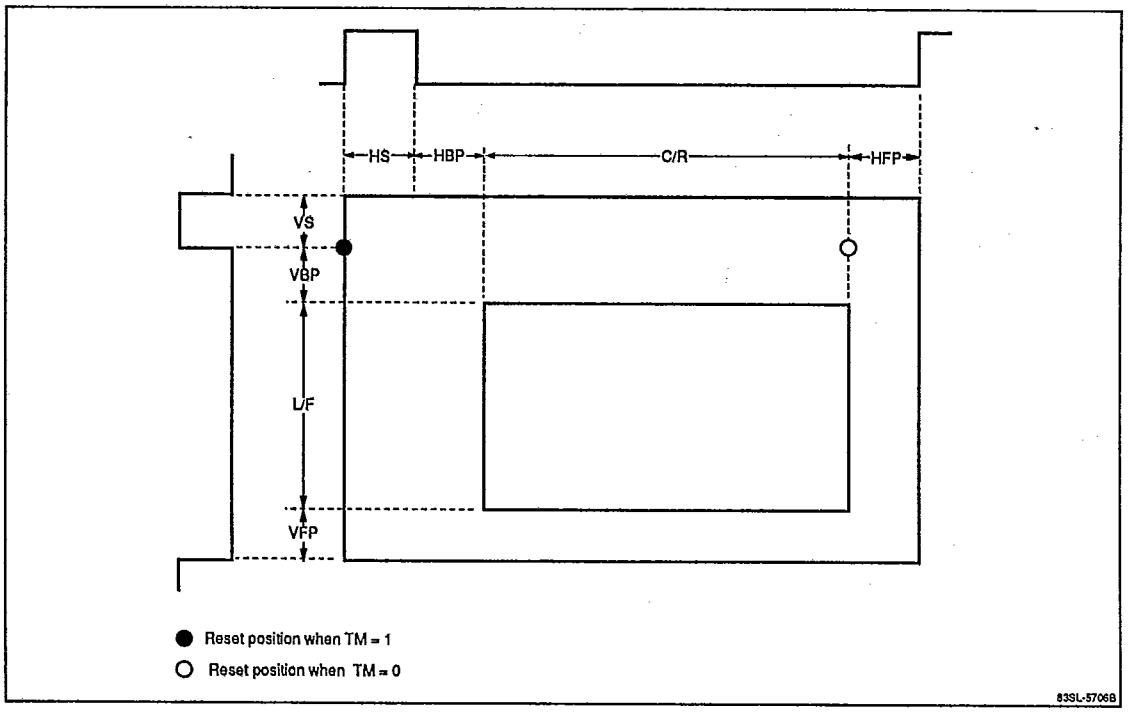
Figure 2. Horizontal Counter Reset Timing



DTE, CY1, CY0 Bits. To prevent the display screen from becoming blurred during drawing operations, the μPD7220A normally performed drawing in the flashless drawing mode. Thus, the drawing period was limited and it was difficult to improve the drawing efficiency.

To solve this problem, video RAMs can be used for the μPD72020. Through the use of VRAMs, both drawing and display can be carried out simultaneously in the flashless drawing mode with the result that the drawing efficiency can be improved. DTE, CY1, and CY0 are used to control the μPD41264-type VRAMs and the BLANK signal.

Table 6. $\overline{DT}$ Signal Output Modes

DTE	CY1	CY0	Function
0	0	0	GDC mode 0
0	0	1	GDC mode 1 (BLANK signal mask †)
0	1	0	Inhibited
0	1	1	Inhibited
1	0	0	$\overline{DT}$ signal output mode 0 (BLANK signal mask †)
1	0	1	Inhibited
1	1	0	$\overline{DT}$ signal output mode 1 (BLANK signal mask †)
1	1	1	$\overline{DT}$ signal output mode 2 (BLANK signal mask †)

† If the μPD72020 has started drawing operations in the display mode, the BLANK signal is not set to H.

DTE = 0. Operation is similar to the μPD7220A. The $\overline{DT}$ signal functions cannot be used. The LPEN/WAIT/$\overline{DT}$ pin performs the LPEN or WAIT functions.

The following two modes are available by setting CY1 or CY0 (table 6).

(1) GDC mode 0 operation is similar to the μPD7220A. When the RESET command is input, the μPD72020 is set to this mode.

(2) GDC mode 1 operation is similar to GDC mode 0 except if the μPD72020 starts drawing operations during the display period, the BLANK signal is not set to H even in the flash screen mode.

DTE = 1. The $\overline{DT}$ signal functions are enabled and the $\overline{DT}$ signal is output from the LPEN/WAIT/$\overline{DT}$ pin. The $\overline{DT}$ signal is used for display timing when the display memory consists of dual-port video RAMs. The VRAMs allow drawing during both drawing and display cycles.

When DTE is set to 1, the μPD72020 internally tracks the display address and outputs it and the $\overline{DT}$ signal under either of two conditions.

(1) At the start of every horizontal scan line (figure 3).

(2) When the lower 8 bits of the display address (DAD) internal counter are 0.

The starting display address should be set before setting DTE to 1. The μPD72020 will temporarily stop a drawing operation before issuance of the $\overline{DT}$ signal, as in the case of the μPD7220A WAIT function.

The $\overline{DT}$ signal output timing depends on the setting of the IM and DAD+2 bits of the SCROLL command. CY0 and CY1 determine which of the following three $\overline{DT}$ signal output modes is used.

Mode 0 With DTE = 1. In mode 0, the $\overline{DT}$ signal is output as shown in figure 4.

(1) At the start of every horizontal scan line.

(2) When the lower 8 bits of the DAD counter change from FEH or FFH to 00H.

Additionally, the $\overline{DT}$ signal active state in mode 0 has the following qualifications.

(1) $\overline{DT}$ may become active in succession; for example, when the DAD counter changes to 00H just after the start of a horizontal scan line as in figure 4C.

(2) When the lower 8 bits of the DAD counter become 00H in succession, $\overline{DT}$ becomes active during the first cycle only. See figure 4D.

(3) $\overline{DT}$ will not become active during HFP, HS, HBP, VFP, VS, or VBP periods.

Mode 1 With DTE = 1. In mode 1, the $\overline{DT}$ signal is ouput as shown in figure 5A.

(1) At the start of every horizontal scan line.

(2) When the lower 8 bits of the DAD counter change from FEH or FFH to 00H.

Additionally, the $\overline{DT}$ signal active state in mode 1 has the following qualifications.

(1) $\overline{DT}$ may become active in succession.

(2) When the lower 8 bits of the DAD counter change to 00H in succession, $\overline{DT}$ is active only during the first cycle.

(3) $\overline{DT}$ can become active during HFP, HS, HBP, VFP, VS, or VBP periods.

(4) $\overline{DT}$ will not become active while the DMA refresh operation is disabled (D-bit of SYNC command set to 1).

(5) $\overline{DT}$ becomes active every four cycles.

Mode 2 With DTE = 1. In mode 2, the $\overline{DT}$ signal output is the same as described for mode 1 except $\overline{DT}$ is active every eight cycles instead of every four cycles. See figure 5B.

3

Figure 3. $\overline{DT}$ Signal Output for Each Horizontal Line

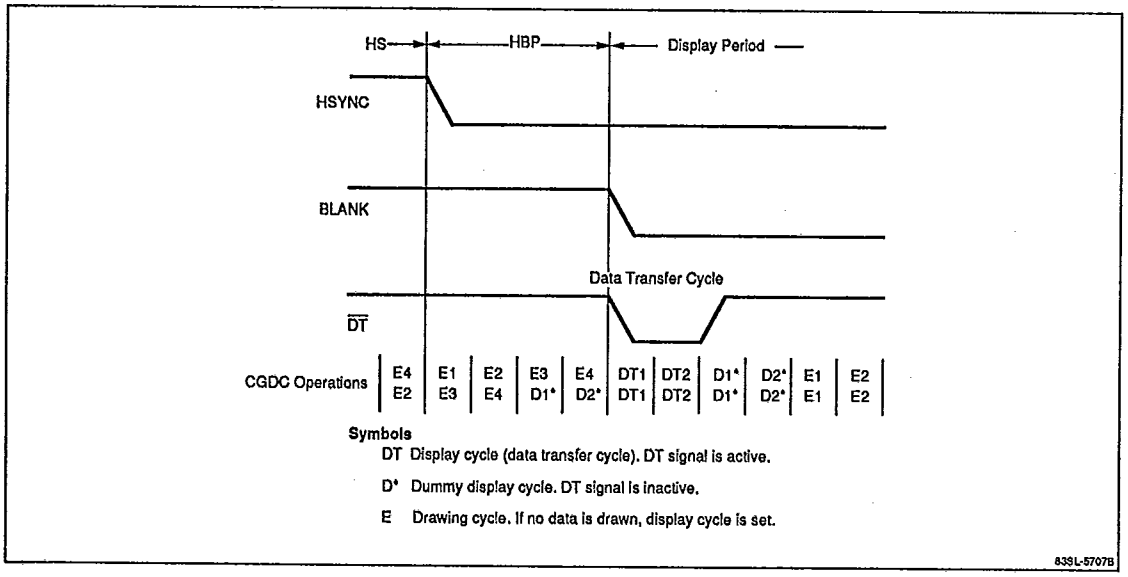
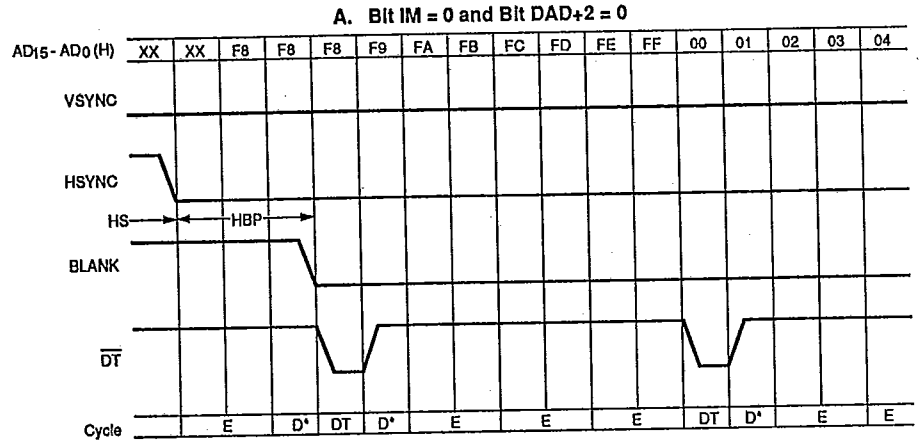
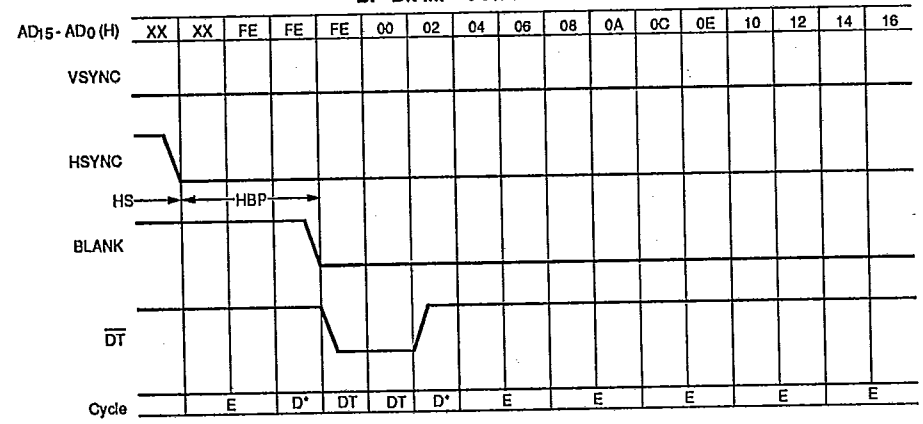


Figure 4. $\overline{DT}$ Signal Output, Mode 0 (Sheet 1 of 2)

A. Bit IM = 0 and Bit DAD+2 = 0



B. Bit IM = 0 and Bit DAD+2 = 1



Symbols

DT Display cycle (data transfer cycle). $\overline{DT}$ signal is active.

D* Dummy display cycle. $\overline{DT}$ signal is inactive.

E Drawing cycle. If no data is drawn, display cycle is set.

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Figure 4. $\overline{DT}$ Signal Output, Mode 0 (Sheet 2 of 2)

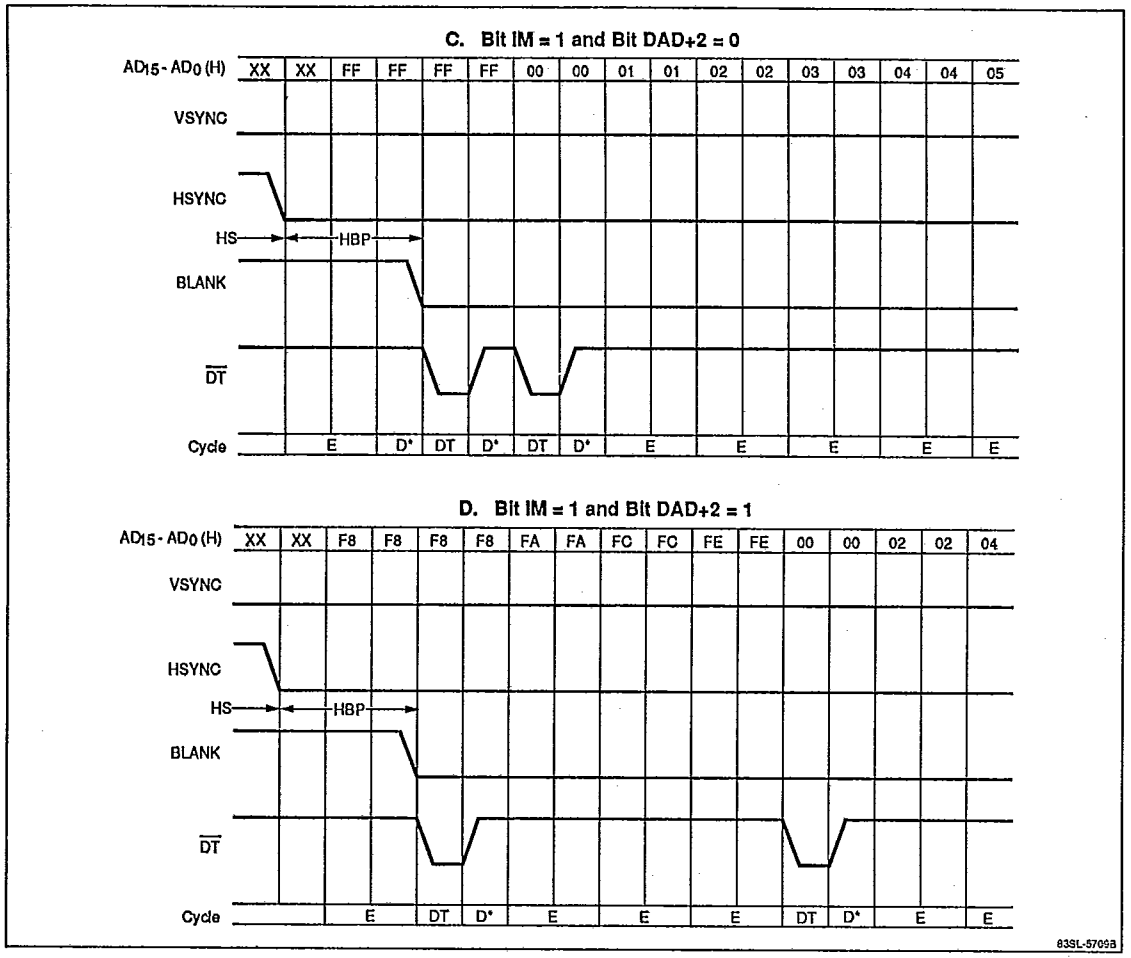

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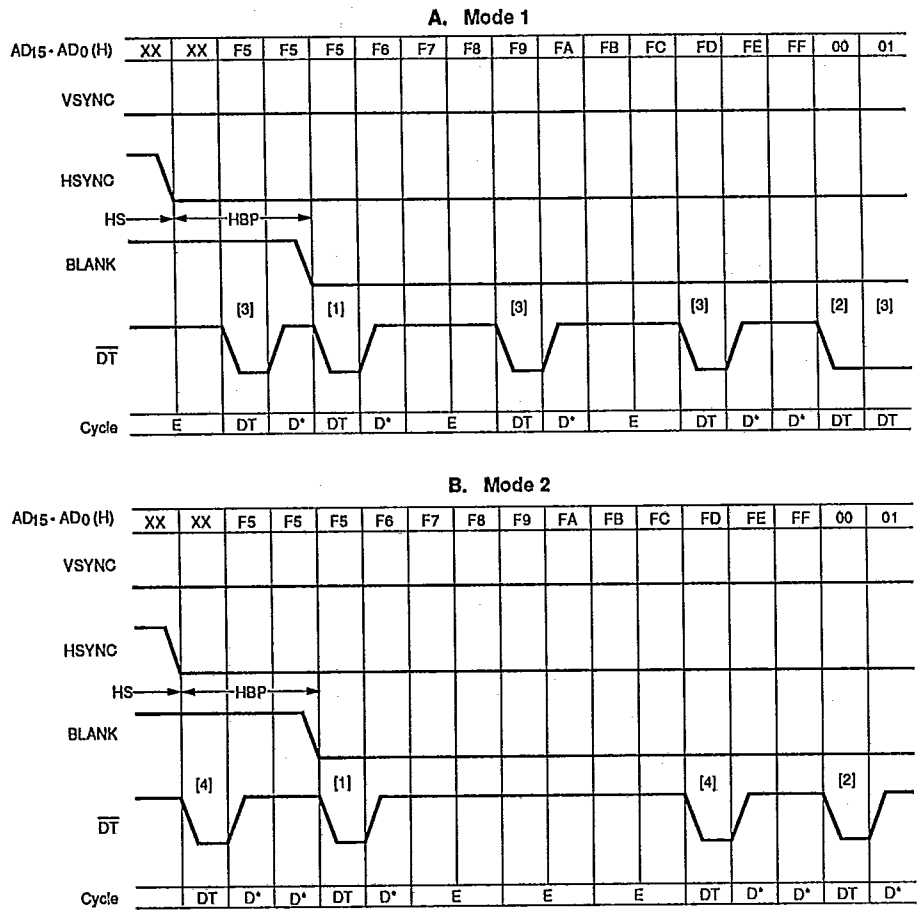
Figure 5. $\overline{DT}$ Signal Output, Mode 1 and Mode 2



Symbols

DT Display cycle (data transfer cycle). $\overline{DT}$ signal is active

D* Dummy display cycle. $\overline{DT}$ signal is inactive.

E Drawing cycle. If no data is drawn, display cycle is set.

[1] $\overline{DT}$ becomes active at display cycle start.

[2] $\overline{DT}$ becomes active when counting of the DAD lower 8 bits has terminated (FEH or FFH changes to 00H).

[3] $\overline{DT}$ becomes active every four cycles as controlled by counter that resets at diplay cycle start.

[4] $\overline{DT}$ becomes active every eight cycles.

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LPEN Command

When the address extension function is set by the WMASK command (with PN set to 1), the upper 2 bits of the light pen address (LAD) in the LPEN command are extended and a maximum of 20 bits can be used.

When PN = 0, the light pen address (LAD) is the same as with the μPD7220A.

The LPEN command format with the extended LAD is shown in figure 6.

Figure 6. LPEN Command Format

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	1	1	0	0	0	0	0	0
D1	LADL							
D2	LADM							
D3	X	X	X	X	LADH			

CSRW Command

When the address extension function is set by the WMASK command (with PN set to 1), the upper 2 bits of the drawing execution address (EAD) in the LPEN command are extended.

When PN = 0, the drawing execution address (EAD) is the same as with the μPD7220A.

Address extension causes the WG bits to be positioned differently in the character/graphics combined mode (character display/drawing) or the graphics mode.

The CSRW command formats are included in table 4.

CSRR Command

When the address extension function is set by the WMASK command (with PN set to 1), the upper 2 bits of the drawing execution address (EAD) in the LPEN command are extended and a maximum of 20 bits can be used.

When PN = 0, the drawing execution address (EAD) is the same as with the μPD7220A.

The CSRR command format with the extended EAD is shown in figure 7.

Figure 7. CSRR Command Format

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	1	1	1	0	0	0	0	0
D1	EADL							
D2	EADM							
D3	X	X	X	X	EADH			
D4	dADL							
D5	dADH							

SCROLL Command

When the address extension function is set by the WMASK command (with PN set to 1), the upper 2 bits of the display start address (SAD) in the SCROLL command are extended.

When PN = 0, the display start address (SAD) is the same as with the μPD7220A.

The SCROLL command format is shown in figure 8. The built-in RAM map with the extended SAD is included in table 4.

Figure 8. SCROLL Command Format

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	0	1	1	1	RA			

Absolute Maximum Ratings

T_A = +25°C

Supply voltage, V_{DD}	−0.5 to +7.0 V
Input voltage, V_I	−0.5 to V_{DD} + 0.3 V
Output voltage, V_O	−0.5 to V_{DD} + 0.3 V
Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage.

DC Characteristics

T_A = −10 to +70°C; V_{DD} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Conditions
Low-level input voltage	V_{IL}	−0.5	0.8	V	Except 2xCCLK
		−0.5	0.6	V	2xCCLK
High-level input voltage	V_{IH}	2.2	V_{CC} + 0.5	V	Except 2xCCLK, $\overline{WR}$
		3.5	V_{CC} + 0.5	V	2xCCLK
		2.5	V_{CC} + 0.5	V	$\overline{WR}$
Low-level output voltage	V_{OL}		0.45	V	I_{OL} = 2.2 mA
High-level output voltage	V_{OH}	0.7 V_{DD}		V	I_{OH} = −400 μA
Low-level input leakage current	I_{LIL}		−10	μA	V_I = 0 V; except VSYNC, $\overline{DACK}$
			−500	μA	V_I = 0 V; VSYNC, $\overline{DACK}$
High-level input leakage current	I_{LIH}		10	μA	V_I = V_{DD}; except LPEN/WAIT/$\overline{DT}$
			500	μA	V_I = V_{DD}; LPEN/WAIT/$\overline{DT}$
Low-level output leakage current	I_{LOL}		−10	μA	V_O = 0 V
High-level output leakage current	I_{LOH}		10	μA	V_O = V_{DD}
Supply current	I_{CC}		70	mA	

Capacitance

T_A = +25°C; V_{DD} = GND = 0 V

Item	Symbol	Min	Max	Unit	Condition
Input	C_I		15	pF	f = 1 MHz; 0 V except for tested pin
Output	C_O		20	pF	
Input/output	$C_{I/O}$		20	pF	
Clock input	C_C		20	pF	

AC Characteristics

T_A = −10 to +70°C; V_{DD} = +5.0 V ±10%

Item	Symbol	Min	Max	Unit	Conditions
Clock 2xCCLK					
Clock cycle	t_{CY}	125	10,000	ns	
High-level clock width	t_{CH}	52		ns	
Low-level clock width	t_{CL}	52		ns	
Clock rise time	t_{CR}		15	ns	
Clock fall time	t_{CF}		15	ns	
Read Cycle					
Address setup time to $\overline{RD}$ ↓	t_{AR}	0		ns	
Address hold time from $\overline{RD}$ ↑	t_{RA}	0		ns	
$\overline{RD}$ pulse width	t_{RR1}	t_{RD1} +20		ns	
Data output delay time from $\overline{RD}$ ↓	t_{RD1}		55	ns	C_L = 50 pF
Data float delay time from $\overline{RD}$ ↑	t_{DF}	0	55	ns	
$\overline{RD}$ pulse cycle	t_{RCY}	4.5 t_{CY}		ns	DE = 0
		12 t_{CY}		ns	DE = 1
$\overline{RD}$ recovery time	t_{RV}	2 t_{CY}		ns	Also valid in DMA cycle
Write Cycle					
Address setup time to $\overline{WR}$ ↓	t_{AW}	0		ns	
Address hold time from $\overline{WR}$ ↑	t_{WA}	10		ns	
$\overline{WR}$ pulse width	t_{WW}	60		ns	
Data setup time to $\overline{WR}$ ↑	t_{DW}	45		ns	
Data hold time from $\overline{WR}$ ↑	t_{WD}	10		ns	
$\overline{WR}$ pulse cycle	t_{WCY}	4.5 t_{CY}		ns	
$\overline{WR}$ recovery time	t_{RV}	2 t_{CY}		ns	Also valid in DMA cycle
DMA Read Cycle					
$\overline{DACK}$ setup time to $\overline{RD}$ ↓	t_{AKR}	0		ns	
$\overline{DACK}$ hold time from $\overline{RD}$ ↑	t_{RAK}	0		ns	
$\overline{RD}$ pulse width	t_{RR2}	t_{RD2} +20		ns	
Data output delay time from $\overline{RD}$ ↓	t_{RD2}		2 t_{CY} +60	ns	C_L = 50 pF

AC Characteristics (cont)

T_A = −10 to +70°C; V_{DD} = +5.0 V ±10%

Item	Symbol	Min	Max	Unit	Conditions
DMA Read Cycle(cont)					
DREQ output delay time from 2xCCLK ↑	t_{CRQ}		75	ns	C_L = 50 pF
DREQ setup time to $\overline{DACK}$ ↓	t_{RQAK}	0		ns	
DREQ ↓ delay time from $\overline{DACK}$ ↓	t_{AKRQ}		1.5 t_{CY} + 80	ns	C_L = 50 pF
$\overline{DACK}$ pulse cycle	t_{AKCY}	4.5 t_{CY}		ns	See Note.
High-level $\overline{DACK}$ width	t_{AKH}	t_{CY}		ns	
Low-level $\overline{DACK}$ width	t_{AKL}	2.5 t_{CY}		ns	
DMA Write Cycle					
$\overline{DACK}$ setup time to $\overline{WR}$ ↓	t_{AKW}	0		ns	
$\overline{DACK}$ hold time from $\overline{WR}$ ↑	t_{WAK}	0		ns	
Read/Modify/Write Cycle					
Address/data delay time from 2xCCLK ↑	t_{CA}	15	80	ns	C_L = 50 pF
Address/data float delay time from 2xCCLK ↑	t_{CAF}	15	80	ns	C_L = 50 pF
Data setup time to 2xCCLK ↓	t_{DC}	0		ns	
Data hold time from 2xCCLK ↓	t_{CDF}	t_{CBI}		ns	
$\overline{DBIN}$ delay time from 2xCCLK ↓	t_{CBI}	15	60	ns	C_L = 50 pF
$\overline{RAS}$ ↑ delay time from 2xCCLK	t_{CRSH}	15	60	ns	C_L = 50 pF
$\overline{RAS}$ ↑ delay time from 2xCCLK ↓	t_{CRSL}	15	50	ns	C_L = 50 pF
High-level $\overline{RAS}$ width	t_{RSH}	1/3 t_{CY}		ns	
Low-level $\overline{RAS}$ width	t_{RSL}	1.5 t_{CY} − 30		ns	
Address setup time to $\overline{ARSL}$ ↓	t_{ARSL}	30		ns	
Display Cycle					
Output signal delay time from 2xCCLK ↑	t_{CO}		70	ns	C_L = 50 pF

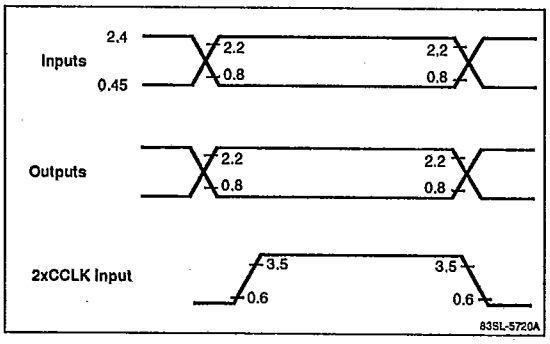
AC Characteristics (cont)

T_A = −10 to +70°C; V_{DD} = +5.0 V ±10%

Item	Symbol	Min	Max	Unit	Conditions
Input Cycle					
Input signal setup time to 2xCCLK ↑	t_{PC}	10		ns	
Input signal pulse width	t_{PP}	t_{CY}		ns	

Note: Performs two-dimensional rectangular area assignment whereby the dc parameter is set to other than 0. When byte-by-byte transfer is specified, the value is 5.5 t_{CY}.

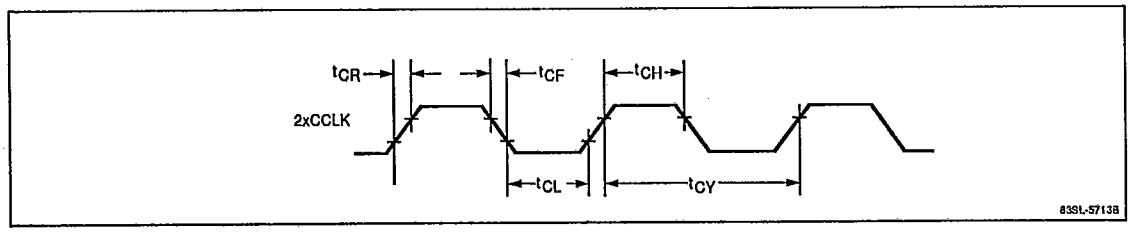
Voltage Thresholds for Timing Measurements



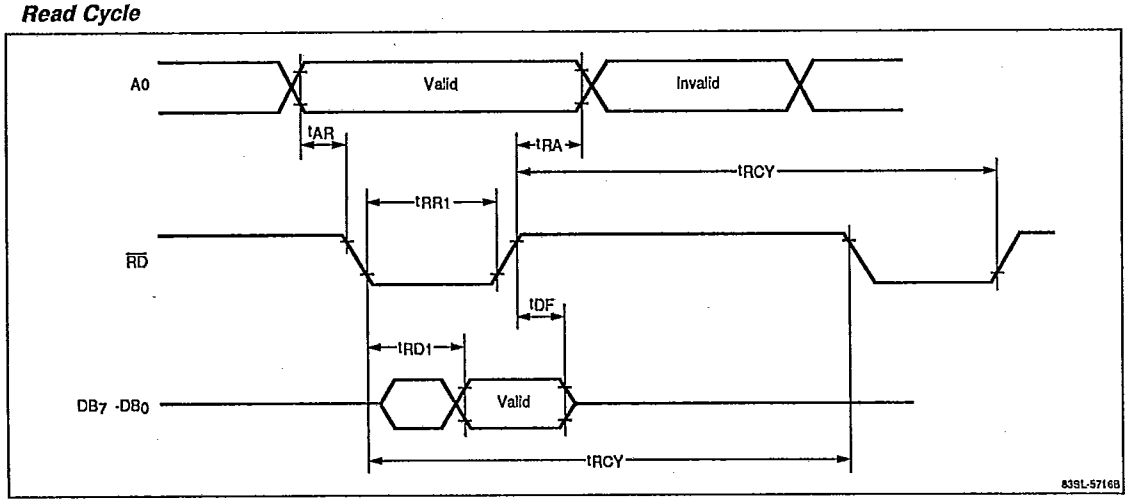
3

Timing Waveforms

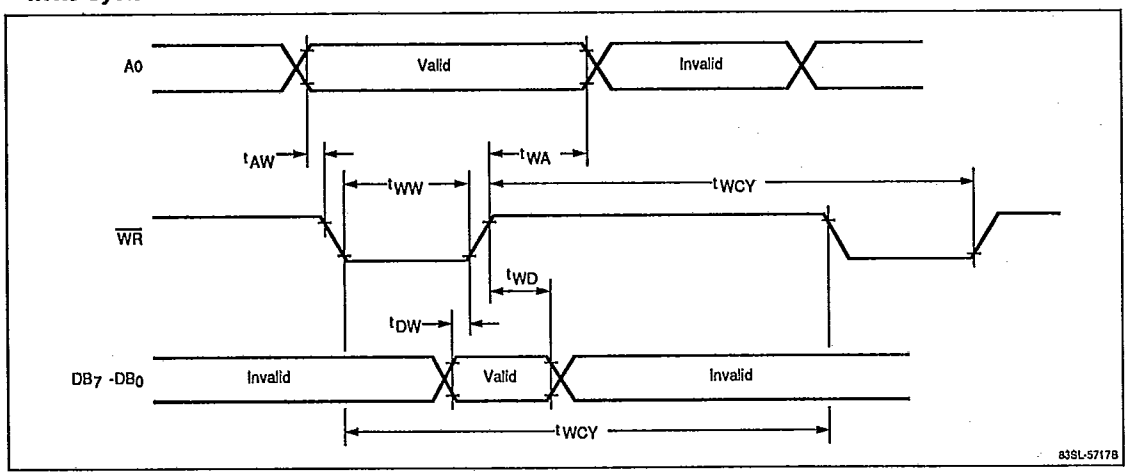
Clock 2xCCLK



Read Cycle

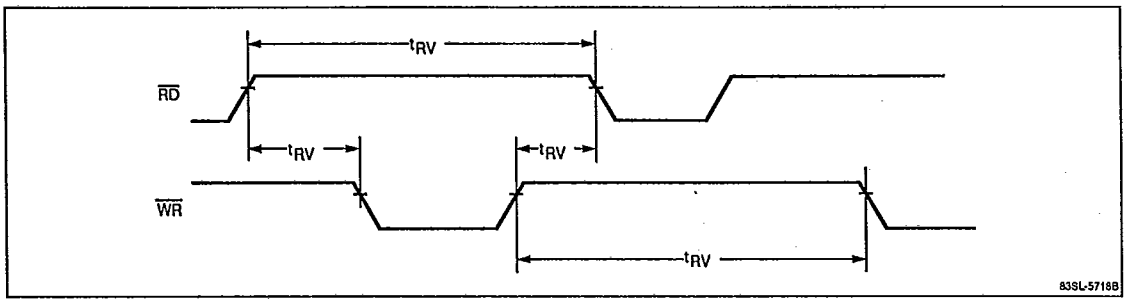


Write Cycle

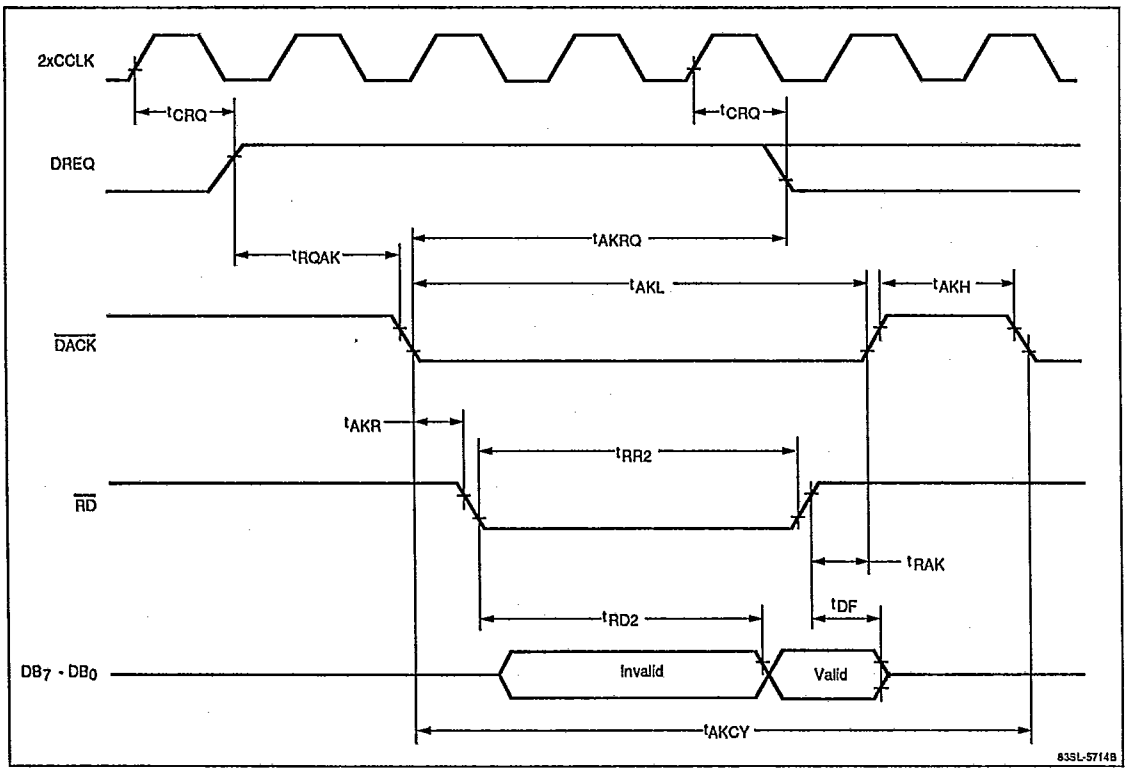


Timing Waveforms (cont)

Read/Write Recovery



DMA Read Cycle



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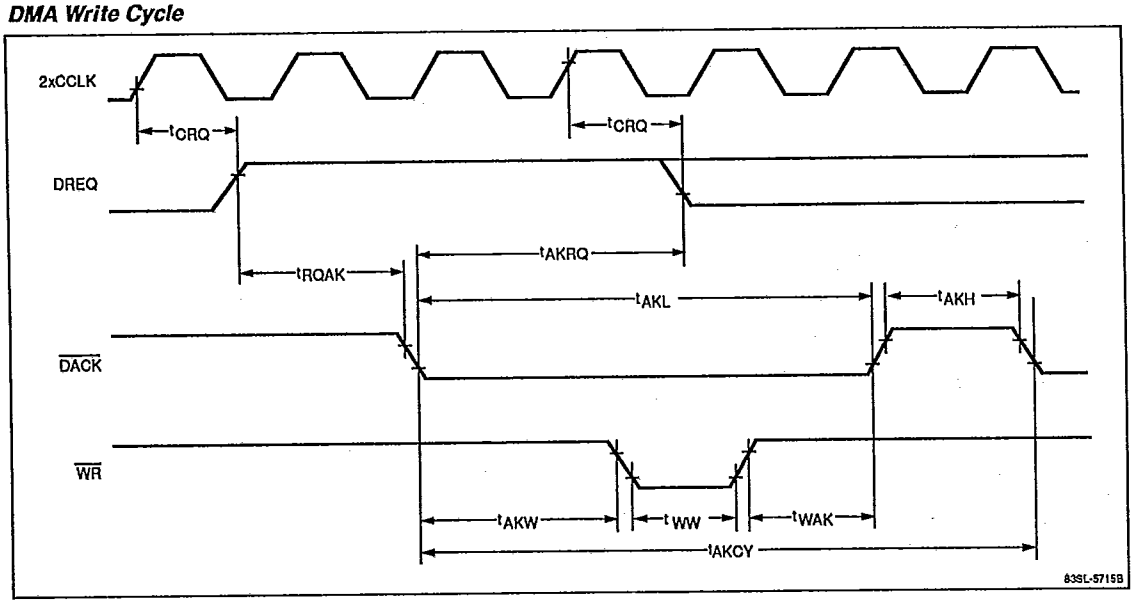
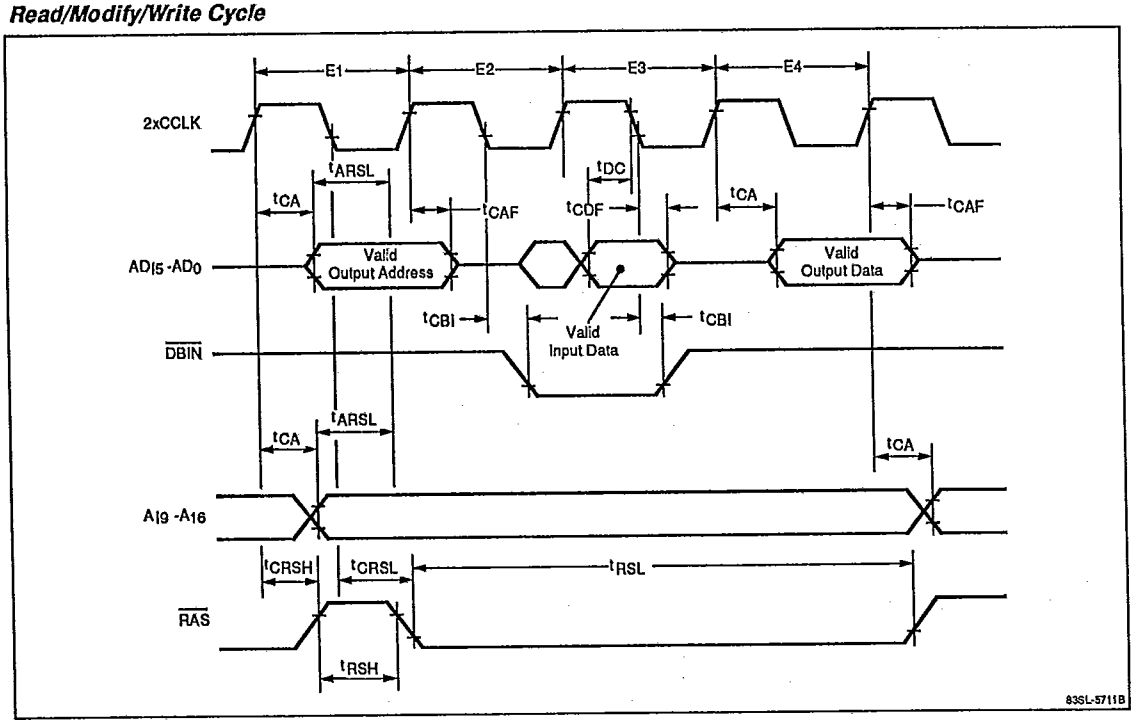
Timing Waveforms (cont)

DMA Write Cycle



Read/Modify/Write Cycle



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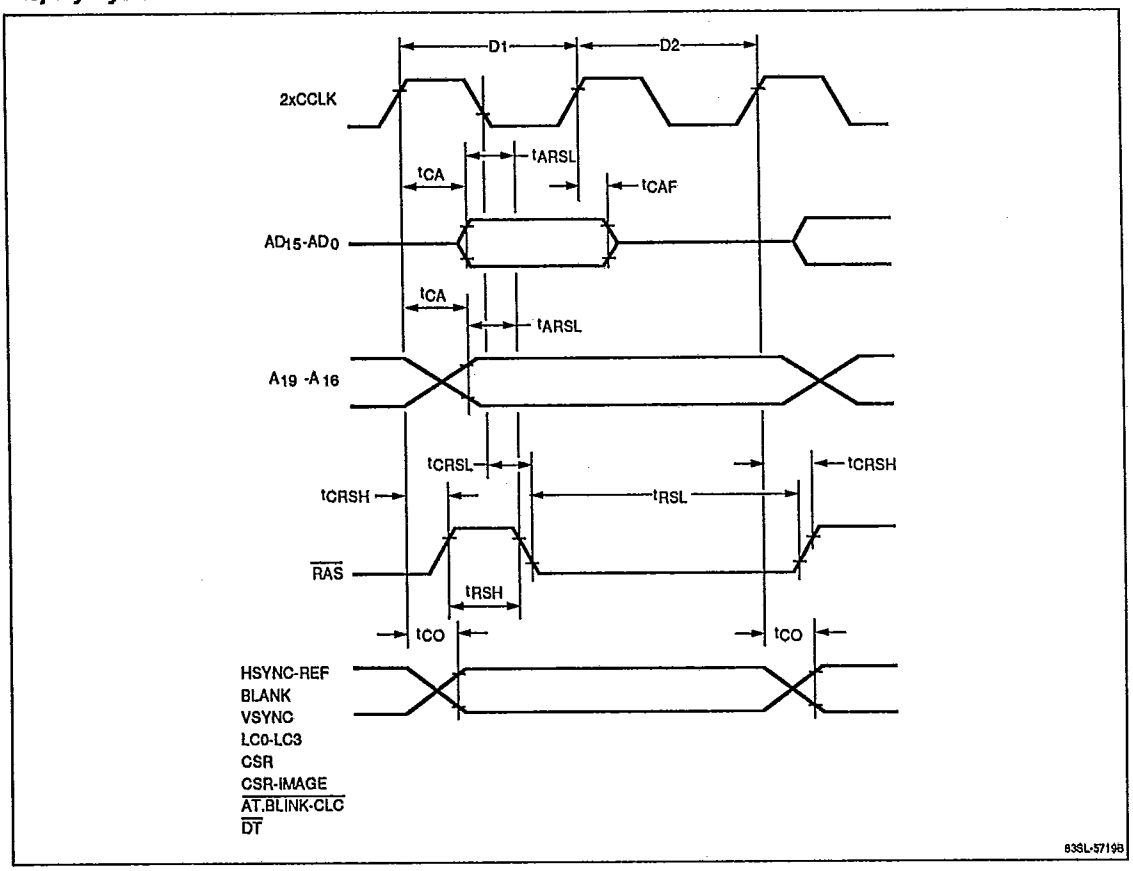
Timing Waveforms (cont)

Display Cycle



Input Cycle