CHAPTER 3
OPTION
(PRINCIPLES OF OPERATIONS)

3.1 Microcassette

The microcassette tape is controlled by the 6303 slave CPU. The unit requires a comparatively large power supply because of the mechanical functions it performs. It is powered only when used. Fig. 3-1 is a block diagram illustrating signal flow to and from the microcassette.

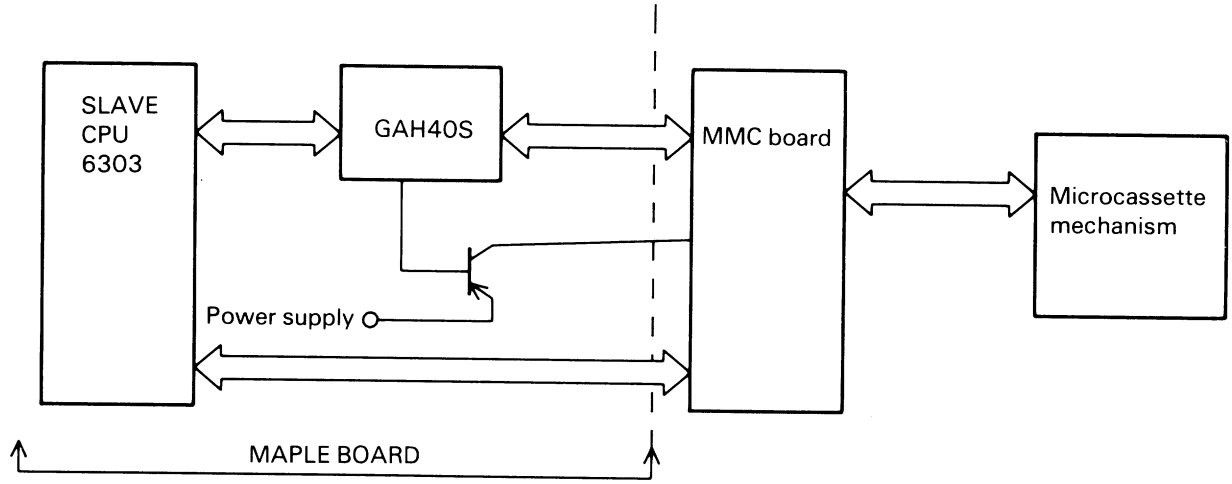


Fig. 3-1 Microcassette Tape Operation Control Block Diagram

3.1.1 Slave CPU Functions

The 6303 slave CPU directly controls all microcassette tape operations using the following signals:

- HSW: Indicates the current position of the read/write head (LOAD/ UNLOAD).
- WE: Indicates whether the microcassette is write-enabled.
  (detects the presence of the microcassette write inhibit tab).
- ERAH: Erase signal.
- HMT: Head pinch motor drive signal.
- D: Write data.

3.1.2 Gate Array Functions

The gate array issues or accepts the following signals under the control of the slave CPU:

MTA – MTC: Capstan motor drive control signal
CNTR: Tape count detection signal (photo-reflector detection signal)
RDMC: Read data
SWMC: MMC board and mechanism operation power control signal

3.1.3 Microcassette Tape Data Format

Data are recorded on a microcassette tape in blocks of 256 bytes and all cassette tapes are accessed in blocks. Fig. 3-2 illustrates the structure of a data block.

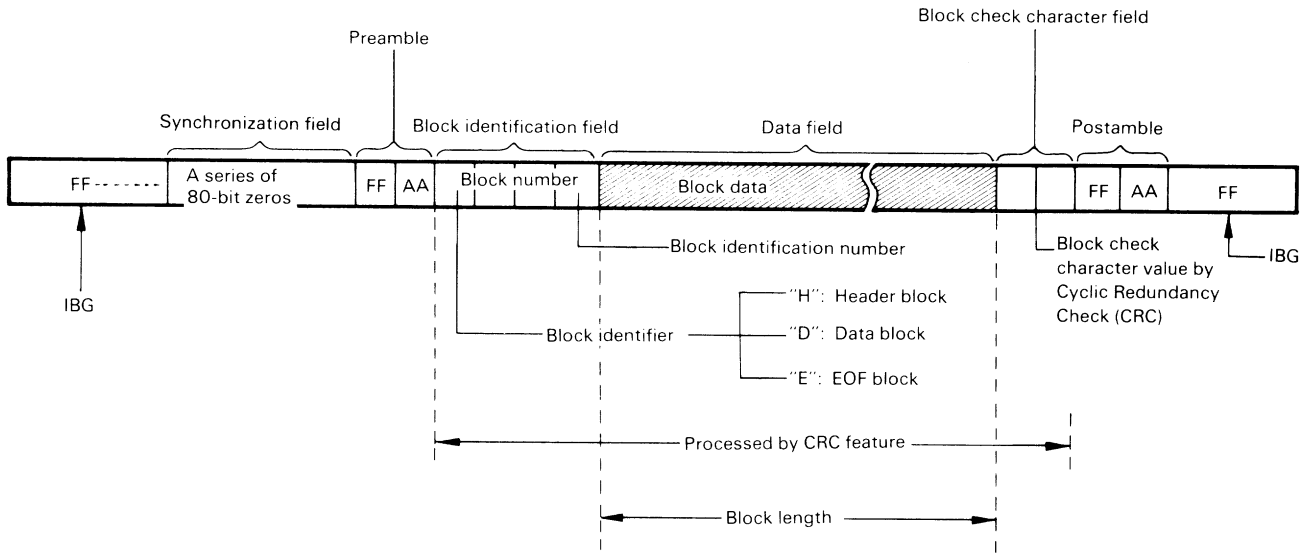


Fig. 3-2 Microcassette Tape Data Format

One tape reel (or one tape volume) consists of a directory and one or more files. The directory consists of three blocks; the first block contains identification data for the tape and directory and the second and third blocks contain control data for the files.

One file consists of a header block, one or more data blocks, and an end-of-file (EOF) block. Fig. 3-3 illustrates the general data structure of one reel.

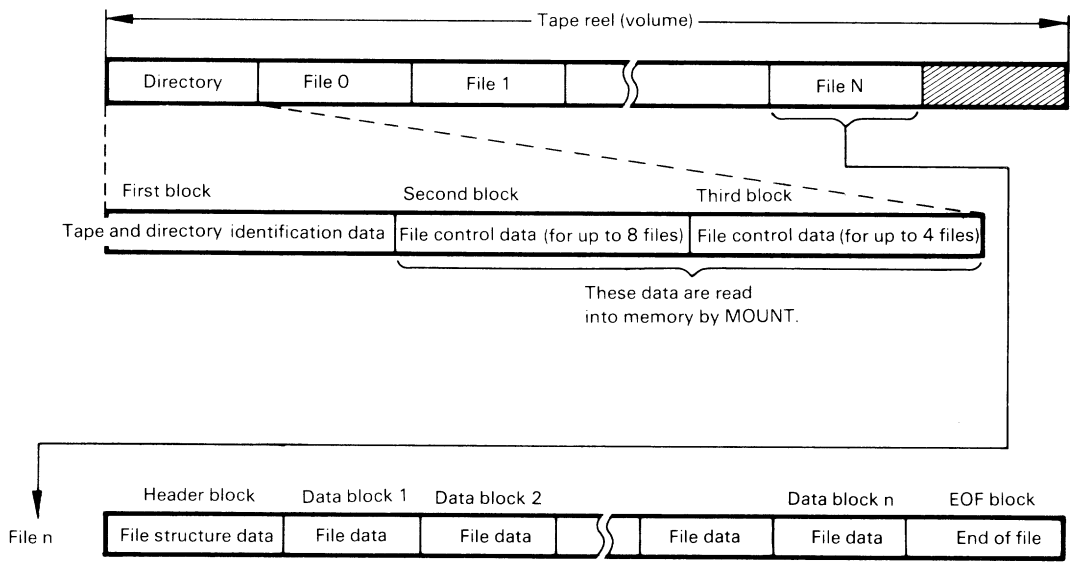


Fig. 3-3 Cassette Tape Reel Structure

3.1.4 Outline of Microcassette Mechanism

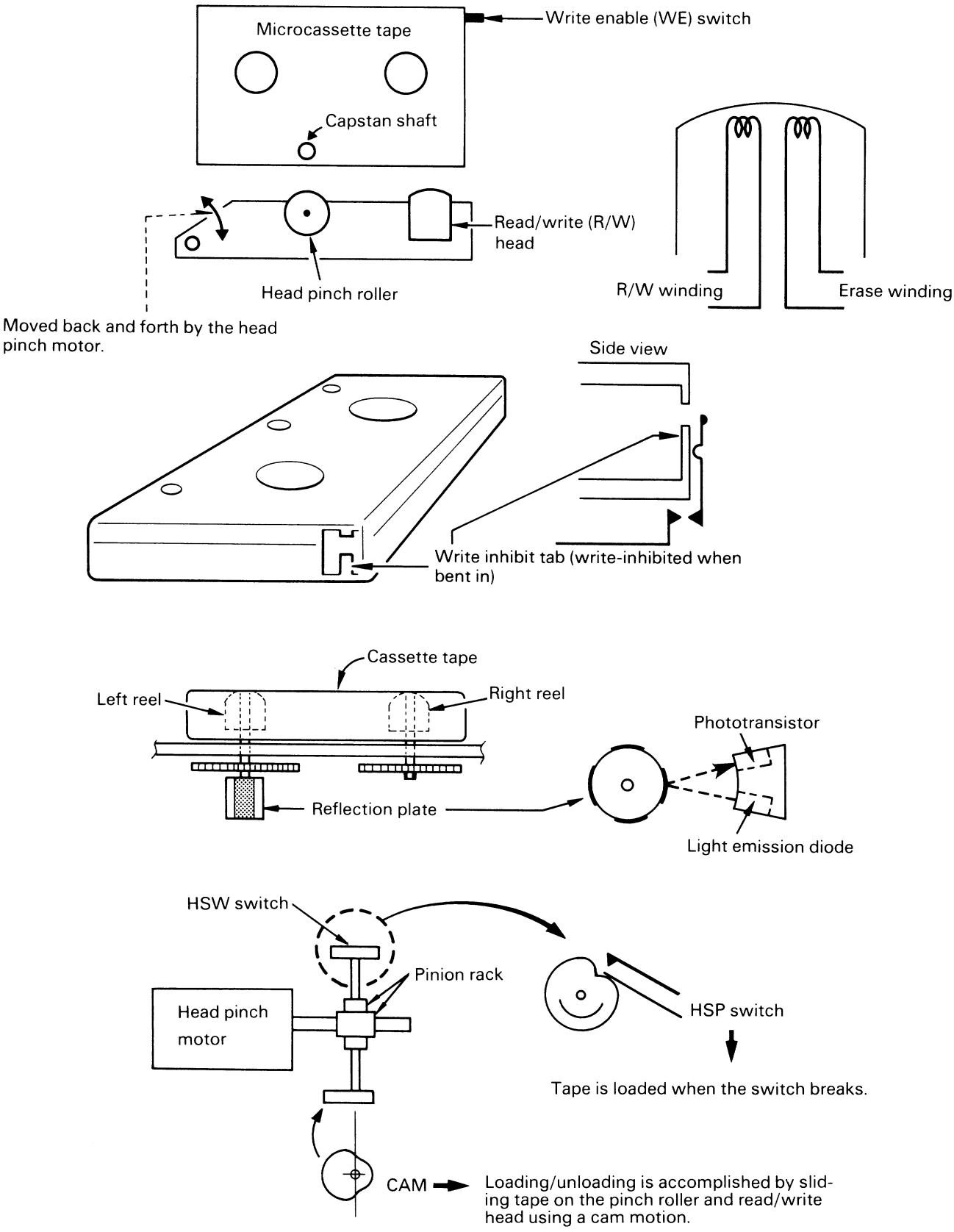


Fig. 3-4

3.1.5 MMC Board

The MMC board consists of two major sections, the motor drive control and read/write, which provide the following functions:

3.1.5.1 Motor Control Section

The motor control section occupies the upper half of the MMC board and controls the capstan motor and head pinch motor drive, and tape count detection. The individual circuits are discussed in the following:

(1) Capstan motor drive circuit

This circuit uses two ICs: IC1 and IC2. IC1 controls motor drive circuit switching and IC2 controls motor revolution speed.

- Motor drive circuit

Fig. 3-5 shows the internal circuit of IC1.

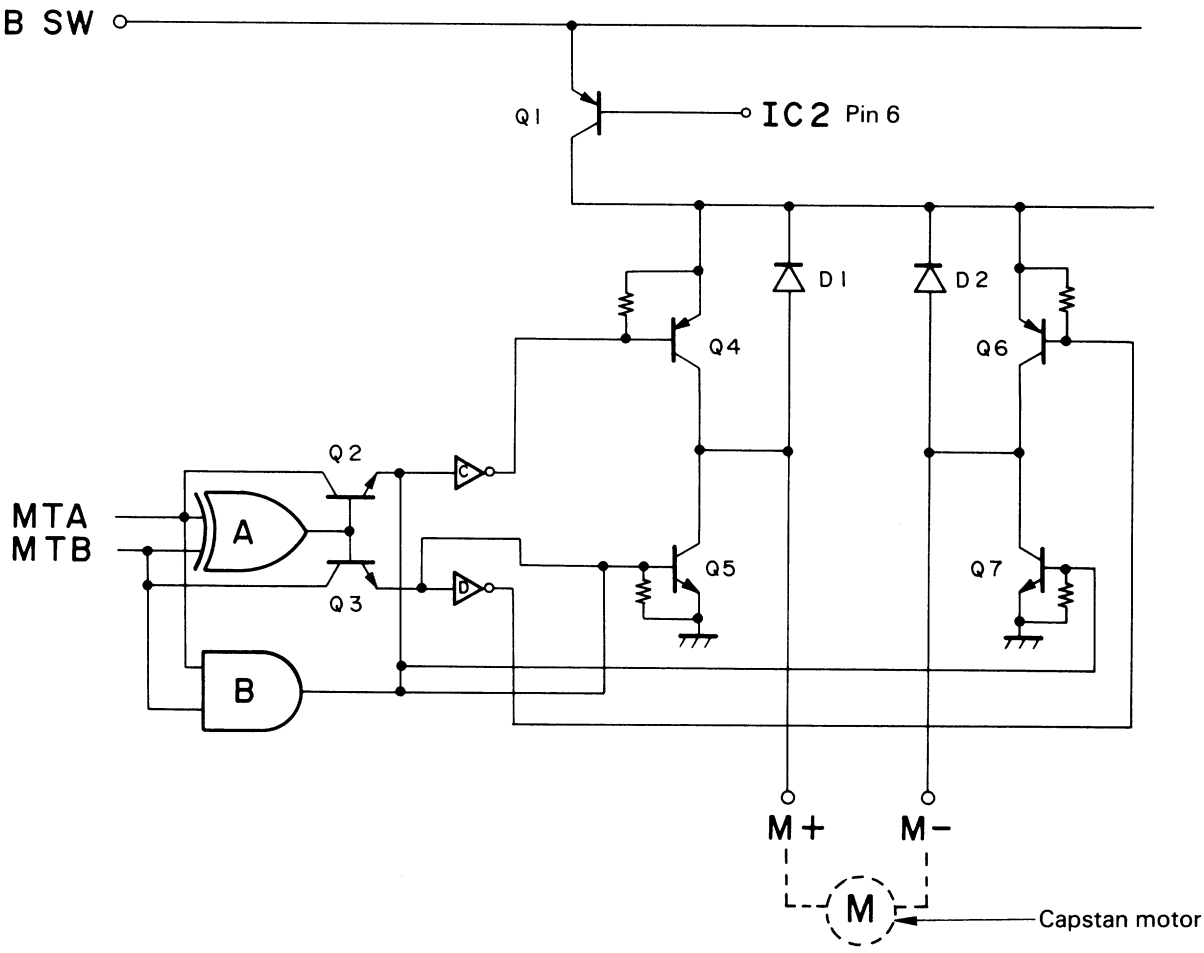


Fig. 3-5 Motor Drive IC Circuit

The circuit switches the polarity of the voltage applied to the capstan motor. Simplified circuit descriptions follow. While the actual circuit operation is more complicated, the basic operation is the same.

Table 3-1 Cassette Tape Operation Truth Table

Operation	MTC	MTB	MTA	Erase Head	Head Position
READ (Replay)	0	0	1	0	Load
WRITE (REC)	0	0	1	1	Load
REWIND (FAST)	1	1	0	0	Unload
REWIND (SLOW)	0	1	0	0	Unload
F.F. (FAST)	1	0	1	0	Unload
F.F. (SLOW)	0	0	1	0	Unload

MTA = High, MTB = Low

Since both the signals are supplied to the exclusive OR gate A, the base of the transistors Q2 and Q3 are held high, maintaining them in conduction. This causes the emitter of Q2 to be held high which in turn maintains transistor Q7 in conduction, holding the M- terminal of the capstan motor at ground level. The low signal inverted by inverter C turns transistor Q4 on which drives the external transistor Q1, supplying the VBSW voltage to the M+ terminal of the capstan motor. This results in a forward capstan motor drive which winds the tape. (The motor control transistors Q4 and A7 are in conduction.)

MTA = Low, MTB = High

Both Q2 and Q3 are in conduction similare to the above phase. However, the high level at the collector of Q3 maintains the transistor in conduction this time, causing the the M+ terminal of the capstan motor to be held at ground level. The low signal inverted by inverter D turns transistor Q6 and supplies the VBSW voltage to the M– terminal. This results in a backward capstan motor drive, which rewinds the tape. (The motor control transistors, Q5 and Q6, are in conduction.)

MTA = High, MTB = High

When both the signals are high, the low output of the exclusive OR gate A cuts off transistors Q2 and Q3, and no effective control signal can be output at the emitter of either transistor, but the high level output of AND gate B maintains transistors Q5 and Q7 in conduction, holding both the M+ and M– terminals of the capstan motor at ground level. (The motor control transistors Q5 and Q7 are in conduction.)

MTA = Low, MTB = Low

Both the outputs of the exclusive OR gate A and the AND gate B are low; no control signal is available. All the motor control transistors, Q4 through Q7, are cut off, leaving the capstan motor in a floating state.

The external transistor Q1 is controlled by the output at pin 6 of IC2 (a speed control signal). Thus, the VBSW voltage may not be supplied to the capstan motor if either Q4 or Q6 is in conduction.

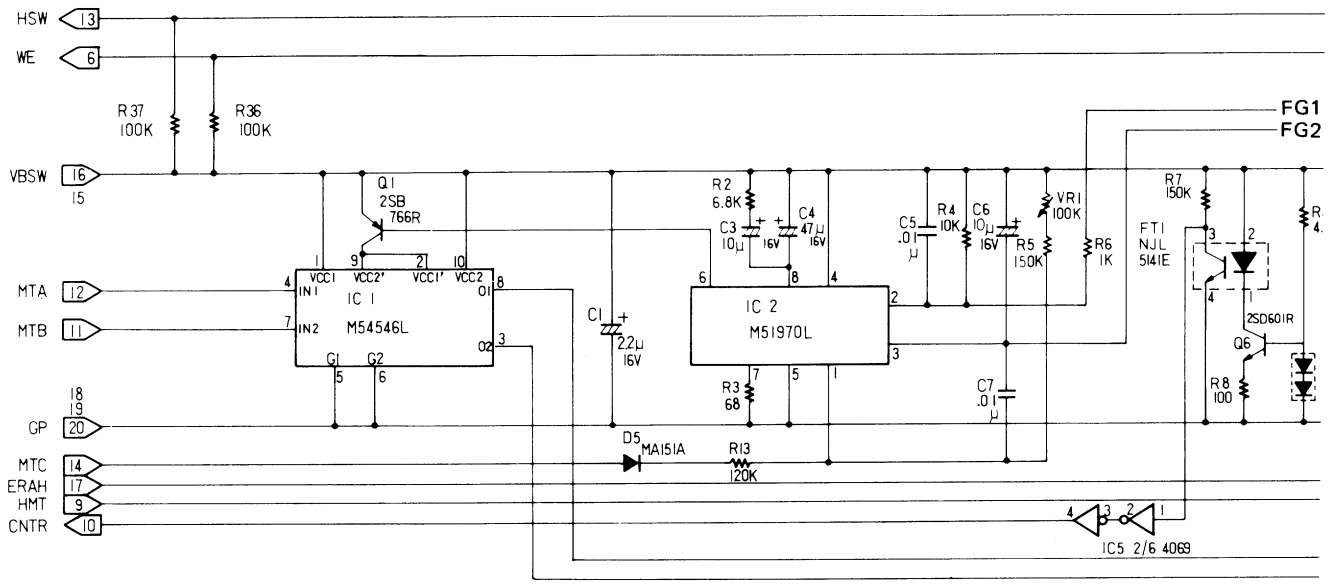


Fig. 3-6

3.1.5.2 Motor Revolution Speed Control Circuit

This circuit controls revolution of the capstan motor to ensure a cassette tape feed at a constant speed. Tape must be read/written at a speed of 2.4 cm/s. To secure this tape speed, the capstan motor must revolve at 2,400 rpm.

Because no tape speed control is desired during fast forward feed or rewind, a function which can enable or disable the tape speed control is also required. Fig. 3-7 is a block diagram of the internal circuit of IC2.

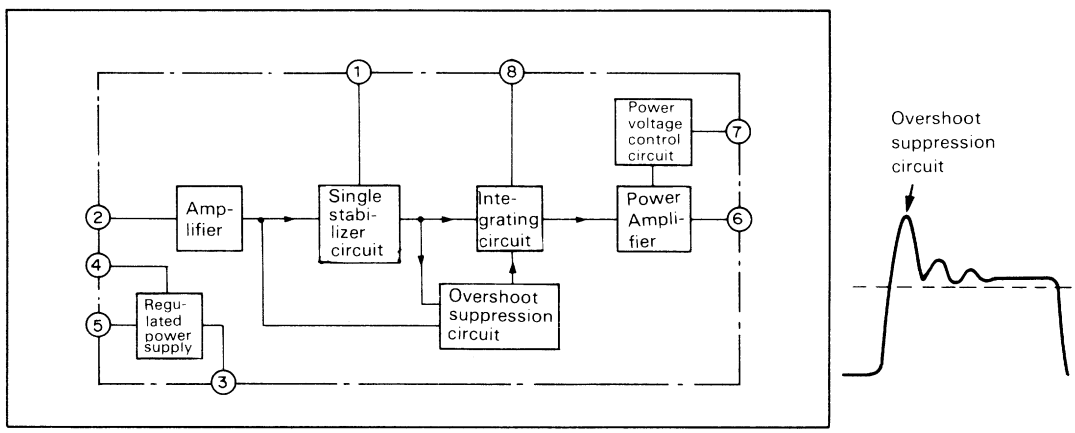


Fig. 3-7 IC2 Internal Circuit Block Diagram

The principle of the motor speed control can be illustrated by Fig. 3-8.

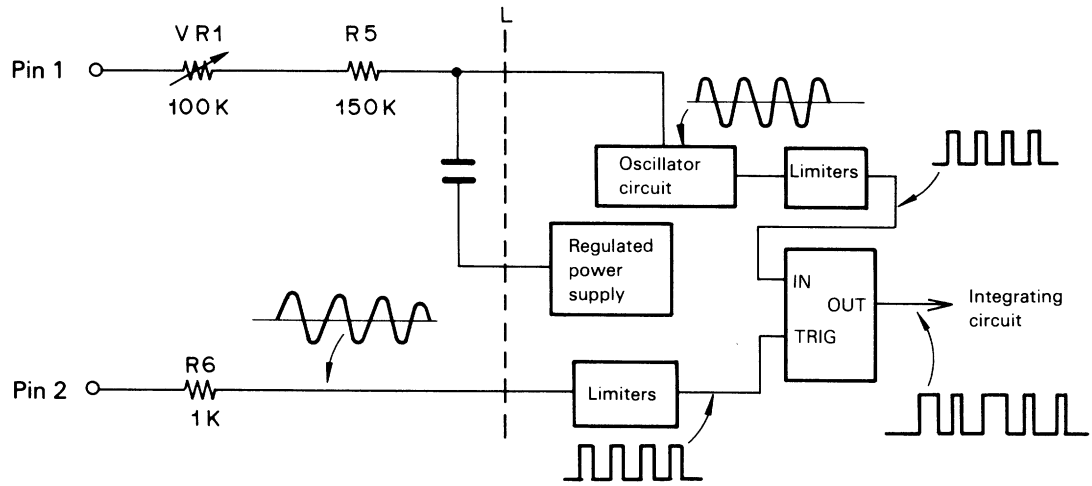


Fig. 3-8 Motor Speed Control Circuitry

Integrating Circuit

The IC output is a pulse signal as shown in Fig. 3-9. However, the capstan motor cannot be controlled by a pulse signal as the motor would oscillate. The IC output is integrated by the next stage integrating circuit, which uses the external capacitors C3 and C4. The pulse delay time (t) is determined by the capacitance of C4.

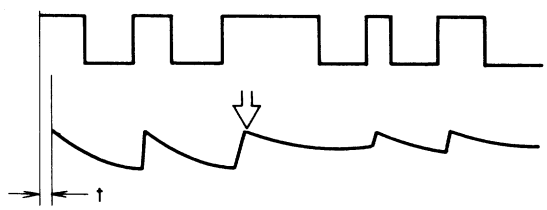


Fig. 3-9 Integrating Circuit

Current Control

The output current from the integrating circuit is amplified and the amplified current is limited to a proper value by the external resistor R3. Fig. 3-10 conceptually illustrates the principle.

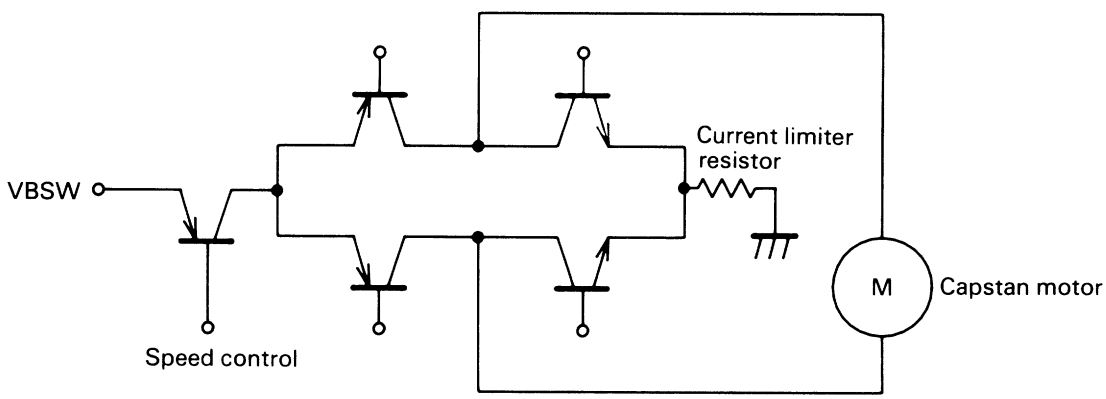


Fig. 3-10

3.1.5.3 Power Supply

Because IC 2 requires a negative voltage supply, pin 5 is grounded and pin 4 is connected to the VBSW voltage.

Input – Monostable Circuit

Motor speed control is accomplished by comparing the time constant determined by VR1, R5, and C7 with the frequency fed back from the capstan motor tachogenerator. The relationship between the time constant and the rpm of the capstan motor is as follows:

$$NP = \frac{1}{1.17Rx\ C7}$$

$$2400 \cdot 10 = \frac{1}{1.17Rx \cdot 0.01}$$

$$Rx = \frac{24 \times 10^3}{1.17 \times 0.01} \text{ ..... Approximately 205 k}\Omega$$

where N: rpm of capstan motor – 2,400 rpm
P: Number of tachogenerator poles – 10
Rx: Total resistance of VR1 and R5 (kohms)
C7: 0.01 uF (pF)

The specified speed should be attained by adjusting VR1 nearly at the center. The optimum frequency output from the tachogenerator, 400 Hz, is deviced as follows:

$$\frac{2{,}400 \text{ rpm}}{60} \times 10 \text{ (poles)} = 400 \text{ Hz}$$

3.1.6 Mechanism Control

3.1.6.1 Tape Count Detection

Tape count detection is accomplished by mirrors directly coupled to the left reel (the reel taking up tape during read/write) and a photo-reflector assembly (a single element which is a combination of a light emission diode and a phototransistor). Fig. 3-11 shows the circuit and the positional relationship between the elements.

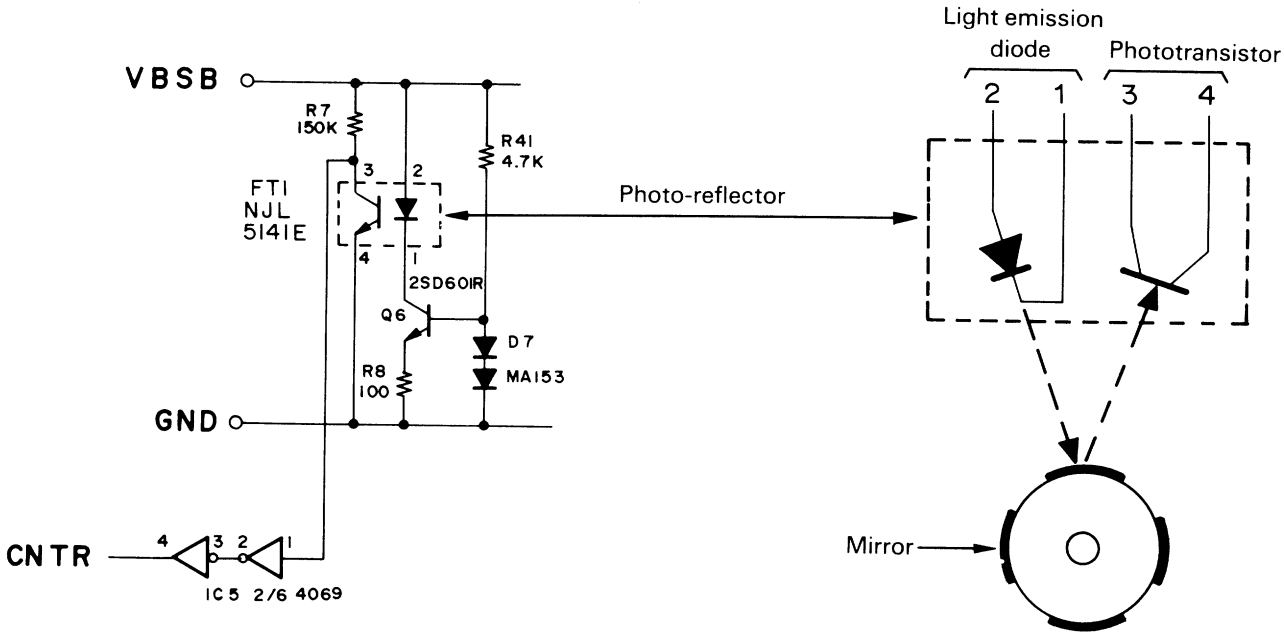


Fig. 3-11 Tape Count Detector Circuit and Positional Relationship between Elements

The reflector drum has four mirrors on it as shown in Fig. 3-11. One reel revolution is counted as four.

3.1.6.2 Head Pinch Motor Control

The head pinch motor moves the P-lever assembly consisting of the pinch roller and the read/write head. The assembly slides back and forth to accomplish tape loading and unloading. This motor always revolves in a direction and drives two cams; one is used to move the P-lever assembly back and forth and the other makes and breaks thc HSW switch, which detects the read/write head position. Fig. 3-12 shows the control circuit.

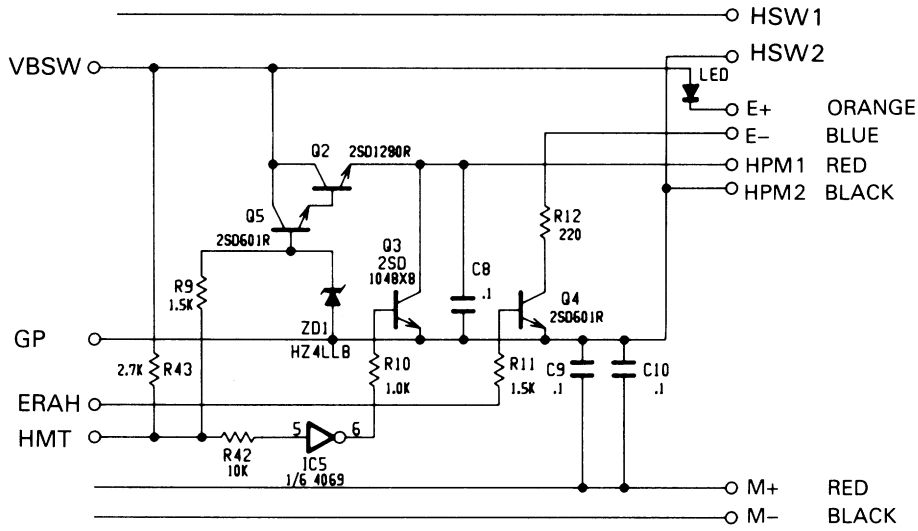


Fig. 3-12 Head Pinch Motor Control Circuit

When the HMT signal goes high, the transistors Q5 and Q2 are turned on and the VBSW voltage is supplied to HPM1 (the positive side terminal of the motor), revolving the motor which in turn causes the P-lever assembly to move back and forth.

When the HMT signal is turned low to stop the motor, the output of IC5 turns off and the output of pin 6 goes high, turns off transistors Q5, Q2, and turns on Q3. This causes the HPM1 line to be shorted to ground, and applies a brake to the motor, preventing revolution by inertia. If the motor continued revolving by inertia, the read/write head position and the pinch roller's contacting pressure against the capstan shaft would deviate from the specifications, and such failures as read/write error would occur.

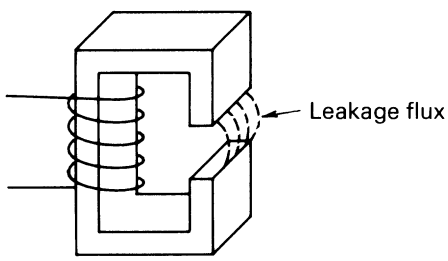
The zener diode ZD1, connected at the base of Q5 maintains the voltage supplied to the motor below the VBSW voltage (approximately 5V). – (A higher motor drive voltage would increase the motor inertia as described above.)

3.1.6.3. Erase Circuit

When the ERAH signal is activated low, transistor Q3 is turned on. This causes a current from the VBSW line to ground passing through the erase winding of the read/write head, and erasing previously written tape data. This circuit operates only during write.

Read/Write Head Structure

Both the read/write and erase heads make use of leakage flux.



Data are actually written on the tape at the copre slit where leakage flux is generate.

Fig.3-13 Read/Write Head Structure

3.1.7 Read/Write Control Section

The read/write control is located in the lower half of the MMC board and consists of a read and write circuit. However, most of the section is actually occupied by the read circuit operational amplifier.

3.1.7.1 Write Circuit (Erase and Write)

Magnetic tape write is accomplished using leakage flux as illustrated above. A logical value of 0 or 1 can be written on reversing tape by reversing the direction of the flux; i.e., the direction of the current through the write head winding.

This circuit reverses the write current direction by means of charging and discharging an electrolytic capacitor. Thus, the current waveform theoretically looks as shown in Fig. 3-14.

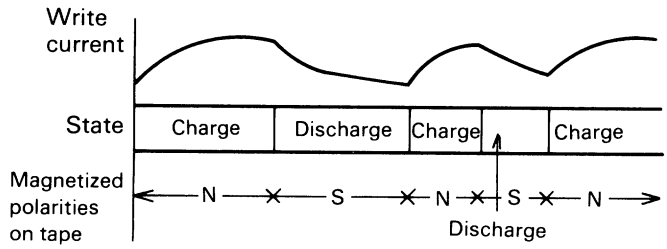


Fig. 3-14 Tape Write Current Waveform

Writing a value is ultimately generating a magnetic polarity determined by the write current direction. In order to eliminate interference which may be caused by data patterns previously written (magnetized) on the tape, the erase head is always activated during write operation initiated by the ERAH signal. New data, then will not be affected by previously magnetized polarities and the tape can be uniformly magnetized as new data is written Fig. 3-15 conceptually illustrates this operation, including the positional relationship between the read/write and erase heads.

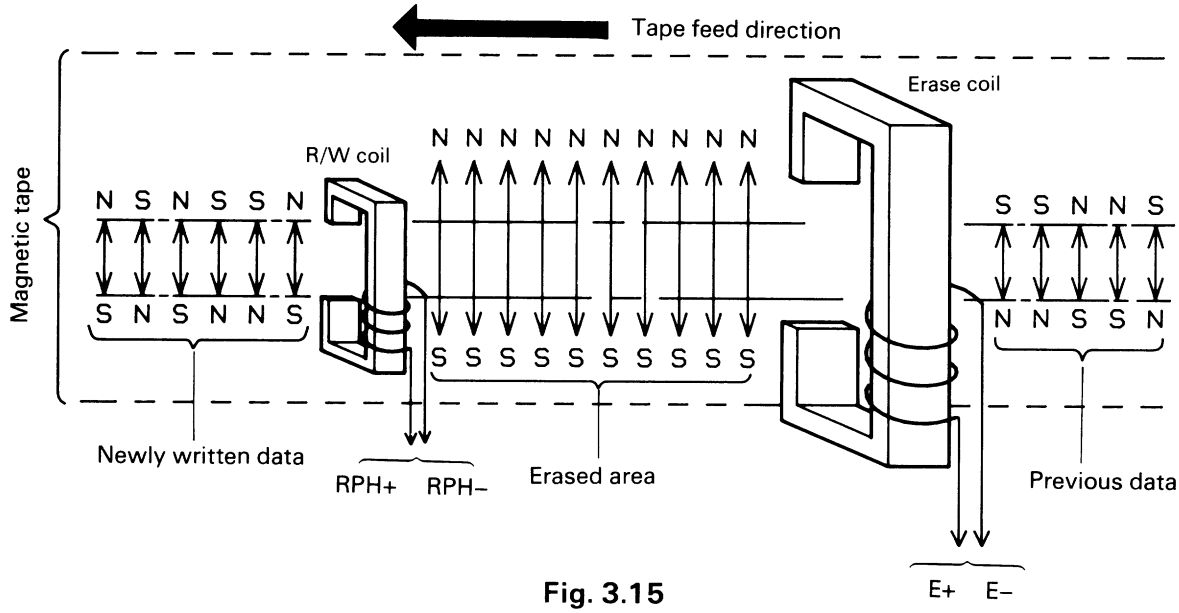


Fig. 3.15

3.1.7.2 Circuit Operations

Fig. 3-16 illustrates the write circuit. To write data, the direction of the write current through the read/write head is alternated by repeating charging and discharging the electolytic capacitor C12.

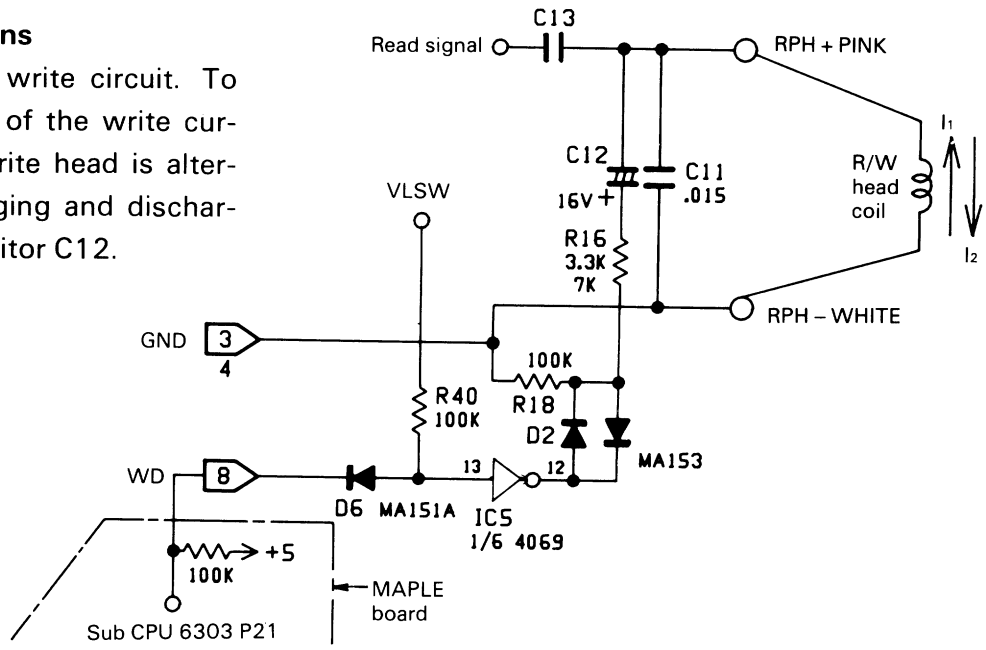


Fig. 3-16

A series of actual data bits is written on tape by alternating current to enable or disable, depending on the value of each bit, the pull-up of the input to pin 5 of IC5 to the VLSW voltage line through R4. The WD signal, which represents the logical value 0 or 1 of each data bit, usually varies its level and appears as shown in Fig. 3-17; it looks like a train of pulses.

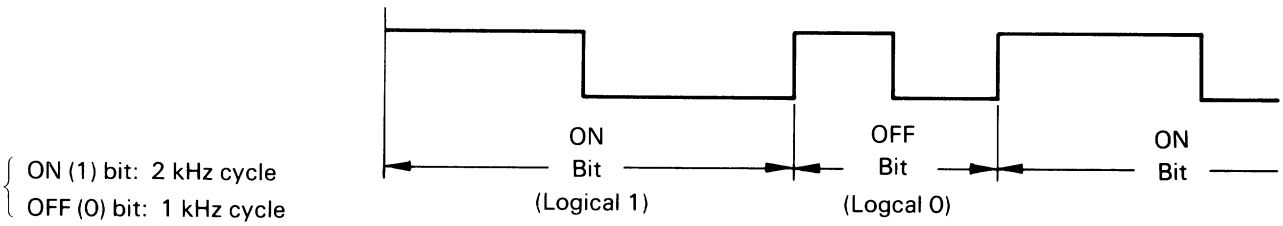


Fig. 3-17 Write Signal (WD) Pulse Train

* The flag bit is also written for each data byte and the write signal appears as shown in Fig. 3-18.

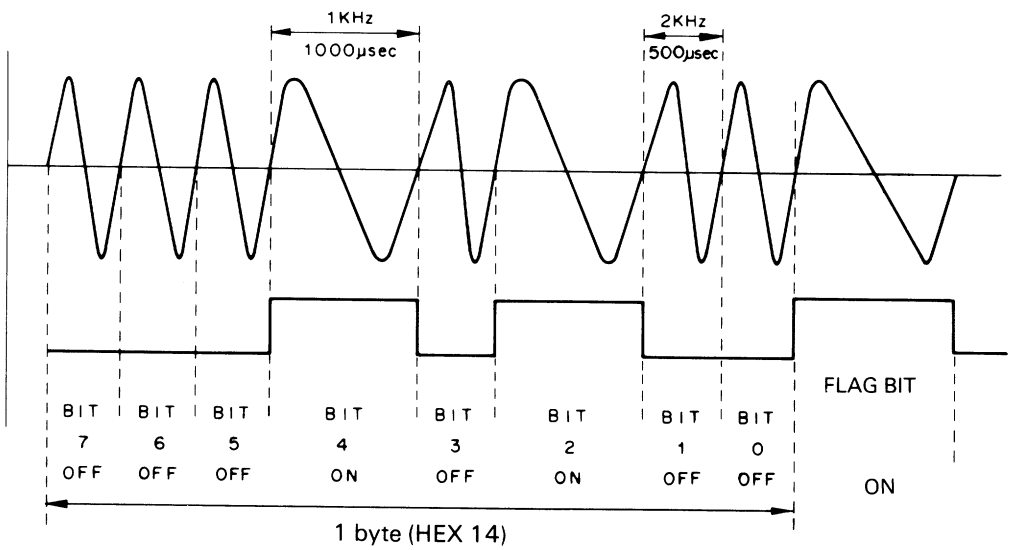


Fig. 3-18 Sample Write Signal Waveform

The above sample illustrates a data write (i.e. transfer) rate of approximately 1286 bps. As shown below, the rate varies depending on the bit configuration of the byte. Because the above sample data byte has four bits on and four bits off, the time required to write the entire byte (8 data bits and 1 stop bit) is:

$4 \times 0.5 + 5 \times 1.0 = 7$ ms

Thus, a write time of 0.777 ms (7/9) is required per bit, resulting in the data transfer rate of approximately 1286 bps.

Circuit Operations During Non-Write

Part 21 of the 6303 slave CPU on the MAPLE board is a floating part, IC neither activate nor non-active signals are output. The WD signal line is always pulled up through a 100 kohm resistor. This causes output pin 13 of IC5 to be held low. The positive pole terminal of capacitor C12 is always grounded through the diode D2 and IC5, and no current flows through the read/write head.

Circuit Operations During Write

When the WD signal is low, a current flows from the VLSW line to port 21 through R40 and D6, lowering pin 13 of IC5 to almost 0V. This causes pin 12 to go high which allows the capacitor C12 to be charged, resulting in the write current through the read/write head in the direction indicated as I2 in Fig. 3-16.

When the WD signal goes high, C12 starts charging and results in the write current indicated as I1. This charge and discharge cycle is repeated for each data bit until the complete series of data bits is written. The diode D2 connected at pin 12 of IC5 limits the top and bottom of the signal by approximately 0.6V each as shown in Fig. 3-19. This serves to supply the optimum current waveform to the write winding.

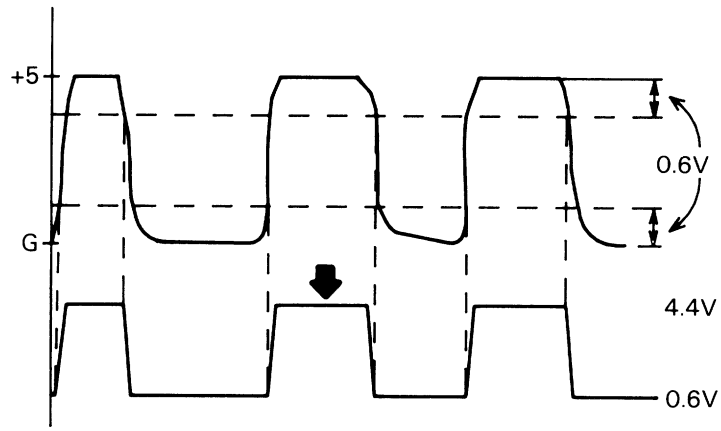


Fig. 3-19 Write Current Waveshaping

For data integrity, however, the data section of each file is written twice. Furthermore, each cassette tape reel requires a directory and a gap between blocks. Thus, the actual write time requires more than twice as long as that obtained from the above transfer rate.

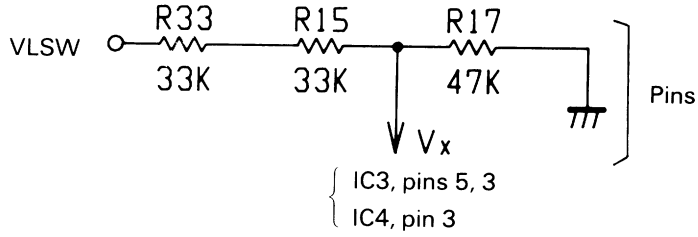
3.1.7.3 Read Circuit

Data written on tape as a series of alternating magnetized polarities is read using voltage induction across the read winding. The induced voltage is amplified by a negative feedback integrating circuit and played back. To also allow sound playback, this circuit has a signal output terminal to the speaker (RDSP) in the middle of a series of amplifiers. Fig. 3-20 shows the circuit.

Circuit Operations

The read signal from the read winding is fed to pin 6 of IC3, after its dc component is removed by capacitor C13. Divided voltage from VLR0 is supplied to pin 5 by the voltage divider circuit.

$$Vx = \frac{5 \cdot 47K}{33K + 33K + 47K} \rightarrow = 2.0\ V$$



Pins 5 through 7 of IC3 form a negative feedback amplifier ($G = -\frac{R20}{R14}$).
The output signal is fed, after its dc component is rejected by capacitor C18, to the next stage, which is also a negative feedback amplifier ($G = -\frac{R22}{R21}$).
The output of this amplifier is fed to the next filter circuit. It is also supplied to the speaker circuit on the MAPLE board. Since no phase compensation is provided in the previous stages, the signal here has some delay.

In the filter circuit, a high frequency component is removed by the T-type filter consisting of R26, R27, and C23, and the amplifier circuit. The amplifier frequency response is varied to lower the gain in a high frequency range.

The amplifier, consisting of pins 1 through 3 of IC3, detects signal peaks.

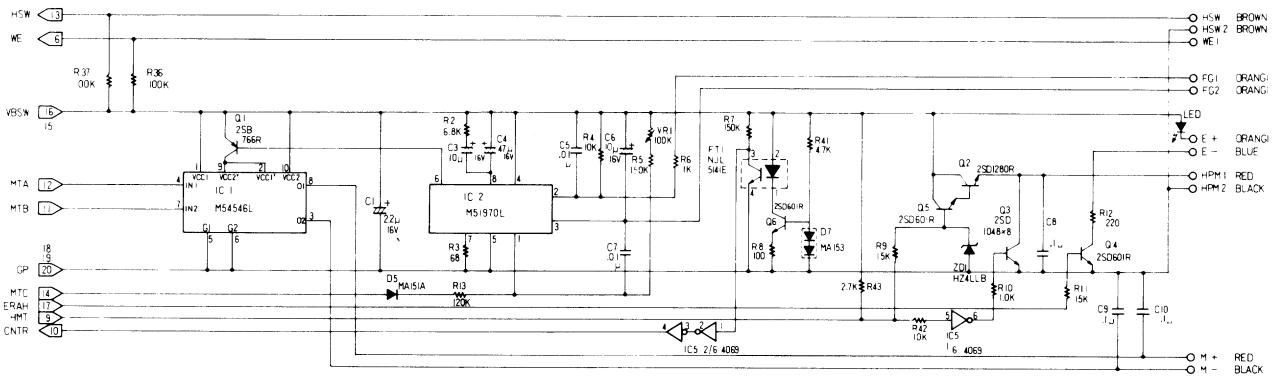


Fig. 3.20 Read Circuit

Observed read signal waveforms – (AZIMUTH tape playback signals)

(Top) Measured at IC3, pin 7 – 5 mV/DIV

(Bottom) Measured at IC3, pin 1 – 5 mV/DIV
Sweep: 0.1

} 200 μS/DIV

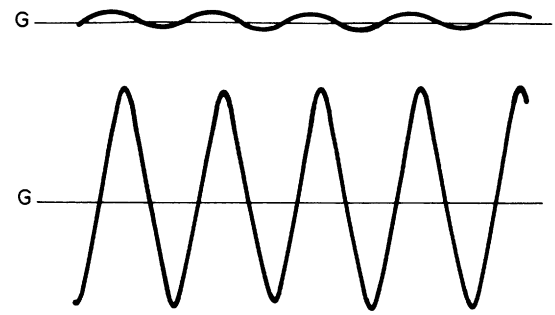


Fig. 3-21

(Top) Measured at IC4, pin 7 – 200 mV/DIV

(Bottom) Measured at IC4, pin 1 – 500mV/DIV

} 200 μS/DIV

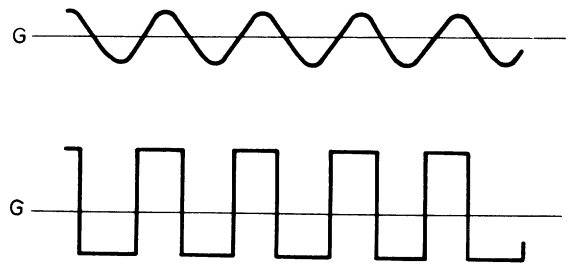


Fig. 3-22

(Top) Measured at IC4, pin 2 – 50 mV/DIV

(Bottom) Measured IC4, pin 1 – 500 mV/DIV

} 200 μS/DIV

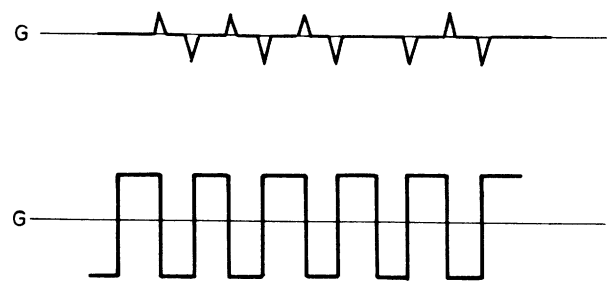


Fig. 3-23

Observed microcassette tape playback waveforms – AZIMUTH tape

(Top) Measured at IC3, pin ..... 5 mV/DIV
(Second from top) Measured at the center of R26 and R27..... 20 mV/DIV
(Second from bottom) Measured at IC4, pin 6..... 50 mV/DIV
(Bottom) Measured at IC4, pin 5. AC mode ..... 2 V/DIV

500 μS/DIV

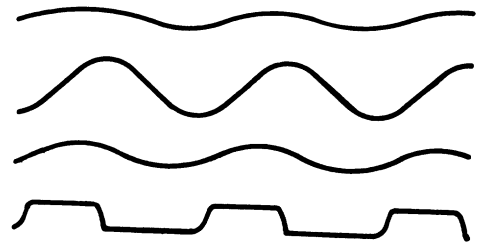


Fig. 3-24

The top three are since waves. The bottom signal is almost a square wave, due to a peak detection by a diode inserted across pins 1 and 2 of IC4.

Observed noise filter (phase compensation) circuit signal waveforms AZIMUTH – tape

(Top) Measured at IC3, pin
(Second from top) Measured at the center of R26 and R27.
(Second from bottom) Measured at IC4, pin 6.
(Bottom) Measured at IC4, pin 5. AC mode

200 mV/DIV
50 μS/DIV

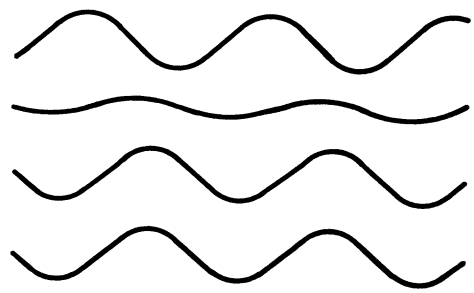


Fig. 3-25

Observed capstan motor control signal waveforms

(Top) Feedback signal from tacho generator – measured at IC2, pin 3.

(Bottom) 400 kHz basic clock signal measured at IC2, pin. 2.

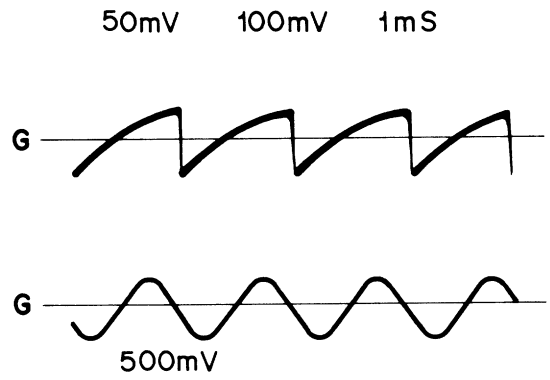


Fig. 3-26

(Top) Capstan motor drive voltage input – measured at IC, pin 2.

(Bottom) Voltage control signal – measured at IC2, pin 6.

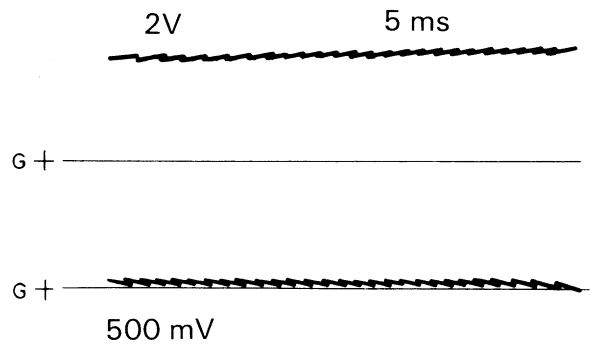


Fig. 3-27

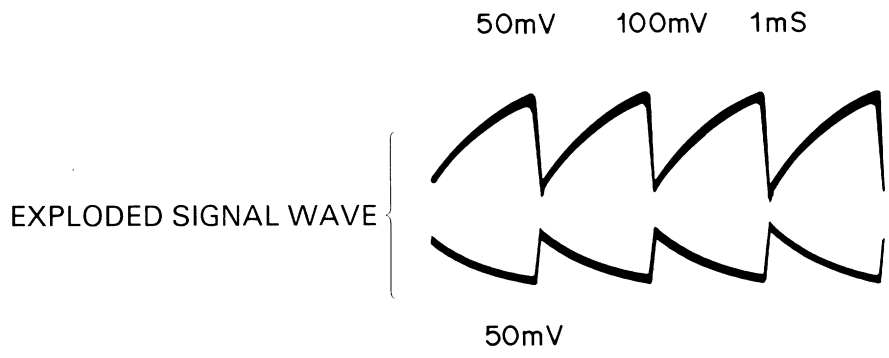


Fig. 3-28

3.2 RAM Disk Unit

Two models of 60K and 120K bytes are available. The models have the same circuit and operates exactly the same way. Only the difference is whether 64K or 128K bytes of DRAM are installed. The RAM disk unit has a Z-80 CPU built in and is operated asynchronously with the Main Frame.

3.2.1 Major Circuit Elements

The RAM disk unit is built on a circuit board which contains casing components and the following major circuit elements shown and listed below including a battery.

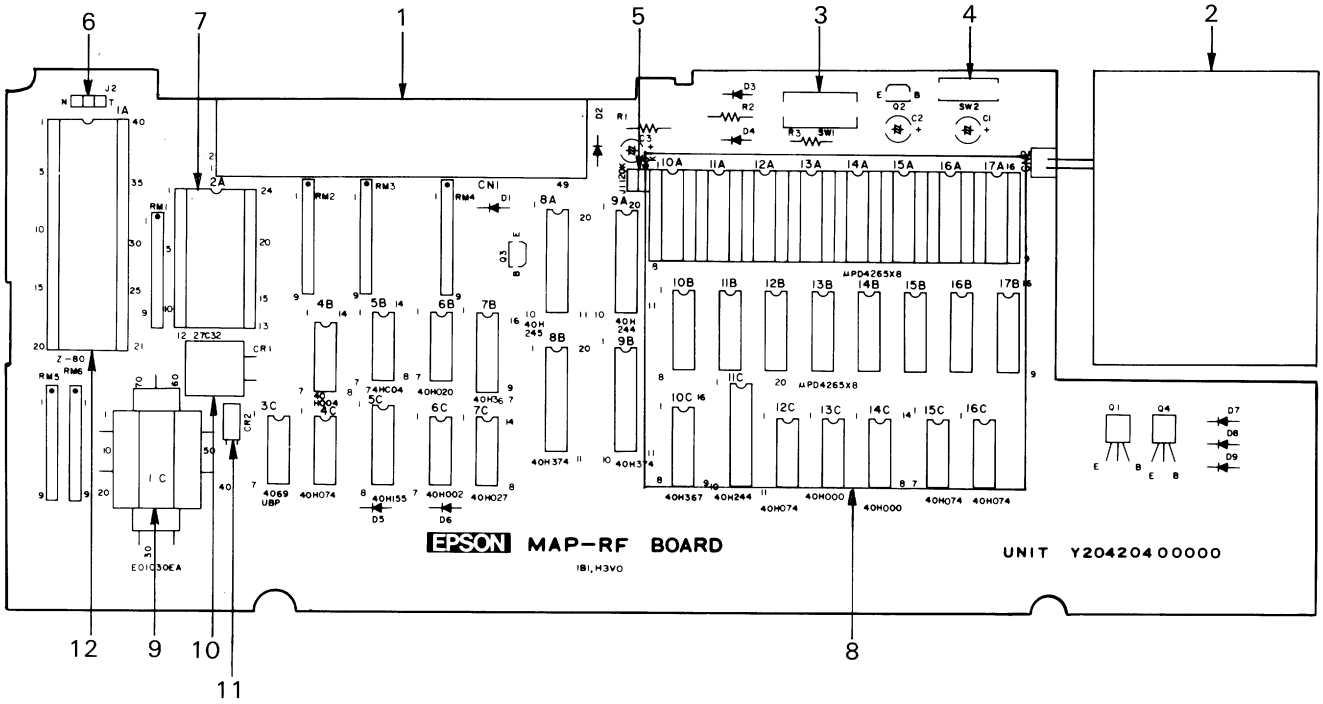


Fig. 3-29 RAM Disk Board Element Lay-Out

Table 3-2 Major Circuit Element

No.	Element	Function	No.	Element	Function
1	Connector CN1	Interface the data and address busses with Main Frame.	2	Battery	4.8V, 480mAH
3	SW 1	Write protect control ON: Protect OFF: Unprotect	4	SW 2	Connect/disconnect the built-in battery – the line normally connected.
5	Jumper J1	Define RAM capacity (60 K or 120 K).	6	Jumper J2	Z-80 CPU selection.
7	ROM (27C32)	Control for RAM disk Operation.	8	D-RAM	64/128 K D-RAM
9	Gate array (GAH40D)	Control for DRAM read/write.	10	Crystal resonator CR1	Provide a clock signal of 9.8 MHz
11	Crystal resonator (R2)	Provide a clock signal of 32.768kHz.	12	CPU Z-80	Control the RAM disk unit – operates at a clock rate of 2.45 MHz.

3.2.2 Function Circuit Blocks

Fig. 3-30 is a functional block diagram of the RAM disk unit.

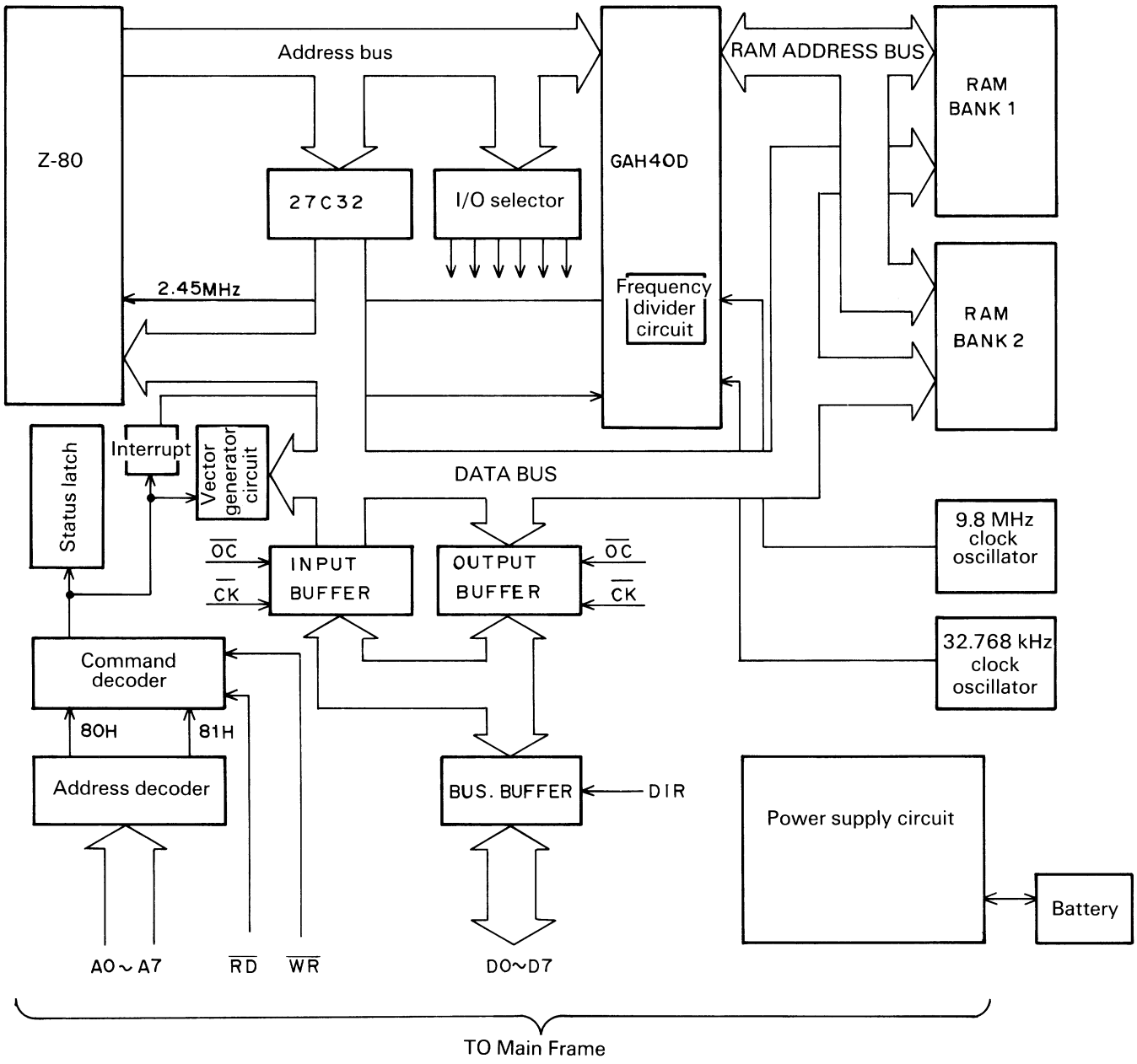


Fig. 3-30 RAM Disk Unit Block Diagram

The RAM disk unit includes a power supply circuit, hand-shaking circuits such as an address and command decoders and a status latch, etc.; a DRAM control circuit; a interrupt control circuit; a data bus input/output control circuit; two clock-oscillator circuits; and an I/O selector circuit. etc. Data are transferred between the Main Frame and RAM disk main CPUs (i.e., read/write operation for RAM disk unit by referring to the status latch. The CPUs have their own memory spaces independent from each other and data transfers between them are accomplished in forms of I/O read/write operations.

3.2.3 Interface Signals

The RAM disk unit is connected to the Main Frame board via a cable assembly # 727. Table 3-3 lists the interface signals.

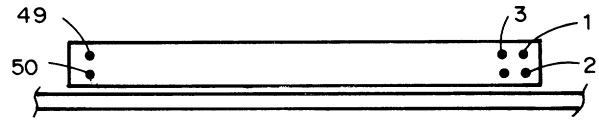


Table 3-3. RAM Disk Unit Interface Signals

Pin No.	Signal Name	Direction	Definition
1	–	–	Not used.
3	–	–	Not used.
5	AB1	Input	Address but line 1
7	–	–	Not used
9	AB4	Input	Address bus line 4
11	AB6	Input	Address bus line 6
13	–	–	Not used.
15	–	–	Not used.
17	DB0	Input/ Output	Data bus line 0
19	DB2	Input/ output	Data bus line 2
21	DB4	Input/ Output	Data bus line 4
23	DB6	Input/ Output	Data bus line 6
25	–	–	Not used.
27	–	–	Not used.
29	VL	Input	Logic circuit +5V supply
31	GND	–	Signal ground
33	$\overline{RS}$	Input	Reset
35	$\overline{RD}$	Input	Read
37	$\overline{WR}$	Input	Write
39	VCH	Input	Battery charge voltage
41	DCAS	Input	Cata CAS
43	–	–	Not used.
45	–	–	Not used.
47	VB1	Input	Battery voltage
49	–	–	Not used.

Pin No.	Signal Name	Direction	Definition
2	–	–	Not used.
4	–	–	Not used.
6	AB2	Input	Address bus line 2
8	AB0	Input	Address bus line 0
10	AB3	Input	Address bus line 3
12	AB5	Input	Address bus line 5
14	AB7	Input	Address bus line 7
16	–	–	Not used.
18	DB1	Input/ Output	Data bus line 1
20	DB3	Input/ Output	Data bus line 3
22	DB5	Input/ Output	Data bus line 5
24	DB7	Input/ Output	Data bus line 7
26	–	–	Not used.
28	–	–	Not used.
30	–	–	Not used.
32	GND	–	Signal ground
34	–	–	Not used.
36	–	–	Not used.
38	–	–	Not used.
40	$\overline{IORQ}$	Input	I/O Request
42	DW	Input	Data Write
44	OFF	Input	GAH40D Initialization
46	–	–	Not used.
48	–	–	Not used.
50	–	–	Not used.

Note:

Some of the signals used in the Main Frame including the address bus lines AB7 through AB15, etc. are not used in this interface.

3.2.4 Jumpers and Switches

The following jumpers and switches are mounted on the RAM disk unit board. The switches SW 1 and SW 2 will be accessed by user.

Table 3-4 Jumper and Switch

Jumper/switch	Standard	Drawing coordination	Function
J1	—	D.E -4	Select a RAM capacity: 60K or 120K bytes, according to the installed RAM elements.
J2	—	E -2	Specifies the main CPU.
SW1	ON	ONE -4	Enable/disable DRAM write protection ON: Enables write protection – allows read only. OFF: Disables write protection – allows both read and write.
SW2	ON	A -6	Enable/disable battery backup ON: Enables battery backup – allows battery charge/discharge. OFF: Disables battery backup – battery charge/discharge is inhibited.

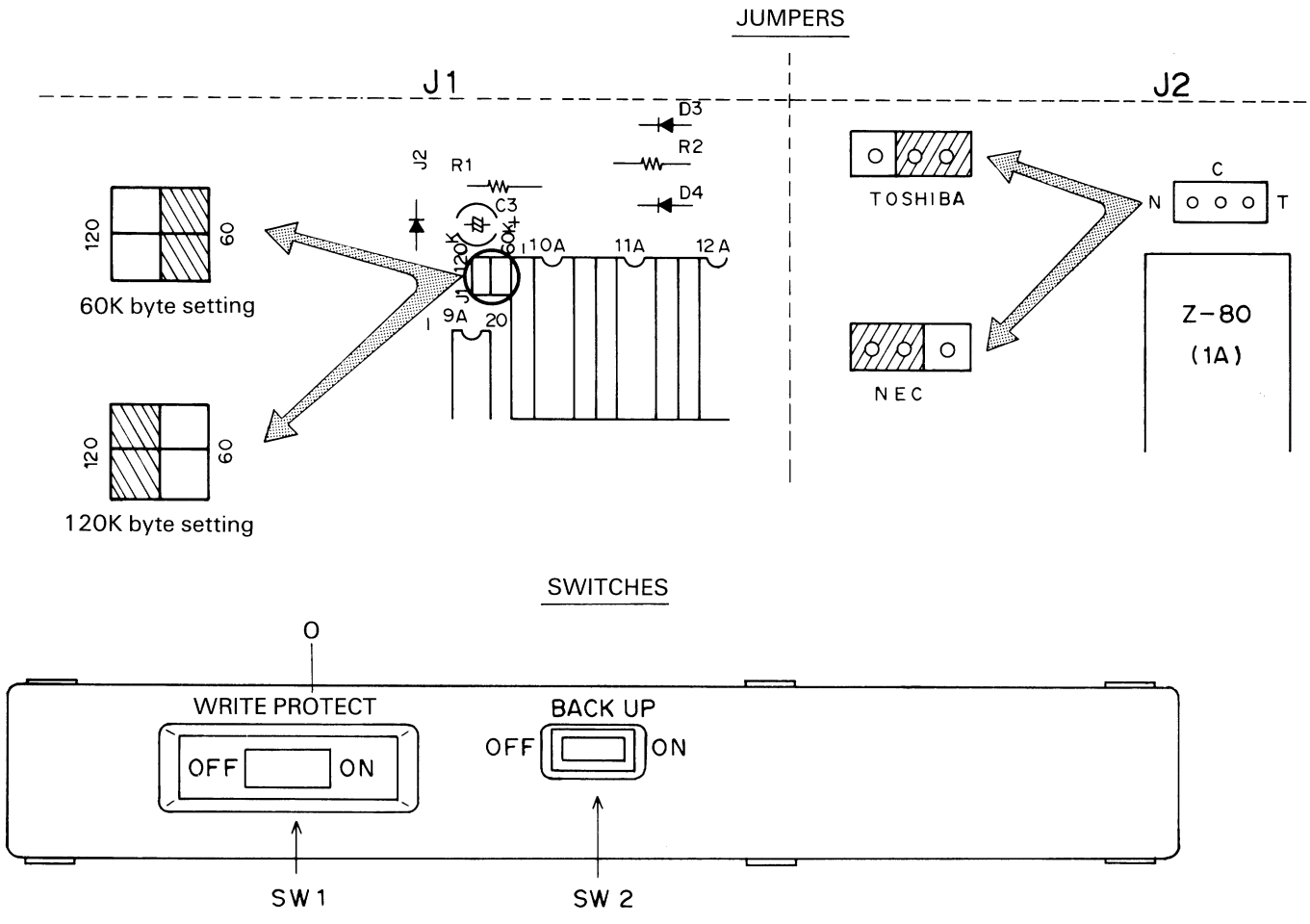


Fig. 3-31 Jumper and Switch Location

3.2.5 Power Supply Circuit

The RAM disk unit power supply circuit consists of a +4.8V, 450 mAH rechargeable battery, a charge circuit, a logic voltage source circuit, and a backup circuit.

1. Rechargeable battery and charge circuit

   The battery is connected to the MAP-RF board via a connector CN 2. The switch (SW2) on the board allows the user to connect or disconnect the battery to the MAP-RF board.

   The circuit surrounding the battery is shown below.

1) Battery backup switch SW2

   This switch should be reset OFF when storing this unit alone or when not using it for a long period of time as attached to the Main Frame. With this switch reset OFF, the battery is prevented from any discharge other than the natural one so that the longest life can be ensured.

* The backup line circuit operates irrespective of the setting of this switch; when the switch is reset OFF, the line is backed up from the Main Frame battery and its working time may be shortened.

2) Battery charging

   The battery is always charged toward the full via either of the following two charging paths:

   When the Main Frame AC adaptor is connected to the AC power source.

   V_{CH} → D2 → R1 → SW2 → CN2 → Battery

   When the AC adaptor is not used but the battery voltage is lower than the VB1 supply voltage from the Main Frame.

   V_{B1} → D3 → R2 → SW2 → CN2 → Battery

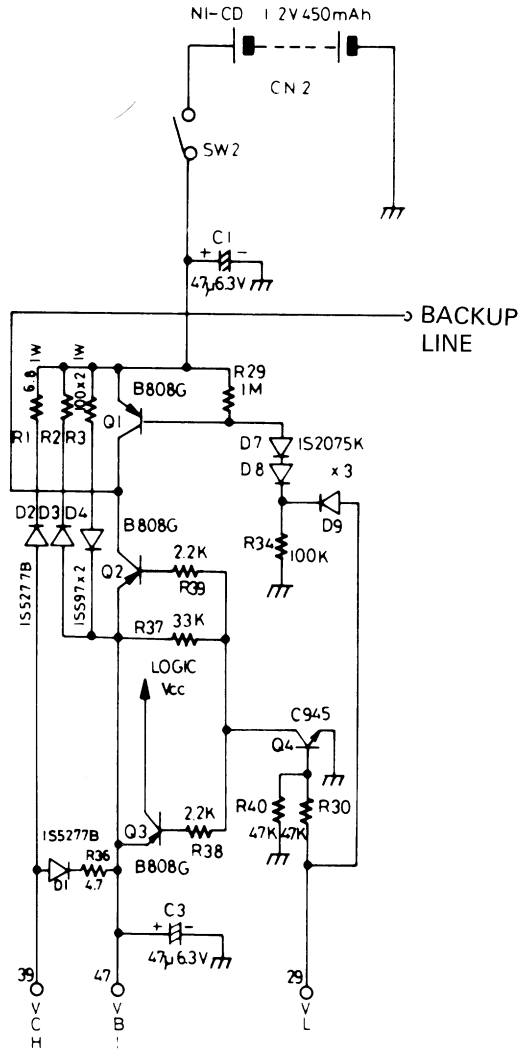


Fig. 3-32 Power Supply Circuit

2. Backup circuit

The backup circuit supplies power required to protect data in the DRAM.

Table 3-5 lists the elements backed up by this circuit.

Table 3.5 Backed Up Elements

Element	Drawing coordination	Function
1C	F-1, 2	Read/write control gate array
9A	H-1	Gate
3C	A, B-7	Gate

Element	Drawing coordination	Function
17B ~ 10B	G-2 ~ 6	D-RAM
17A ~ 10A	H-2 ~ 6	D-RAM
3C	F-3	Gate

These elements are powered from a special line called "Backup" and always active; they are powered by the operating voltage supply while Main Frame is on and from the backup voltage while off.

1) Power supply paths to the backup line

There are the six paths listed in table 3-6 which are selected to supply power to the backup line depending on the various conditions. The abbreviations used in the table mean the following:

V_{B1} : Main Frame battery voltage
V_X : RAM disk unit battery voltage
Battery: RAM disk unit battery

Tabel 3-6 Backup Line Supply Paths

Main Frame power	AC adapter	Battery voltage relation	Path
OFF	Connected	—	V_{CH} → D2 → R1 → Q1 →
	Not connected	$V_{B1} > V_X$	V_{B1} → D3 → R2 → Q1 →
	Not connected	$V_{B1} < V_X$	Battery → CN2 → SW2 → Q1 →
ON	Connected	—	V_{CH} → D1 → R36 → Q2 →
	Not connected	$V_{B1} > V_X$	V_{B1} → Q2 →
	Not connected	$V_{B1} < V_X$	Battery → CN2 → SW2 → R3 → D4 → Q2 →

The backup line is powered either transistor Q1 or Q2 depending on whether Main Frame power is on or off.

* While Main Frame is off, VL is low because the logic circuit operating voltage is not supplied. This maintains transistor Q4 cut off and the collector is pulled up high through resistor R37. Thus, transistors Q2 and Q3 remain cut off.

VL is also connected to the base of Q1 through diodes D7, D8, and D9. The emitter of Q1 is connected to VB1 or the RAM disk battery voltage and normally maintained at +5V. The source is also connected to the base through R29. Because the base is connected to the signal ground through D7, D8, and R34, the current, which flows from the base to the ground unless the junction of D8 and R34 is pulled up to the VL line, generates a potential across the emitter and base. That is, transistor Q1 conducts due to this potential while Main Frame is off.

While Main Frame Power is on, no effective potential is generated across the emitter and base of Q1 because the base is pulled up to VL, and Q1 is maintained cut off. Q4 conducts because the base input (VL) is low and the collector is held low. This maintains Q2 and Q3 in conduction. Thus, the backup line is powered via Q2 and the logic circuit voltage is supplied through Q3.

3. Logic circuit voltage

The logic circuit voltage is supplied from the collector of transistor Q3. The voltage applied to the emitter (VB1 or V_{CH} through D1 and R34) is supplied to the circuit power line. The supply circuit operates as descried above.

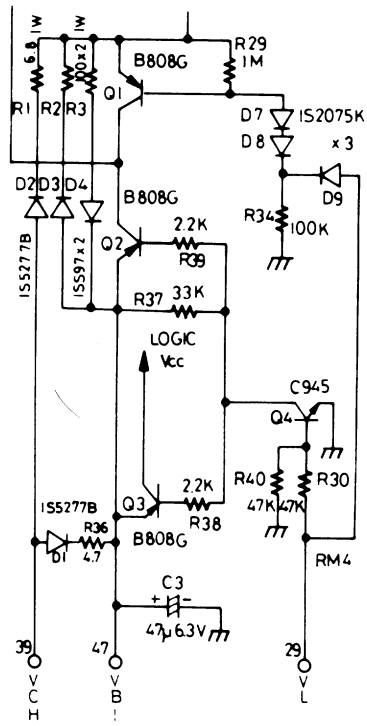


Fig. 3-33 Power Supply Circuit

3.2.6 Interface Circuit

Since this RAM disk unit and Main Frame asynchronously operate, either one must examine the status of the other to accomplish a RAM disk read/write. A function, which temporarily stores the data until it is written in RAM disk or read by Main Frame, is also required.

1. Address decoder

The RAM disk is looked upon as an I/O device by the Main Frame CPU and two I/O addresses are assigned. Fig. 3-34 shows the address decoder circuit.

Pin 10 and 13 of IC "6C" are the outputs of the decoder. As obvious from the figure, the output (pin 8) of IC "6B" must be low to enable the two decoder outputs. Either of them is selected depending on the state of A0. The output IC "6B" is low when the following relation is satisfied among the input signals to this IC and the preceding IC "7C"; $\overline{A1 - A6}$ .A7.$\overline{IORQ}$. This relation can be logically represented as in Fig. 3-34; an address 80 (H) or 81(H) is decoded to access the RAM disk unit.

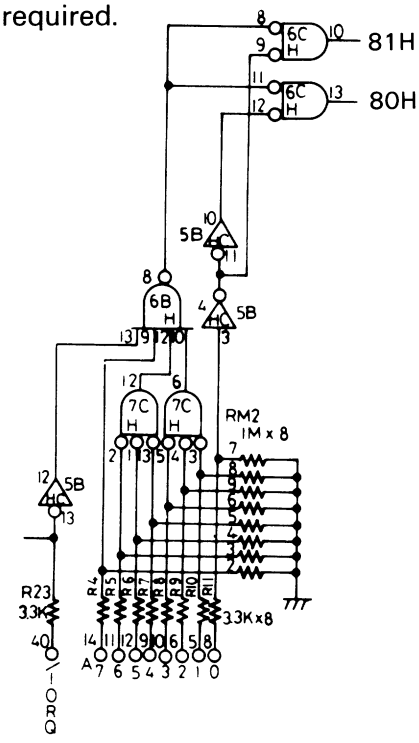


Fig. 3-34 RAM disk address decoder circuit

A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	0	0	0	1/0

80 (H)
or
81 (H)

2. Command decoder

Four signals are generated by IC "14C" from either address supplied from the address decoder and the $\overline{RD}$ and $\overline{WR}$ signals as shown in fig. 3-35.

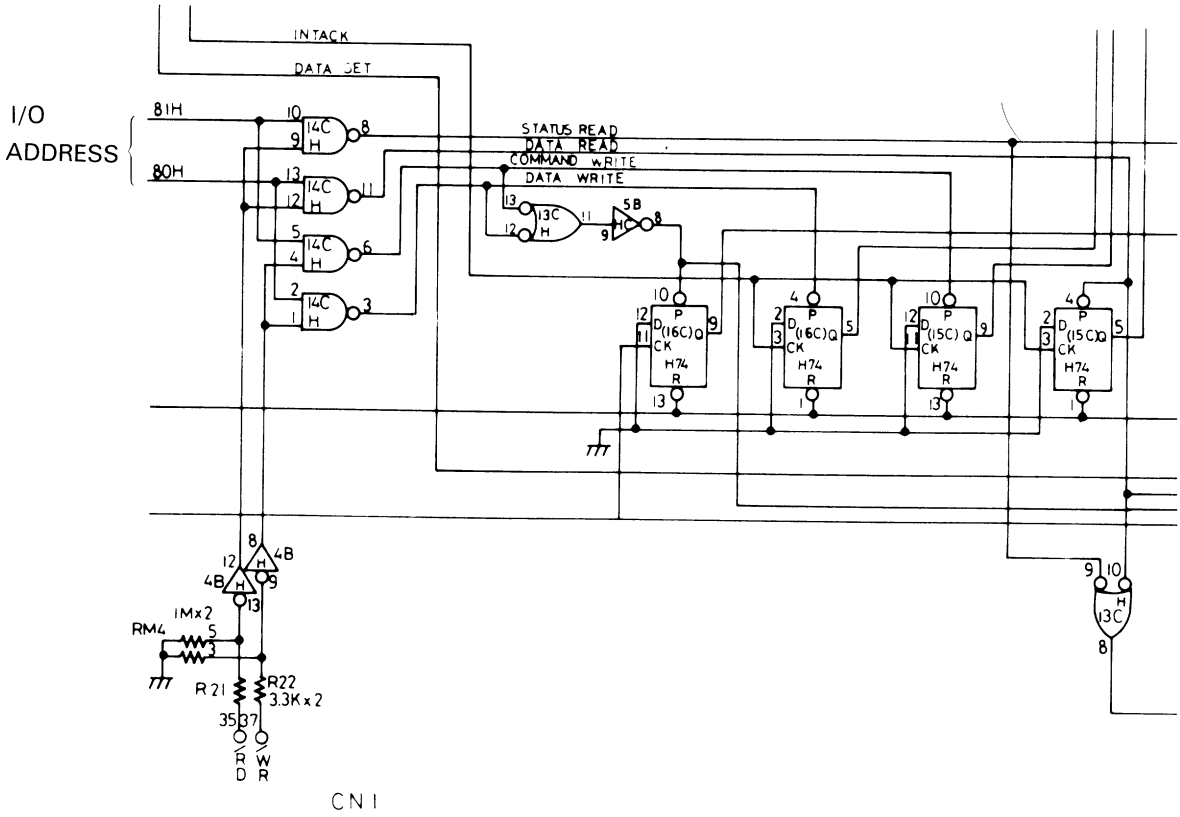


Fig. 3-35

The four I/O read/write signals provide the functions listed in table 3-7.

Table. 3-7 Command Decoder Signals

I/O Addrss	$\overline{RD}$/$\overline{WR}$ signal	Generated signal	Function
81 (H)	$\overline{RD}$	Status Read	Read RAM disk status to Main Frame
	$\overline{WR}$	Command Write	Write a command from Main Frame to RAM disk.
80 (H)	$\overline{RD}$	Data Read	Read data from RAM disk to Main Frame
	$\overline{WR}$	Data Write	Write data from Main Frame to RAM disk.

Unlike the other three, the Status Read signal reads the RAM disk status register irrespective of the RAM disk CPU operation, directly controlling the register read access and data bus drive. The other signals cannot accomplish their functions without intervention by the RAM disk CPU. In addition, any of these signals cannot be directly transferred between the Main Frame and RAM disk CPUs because they are operating asynchronously. Thus, a means is required to temporarily store the signals. This is accomplished by the circuit consisting of the two ICs "15C" and "16C" both of which contain two D-type FF having Preset (P) and Clear (C) terminals. Each of four signals is connected to the Preset terminal of one of the four D-type FFs. Once a signal activated low, the corresponding FF is set and the Q output remains high until either of the following occurs:

* CK input: I/O port 03 (H) read by RAM disk unit - FF output read.
* R input : PX-8 reset or I/O port 01 (H) write by RAM disk unit - program reset.

3. Data and command registers

Two 8-bit registers are provided for input and output which serve as buffers (temporary data storage) used during data transfers between the RAM disk unit and Main Frame. Their input/output or read/write is controlled via an address assigned to them. The data is directed on the data bus from/to the registers under a directional control by the data bus control feature provided by a tri-state buffer IC "8A". Fig. 3-30 shows the data transfer directions and the direction control circuit.

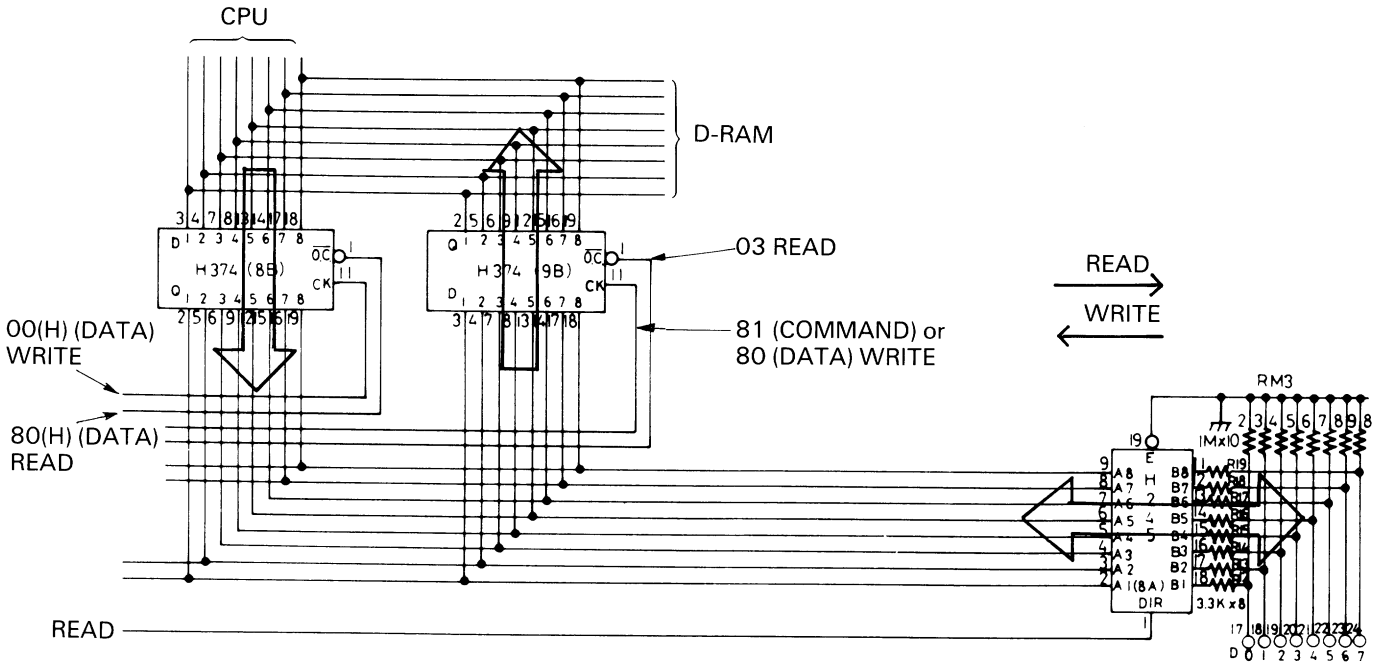


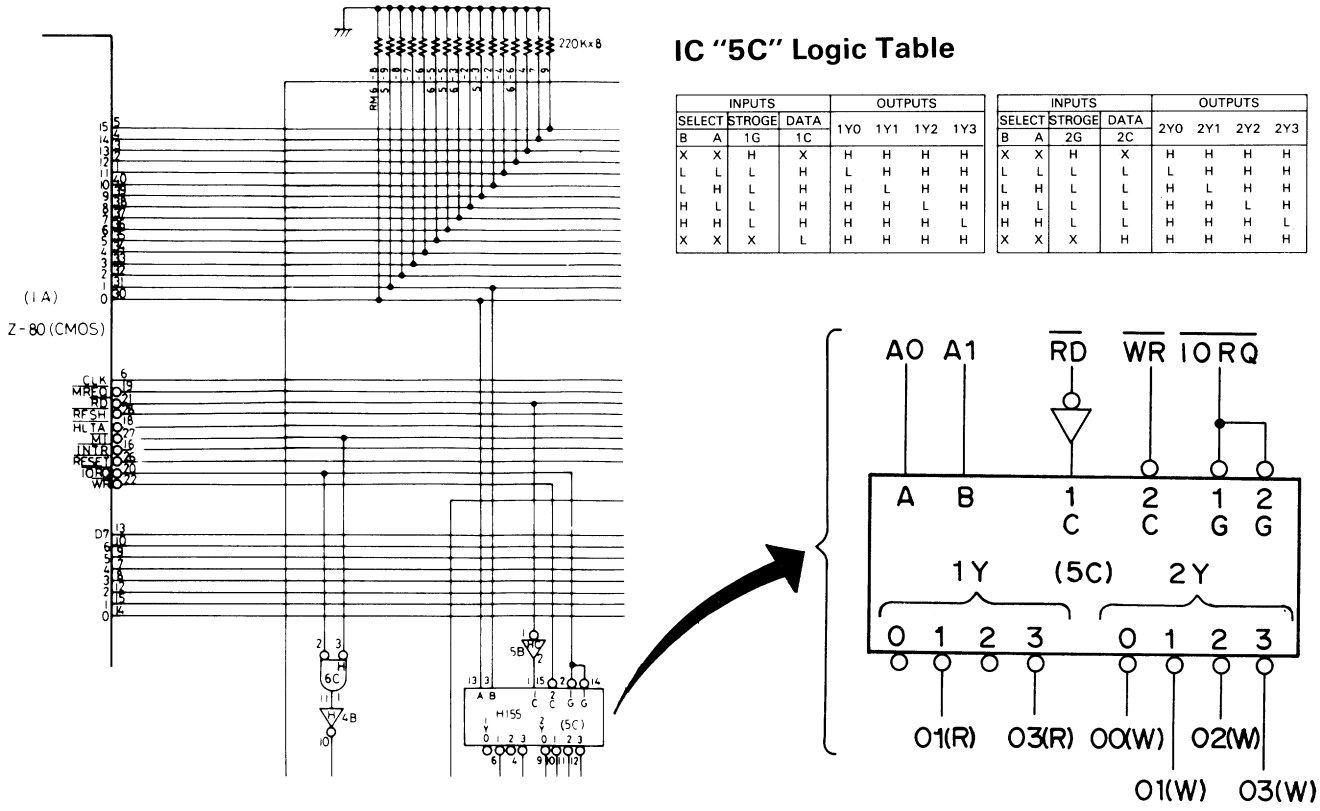
Fig. 3-36 Data Transfer Directions and Control

ICs "8B" and "9B" contain eight tri-state D-type FFs each. The FFs read and latch data from either data bus as arrowed when the "CK" signal rises. When the "$\overline{OC}$" signal goes low, the latched data becomes available onto the data bus from the output (Q) terminals.

- IC "9B" is the Input register. It latches a data directed from Main Frame via address 81 (H). This data is then transferred to the RAM disk CPU when it reads its I/O port 03 (H).
- IC "8B" is the Output register. It latches a data when the RAM disk CPU writes to its I/O port 00 (H). Then, the latched data is sent over the data bus to Main Frame when it reads its I/O port 80 (H)..
- The tri-state buffer register "8A" is controlled by the DIR input signal. When this signal is high, the "bufferred" data is directed from the RAM disk unit to Main Frame. When the signal is low, the data transfer direction is reversed.

3.2.7 I/O Selector

The I/O selector (IC "5C") is the RAM disk CPU I/O address decoder which is used for handshaking in the interface. Fig. 3-37 shows the circuit and table 4-7 lists its decoding logics.



IC "5C" Logic Table

INPUTS				OUTPUTS			
SELECT		STROGE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROGE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

Fig. 3-37 I/O Selector Circuit

IC "5C" has six outputs whose functions are listed in table 3-8.

Table 3-8 I/O Selector Logics

Read/Write	I/O Port Address	Supplied To	Function
READ	01	7B	Read J1 and SW1 status.
	03	9B	Read data or command from input register.
WRITE	00	12C, 8B	Write data to output register.
	01	13C	Program Reset output signal.
	02	4C	RAM bank 0/1 control
	03	4C	RAM bank 2 control

3.2.8 Bank Control

The RAM disk unit can contain a 4 K byte IPL ROM and 64 K or 128 K byte DRAM. However, the Z-80 CPU cannot directly access DRAM above 64 K bytes. Thus, DRAM needs to be divided into banks so that entire DRAM can be accessed indirectly by selecting bank. This control is accomplised by the Bank Latch circuit and the gate array GAH40D shown in fig. 3-38.

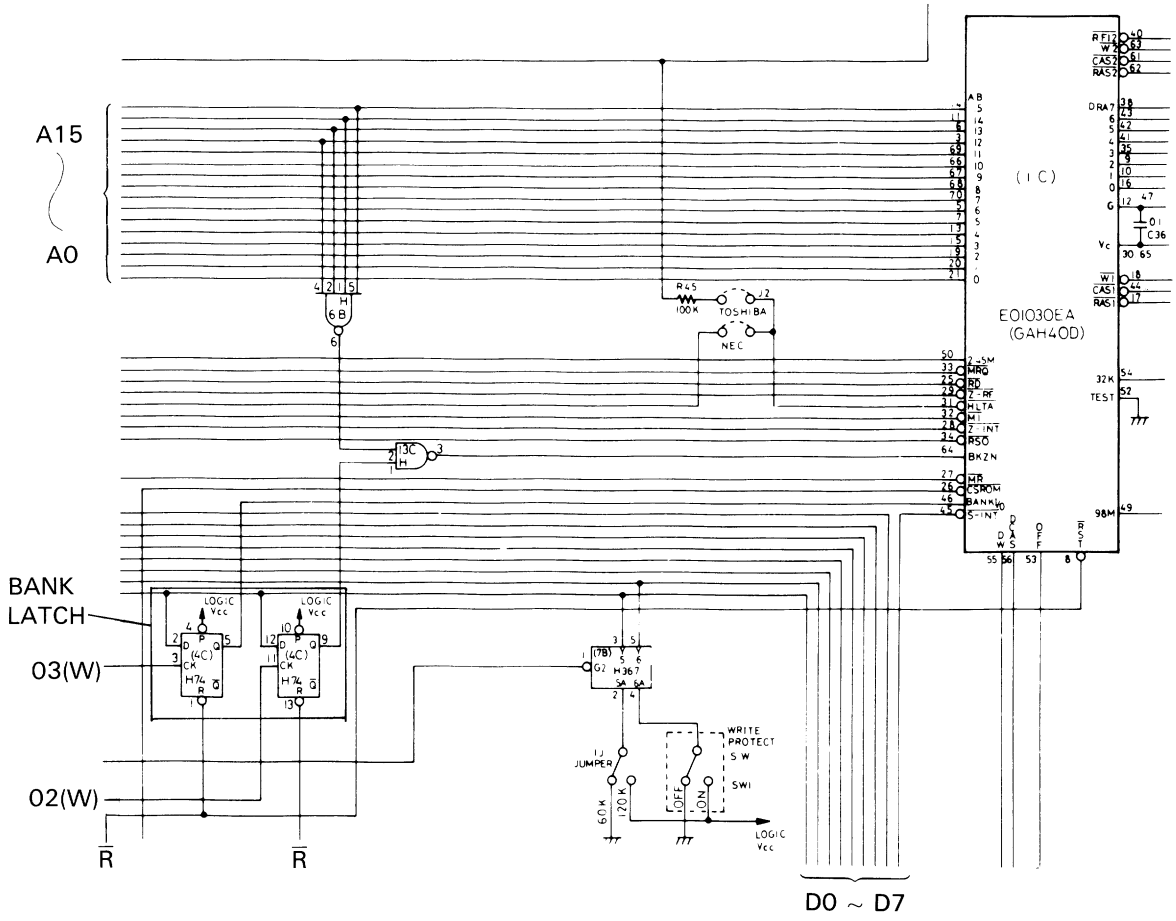


Fig. 3-38 Bank Control Circuit

1. Momory map

The bank control signals and the memory map are associated as shown in table 3-9.

Table 3-9 Bank Control Signal and Memory Map

BK 2 / BK 0/1 / Address	1 / 0	1 / 1	0 / 0	0 / 1
FFFF (FC00)	DRAM 2	DRAM 2	DRAM 1	DRAM 1
(0FFF) 0000	IPL ROM		IPL ROM	

Note:

The DRAM address space from FC00 to FFFF is a comon area which contains the bank selection program.

Gate GAH40D is initialized as follows when Main Frame Power is turned on:

Bank 2 = 1, Bank 0/1 = 0

This initialization is of course accomplished by a hardware reset logic. The initialization circuit operation is described below.

- The Reset ($\overline{R}$) signal is connected to both the Bank Latch FFs located in drawing coordinations C,D-3. Thus, the two Q outputs are held-low - the output from pin 5 is the Bank 0/1 Selection signal and the output from pin 9 is the Bank 2 Selection signal. Address bus lines 12 through 15 from the Z-80 CPU are respectively connected to pins 4, 2, 1, and 5 of IC "6B" which are all low immediately after Main Frame power is turned on, raising the output (pin 6) high. This output signal is fed to IC "13C" where it is NANDED with the Bank 2 Selection signal from the Bank Latch circuit which is also low immediately after power on. Thus, the output from pin 3 is high.

The RAM disk memory address space is mapped as shwon in the second (from the left) or fourth column of table 3-9 by initialization so that the CPU accesses address 0000; i.e., the IPL ROM area.

2. Bank selection

   Bank selection is accomplished by the program in IPL ROM which accesses I/O ADDRESS 02 and 03, which are connected to the Bank Latch, to change the latch setting. Thus, if a bank, which allows no IPL ROM access, were selected by simply accessing the Bank Latch, no subsequent bank selection would be possible. In order to solve this problem, the bank control program is usually written in the DRAM area from a certain address during the IPL program execution. This unit initially loads the bank control program in a DRAM 2 address space from FC00 to FFFF, and a common DRAM 2 area of the highest 64 bytes is always selected independently by gate array GAH40D regardless of bank (0/1 or 2).

3.2.9 Interrupt

As previously stated, the command (i.e., Read or Write) and 8-bit data sent from the Main Frame is temporarily stored in an internal buffer because the RAM disk unit operates asynchronously. The unit is notified of this temporary storage by an interrupt. Fig. 3-39 shows the interrupt circuit.

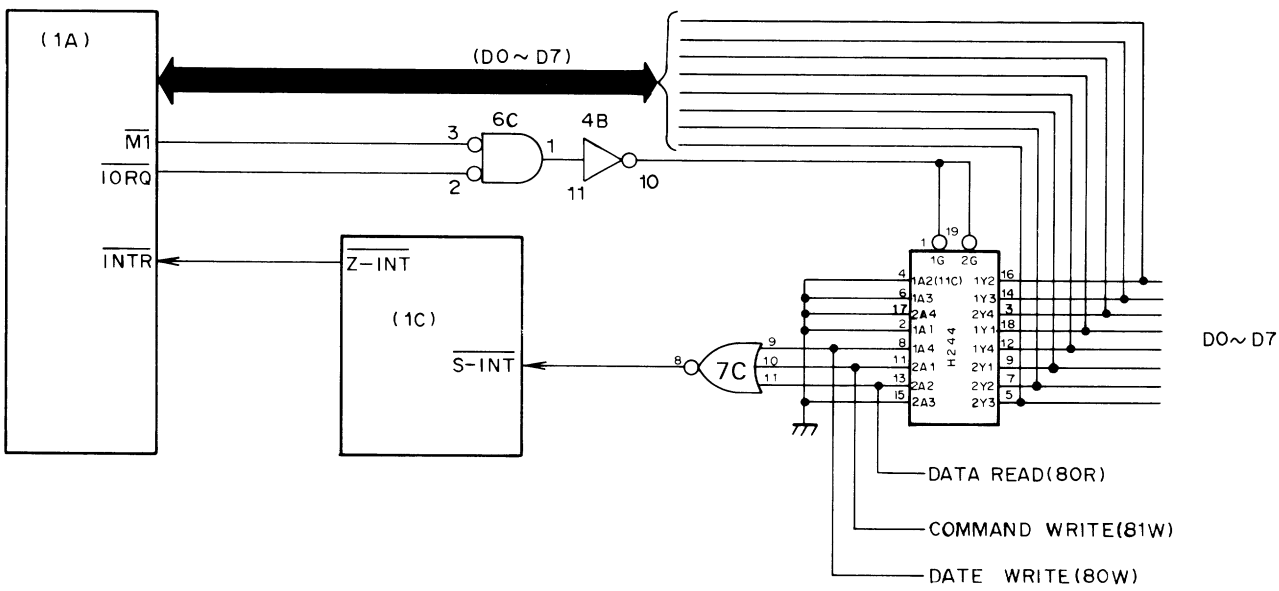


Fig. 3-39 RAM Disk Interrupt Circuit

As obvious from the drawing, the three signals other than Status Read, which instructs an immediate read, are fed to the OR circuit of IC "7C" via D-type FFs "15C" and "16C" whose output is connected to the S-INT terminal of gate array "1C". This input signal is output from the gate array as the Z-INT signal to the INTR terminal of the CPU as the interrupt input. When the AND condition between M1 and IORQ is met (indicating that a vector address is output on the data bus in the CPU mode 3) after an interruption occurs, a byte data corresponding to the RAM disk command signal is output on the data bus from the right terminals of IC "11C". This data is the interrupt vector which is fed to the CPU. There are the following interrupt vectors corresponding to the RAM disk command signals:

Command signal	**Interrupt vector**	
Data Read	02	Each of these vector address calls a specific routine that processes the corresponding command and data.
Command Write	04	
Data Write	08	

After an interrupt is accepted, the D-type FF which caused the interrupt ("15C" or "16C") is initialized. Fig. 3-40 shows the related circuit. The vector address is output and the D-type command buffer FF is reset by the same signal INTACK. However, the FF is reset at the rising edge to ensure the interrupt vector to be completely fed to the CPU as shown in fig. 3-41.

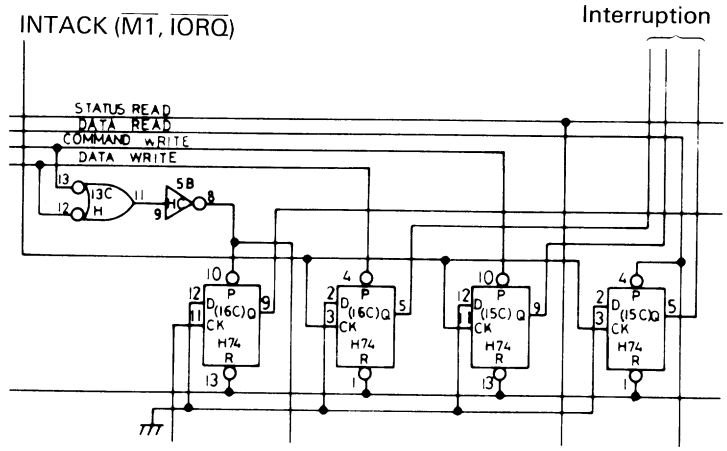


Fig. 3-40

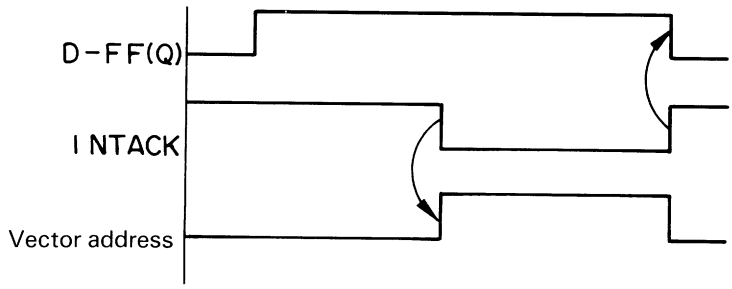


Fig. 3-41 RAM disk command buffer circuit

3.2.10 Clock Signals

Two clock signals of 9.8 MHz and 32.768 kHz are generated in the RAM disk unit. 9.8 MHz clock signal is divided in gate array GAH40D to 2.45 MHz and fed to the CPU. The 32.768 kHz clock signal is also divided in the gate array and used as the DRAM refreshing signal. Fig. 3-42 shows the clock signal oscillator circuits.

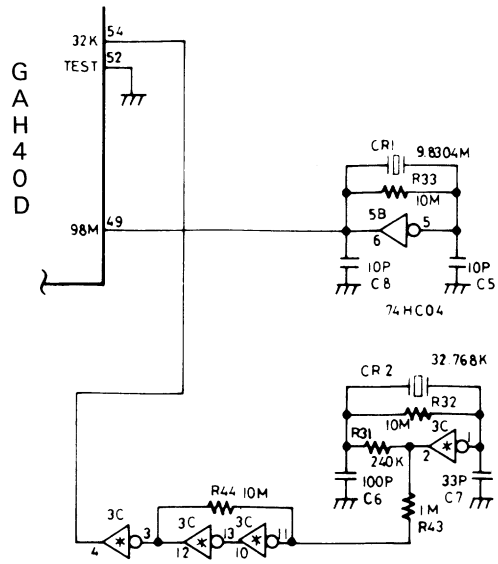


Fig. 3-42

3.2.11 DRAM Banks

The DRAM circuit is organized as shown in fig. 3-43 and controlled by gate array GAH40D.

It is read/written and refreshed (also while Main Frame power is off) in the same way as Main Frame RAM. This unit has two DRAM banks of 64 K bytes each and can provide a capacity of 64 K or 128 K bytes. Two signals DCAS and DW, which determine a refresh mode while power is off, are applied from Main Frame.

- IC "9C" is provided to ensure the address output that can drive 128 K bytes of RAM.

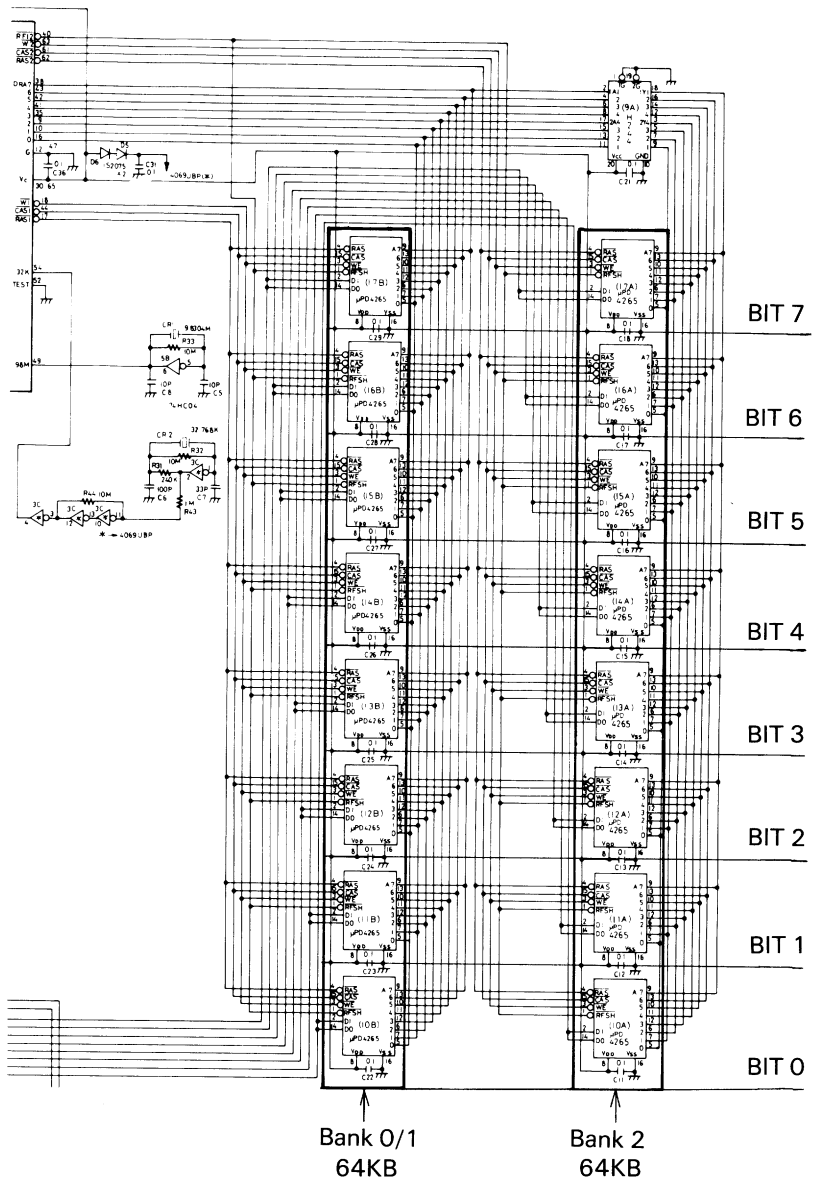


Fig. 3-43 DRAM Circuit Organization

3.2.12 Jumpers and Switch

The combination of jumper J1 and switch SW1 allows the IPL program to be read via I/O port address 01. Jumper J2 selects a CPU model.

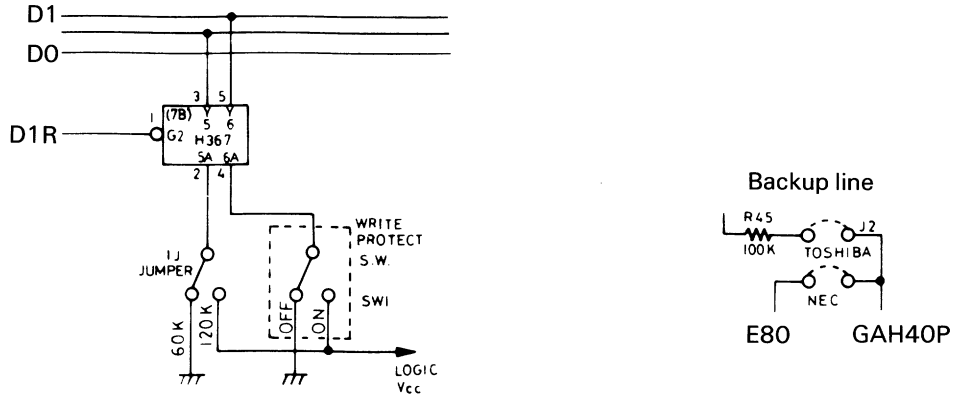


Fig. 3-44

3.2.13 Status Register

The Main Frame CPU reads the RAM disk status from IC "10C" shown in fig. 3-45. Input terminals 6 and 10 are grounded to produce the ID code of the RAM disk unit. The Date/COM Write signal input to terminal 4 indicates whether a data or command received from Main Frame is being processed or not. The signal input to terminal 2 from D-type FF "12C" indicates whether a data is latched (buffered) to be sent to Main Frame or not.

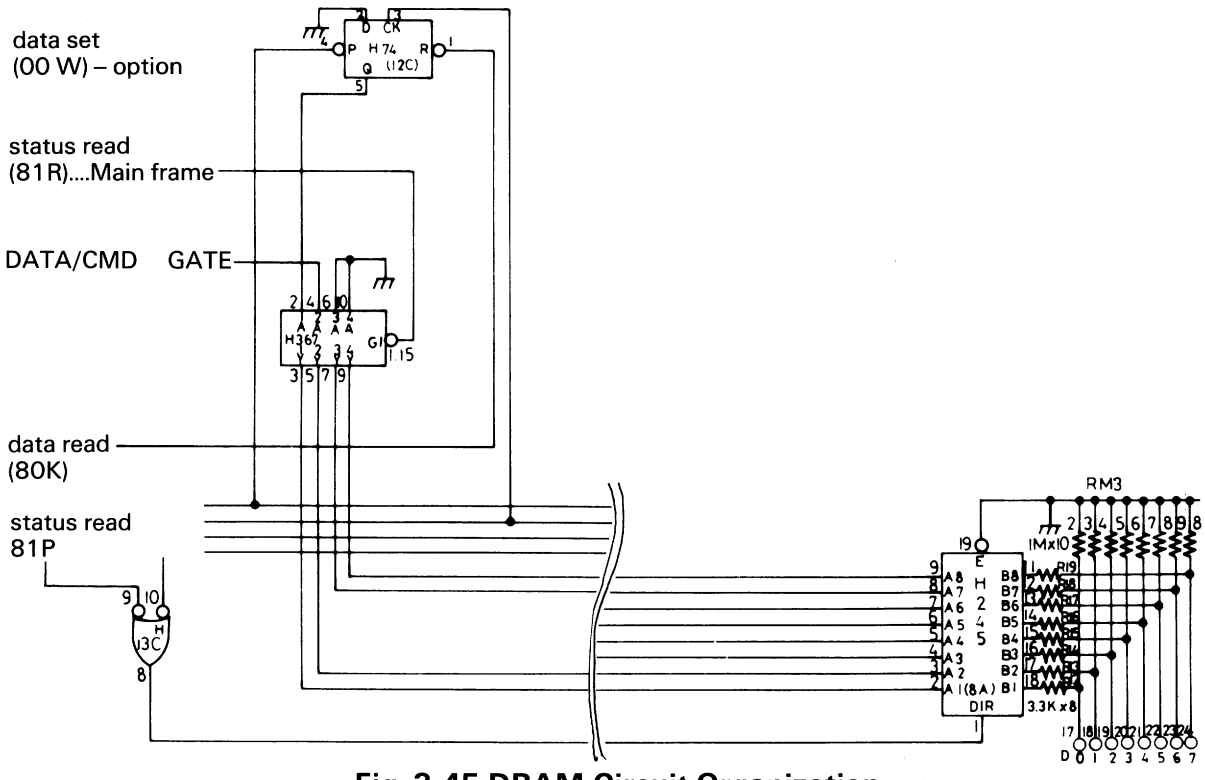
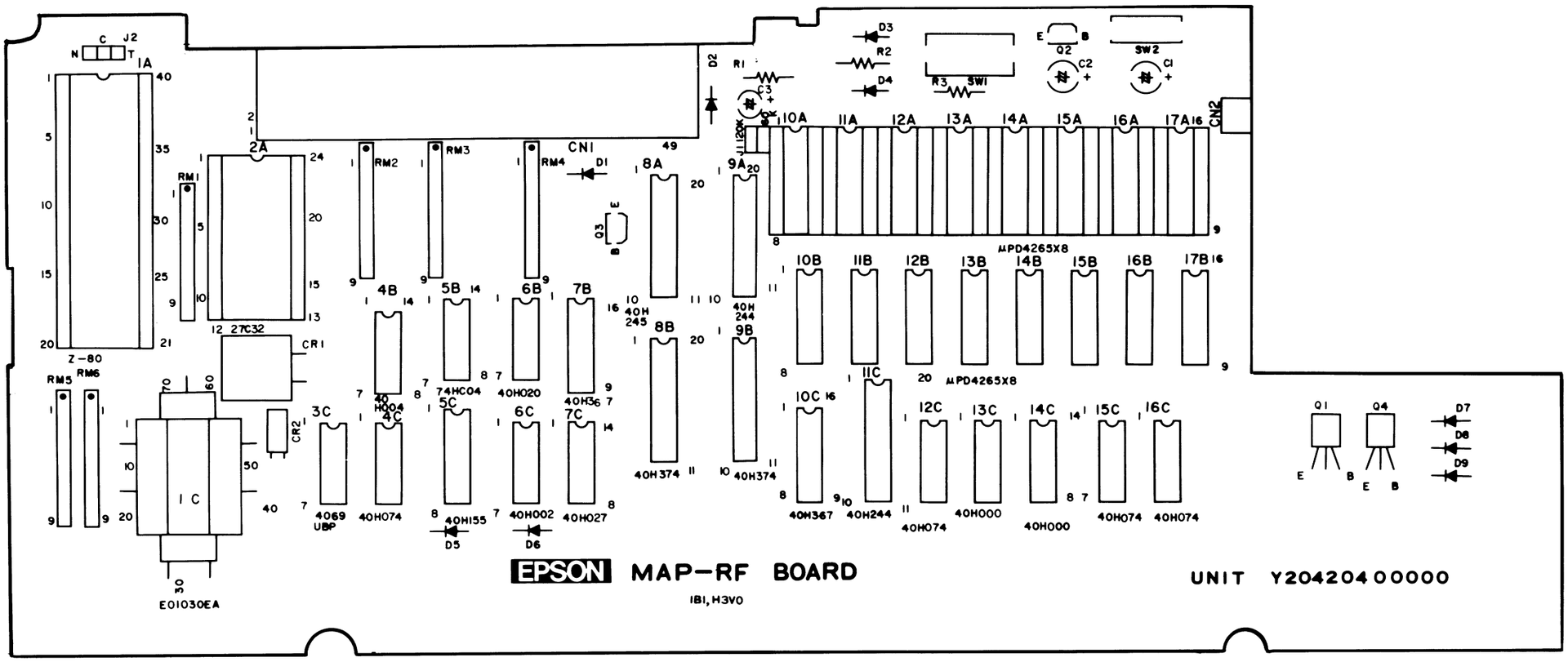


Fig. 3-45 DRAM Circuit Organization



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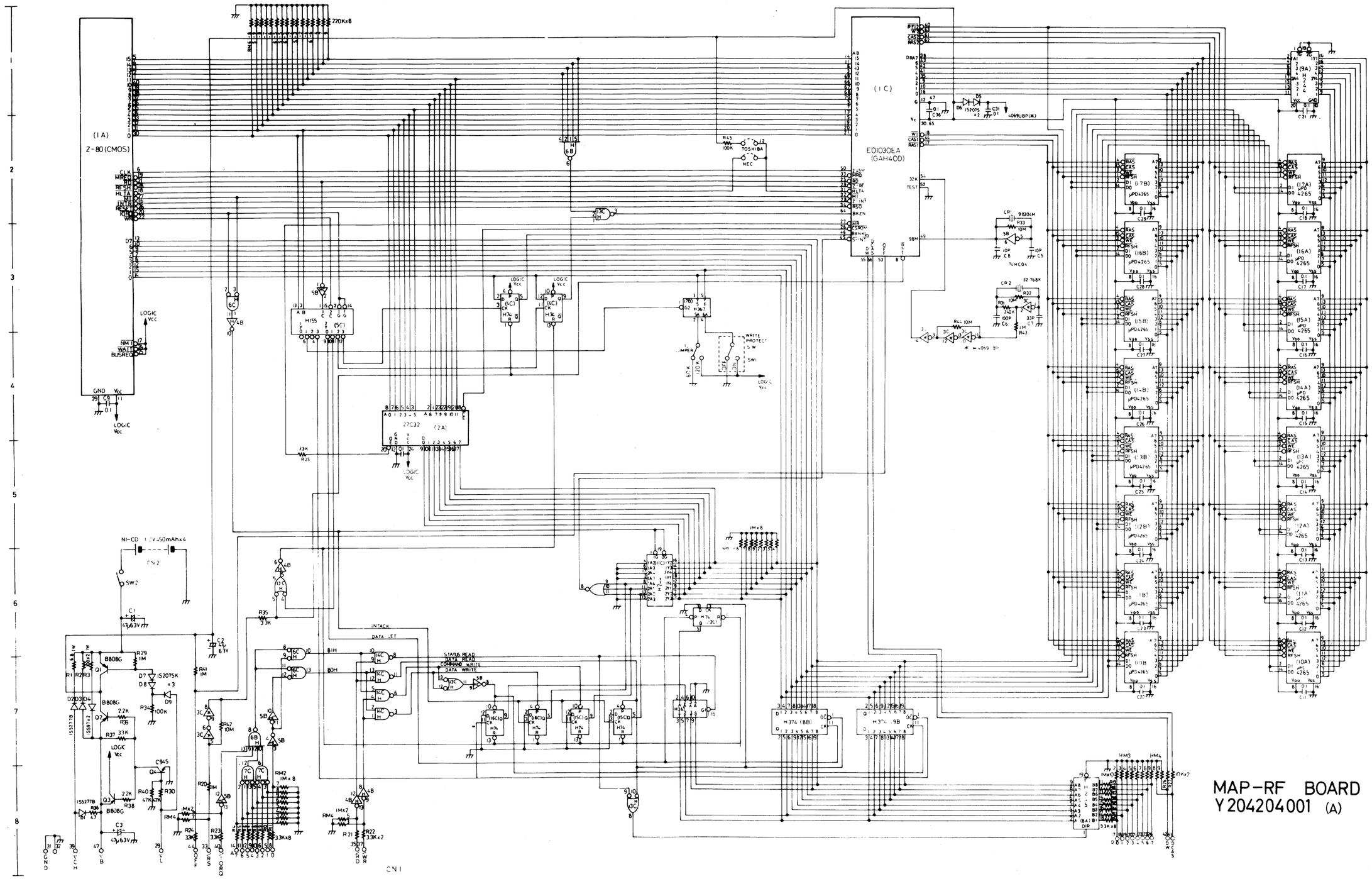
(1A)
Z-80(CMOS)
(1C)
E0I030EA
(GAH40D)
(1B)
MAP-RF BOARD
Y204204001 (A)