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Abstract:

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RCSL Nr. 46-F 0089

ENHED / BETEGNELSE

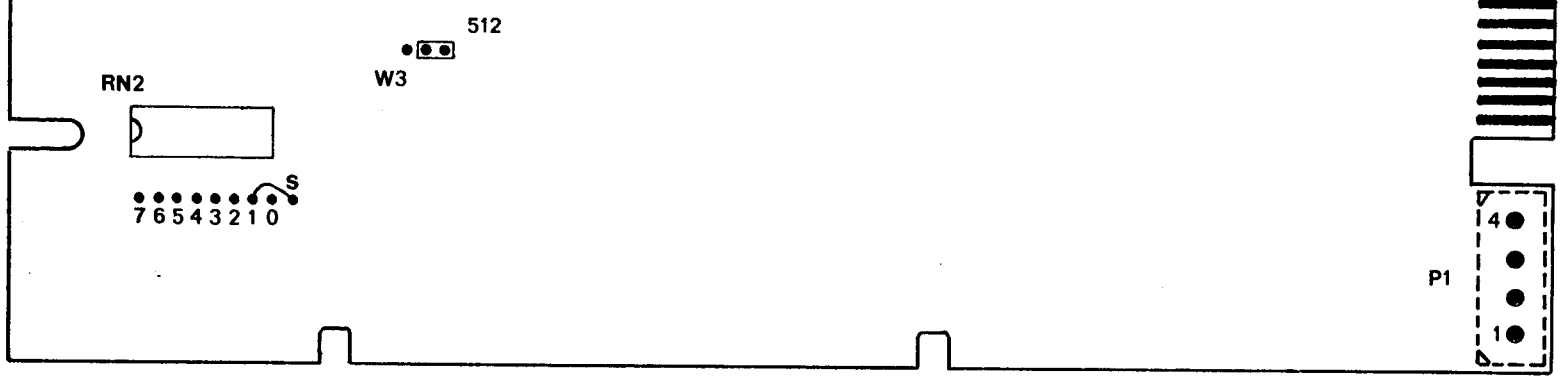
WDC 703

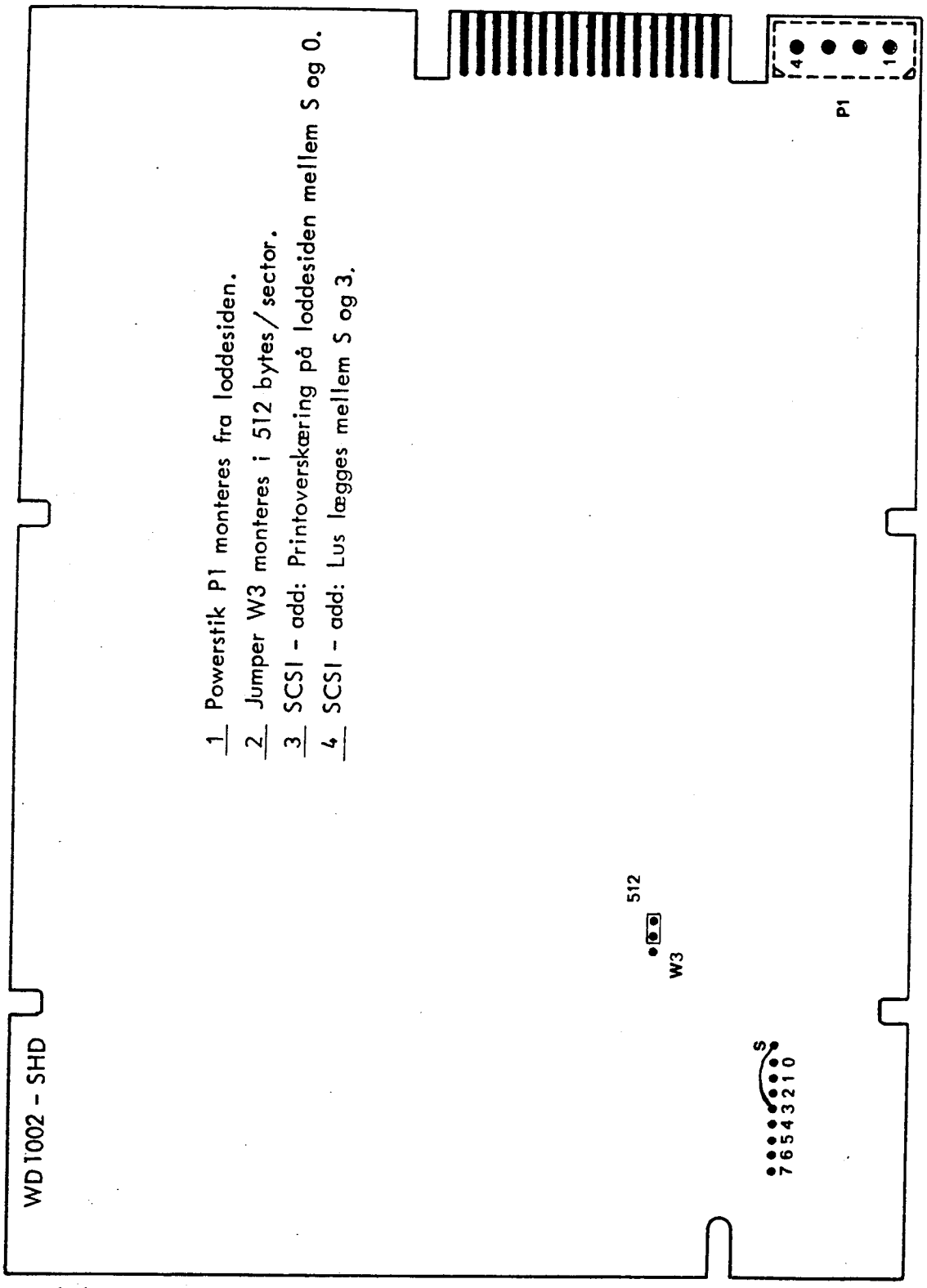
MODIFIKATION AF WD1002-SHD

	0	1	2	3	4	5	6
DATO / SIGN	850125HC						
TEGN NR	760 84340						

WD1002 - SHD

1. Terminering RN2 fjernes.
2. Powerstik P1 monteres fra loddesiden.
3. Jumper W3 monteres i 512 bytes/sector.
4. SCSI - add: Printoverskæring på loddesiden mellem S og 0.
5. SCSI - add: Lus lægges mellem S og 1.





forskel på 703 og 204 trådt på U n 38

ENHED / BETEGNELSE			
WDC 706 MODIFIKATION AF WD1002 - SHD			6
			5
			4
			3
			2
			1
	DATO / SIGN 850312 HK	TEGN NR 760 85 520	0

WD1002-SHD

Winchester

Controller

OEM Manual

Document No.: 79-000004

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August 1984

TABLE OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

SECTION I
INTRODUCTION

1.1 DOCUMENT SCOPE

This document provides the user with the information required to design related software drivers and interface connections for efficient use of the WD1002-SHD Winchester Disk Controller Board. It is to the user's advantage to become familiar with the following related documents:

WD1100-13 ECC Support Device ..... Data Sheet
WD1010-05 Winchester Disk Controller .. Data Sheet
WD1010-05 Winchester Disk Controller ..... Application Note
WD1015-02 Buffer Manager Control Processor ..... Data Sheet

1.2 DESCRIPTION

The WD1002-SHD is a stand alone, general purpose Winchester Controller Board designed to interface up to two Winchester Disk Drives to a Host Processor (Figure 1-1). The Winchester Drive signals are based upon the Seagate Technology ST506 interface and other compatible drives. All necessary receivers and drivers are included on the board to allow direct connection to the drive.

Communication to and from the Host are made via a separate computer access port. This port conforms to the popular Shugart Associates System Interface (SASI™) and consists of control signals and an 8-bit, bi-directional bus. All data to be written to or read from the disk, status information, and command parameters are transferred via this bus. An on-board Sector Buffer allows bus transfers to be executed independently of the actual data transfer of the drive.

The WD1002-SHD is based upon a Western Digital proprietary chip set consisting of the WD1015-02, WD1010-05, and WD1100-13, specifically designed for Winchester control.

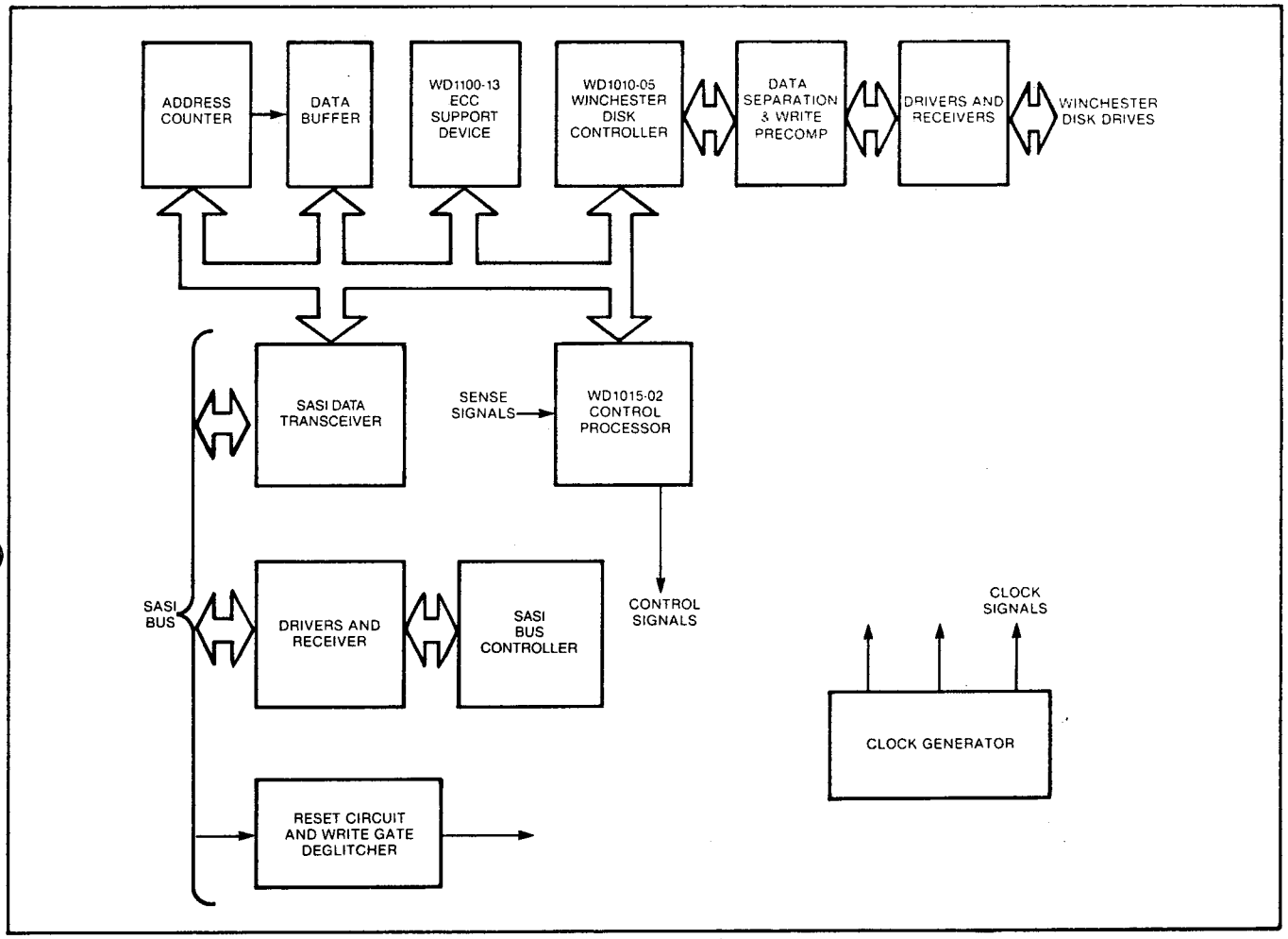


FIGURE 1-1. WD1002-SHD BLOCK DIAGRAM

SASI™ is a trademark of Shugart Associates

1.3 FEATURES

- SASI HOST INTERFACE
- 32-BIT ECC FOR WINCHESTER DATA CORRECTION
- BAD TRACK MAPPING CAPABILITY
- 256 OR 512 BYTES PER SECTOR
- MULTIPLE SECTOR READS AND WRITES
- CONTROL FOR UP TO 2 WINCHESTER DRIVES, WITH UP TO 8 R/W HEADS EACH
- DIAGNOSTIC READS AND WRITES FOR CHECKING ERROR CORRECTION
- AUTOMATIC FORMATTING
- SELECTABLE INTERLEAVE
- BUILT-IN DATA SEPARATOR
- BUILT-IN WRITE PRECOMPENSATION
- IMPLIED SEEKS
- SINGLE +5V SUPPLY
- OVERLAPPED SEEKS
- 0°C to 55°C OPERATIONS

1.4 OPERATION

1.4.1 GENERAL

With regard to bus operations, time can be partitioned into five phases:

Information Transfer
Reset
Bus Release
Bus Free
Target Selecting

1.4.2 BUS PHASE SEQUENCING

A Reset Phase may occur at any time. It is followed by the Bus Free Phase. In the absence of a Reset Phase the bus alternates between the Bus Free Phase and one Transaction.

A transaction always consists of the following sequence:

One Target Selection Phase
One or more Information Transfer Phases
One Bus Release Phase

The five bus phases are described in Section VI.

SECTION II
SPECIFICATIONS

2.1 GENERAL

This section contains the overall specifications for the WD1002-SHD Winchester Disk Controller. These specifications are provided as a guide for installing the WD1002-SHD. Certain specifications indicate limits associated with their parameters that must be adhered to in order to guarantee proper and efficient operation.

2.2 ELECTRICAL

2.2.1 HOST INTERFACE

Type	SASI
Max Cable Length	4.5 meters (15 ft.)
(Total Daisy Chain)	
Termination	Socketed 220/330 ohm resistor pack
Addressing	Jumper selectable 0 to 7

2.2.2 DRIVE INTERFACES

Encoding Method	MFM
Cylinders per Drive	Programmable
Bytes per Sector	Programmable (256 or 512)
Sectors per Track	32 (256 bytes/sector)
	17 (512 bytes/sector)
Head Selects	8
Drive Selects	2
Stepping Rates/Algorythms	Programmable
Data Transfer Rate	5 Mbits/sec
Write Precomp Time	12 nsec
Sectoring Soft	
Max Cable Length:	
Control (Total Daisy Chain)	6 Meters (20 ft.)
Data (Radial-each)	6 Meters (20 ft.)

2.2.3 POWER

Voltage	5 ±5%
Current	2.0 amps max, 1.5 amps typ.
Ripple	0.1 volts max, 0.1 to 25 mv.

2.3 PHYSICAL

Length	8 inches
Width	5.75 inches
Height (max including board, components, & leads)	0.75 inches

2.4 ENVIRONMENTAL

Ambient Temperature	0°C to 55°C
Relative Humidity	10% to 90% non-condensing
Altitude	0 to 3000 meters (10,000 ft)
Air Flow	100 lin ft/min. at 0.5" from component surfaces.

SECTION III
INTERFACE CONNECTIONS

3.1 ORGANIZATION

The WD1002-SHD has five on-board connectors for user application.

1. Host SASI Bus: 50-pin vertical header, mates to an AMP88379-8 (J1)
2. Winchester Drive Control: 34-pin PC card edge connector, mates to an AMP88373-3. (P2)
3. Winchester Drive Data: 20-pin vertical headers on .1" centers, mates to an AMP88377-4. (J2, J3)
4. Power: 4-pin connector, AMP1-480424-0 (Housing) AMP350078-4 (Pins). (P1)

Figure 1.1 is a block diagram illustrating the major sections and connectors of the controller.

3.2 HOST SASI INTERFACE CONNECTOR

The WD1002-SHD Controller is designed to interface with the Shugart Associates System Interface (SASI) bus. All interfacing is done through the J1 SASI connector. The Host and seven other SASI compatible devices can be daisy-chained to this bus, the last device on the daisy-chain must be terminated with a standard 220/330 ohm resistor pack.

The Controller is configured at the factory as address zero, but can be changed to an address of 1 thru 7 by the user.

TABLE 3.1 HOST INTERFACE CONNECTOR (J1) PIN DESCRIPTION

SIG. GND.	SIG. PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
1 3 5 7 9 11 13 15	2 4 6 8 10 12 14 16	$\overline{D0}$ thru $\overline{D7}$	$\overline{DATA\ 0}$ thru $\overline{DATA\ 7}$	I/O	8-Bit, tri-state, bi-directional bus used for the transfer of commands, status, and data.
17 thru 34		Spare			
35	36	$\overline{BSY}$	$\overline{BUSY}$	O	Falling edge acknowledges receipt of $\overline{SEL}$ and address. Rising edge indicates transaction complete
37	38	$\overline{ACK}$	$\overline{ACKNOWLEDGE}$	I	Handshake for byte transfers (both edges used).
39	40	$\overline{RST}$	$\overline{RESET}$	I	Asserted for 100 nsec.
41	42	$\overline{MSG}$	$\overline{MESSAGE}$	O	Indicates type of bus transfer (see Information Transfer Phase)
43	44	$\overline{SEL}$	$\overline{SELECT}$	I	Asserted, gives control of bus to addressed target.
45	46	$\overline{C/D}$	$\overline{COMMAND/DATA}$	O	Indicates type of bus transfer (see Information Transfer Phase)
47	48	$\overline{REQ}$	$\overline{REQUEST}$	O	Handshake for byte transfers (both edges used).
49	50	$\overline{I/O}$	$\overline{IN/OUT}$	I/O	L = Input to the Host H = Output from the Host (see Information Transfer Phase)

3.3 DRIVE CONTROL CONNECTOR

The control signals are common to both drives and are daisy-chained from a single 34 pin PC card edge connector, J1. To terminate the control signals properly, the last drive in the daisy-chain must not be more than 20 ft. from the controller, and have a 220/330 ohm resistor pack installed.

TABLE 3.2 DRIVE CONTROL CONNECTOR (P2) PIN DESCRIPTION

SIG. GND.	SIG. PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
1	2	$\overline{\text{RWC}}$	$\overline{\text{REDUCE WRITE CURRENT}}$	O	$\overline{\text{RWC}}$ is asserted when the Present Cylinder Number Register is equal to four times or greater than the content programmed in the Write Precomp Register. It is used by the drive to reduce drift caused by greater bit density on the inner cylinders.
3	4	$\overline{\text{HS2}}$	$\overline{\text{HEAD SELECT 2}}$	O	$\overline{\text{HS2}}$ is one of three Head Select signals encoded by the drive to select one of eight R/W heads.
5	6	$\overline{\text{WG}}$	$\overline{\text{WRITE GATE}}$	O	$\overline{\text{WG}}$ is asserted when valid data is to be written. It is used by the drive to enable the write current to the head. WD1002-SHD de-asserts this signal when $\overline{\text{WF}}$ is asserted. WD1002-SHD also prevents $\overline{\text{WG}}$ from being asserted at power up allowing the drive to remain on while cycling the controller on or off.
7	8	$\overline{\text{SC}}$	$\overline{\text{SEEK COMPLETE}}$	I	$\overline{\text{SC}}$, when asserted, informs the WD1002-SHD that the selected head has reached the desired cylinder and has stabilized.
9	10	$\overline{\text{TK000}}$	$\overline{\text{TRACK 000}}$	I	The drive asserts $\overline{\text{TK000}}$ when the heads are positioned over the outermost cylinder (track 0).
11	12	$\overline{\text{WF}}$	$\overline{\text{WRITE FAULT}}$	I	$\overline{\text{WF}}$ is asserted by the drive when a write error occurs.
13	14	$\overline{\text{HS0}}$	$\overline{\text{HEAD SELECT 0}}$	O	$\overline{\text{HS0}}$ is one of three Head Select signals encoded by the drive to select one of eight R/W heads.
15	16	NC	Not connected		
17	18	$\overline{\text{HS1}}$	$\overline{\text{HEAD SELECT 1}}$	O	$\overline{\text{HS1}}$ is one of three Head Select signals encoded by the drive to select one of eight R/W heads.
19	20	$\overline{\text{INDEX}}$	$\overline{\text{INDEX PULSE}}$	I	This signal indicates the start of a track. It is used as a synchronization point during formatting and as a time out mechanism for retries. This signal pulses once for each revolution of the disk.
21	22	$\overline{\text{DRDY}}$	$\overline{\text{DRIVE READY}}$	I	The drive asserts $\overline{\text{DRDY}}$ when it has been selected and the motor is up to speed.
23	24	$\overline{\text{STEP}}$	$\overline{\text{STEP PULSE}}$	O	$\overline{\text{STEP}}$, along with $\overline{\text{DIRIN}}$, positions the heads to the desired cylinder.
25	26	$\overline{\text{DSEL 0}}$	$\overline{\text{DRIVE SELECT 0}}$	O	$\overline{\text{DSEL 0}}$ is used to select drive 1.
27	28	$\overline{\text{DSEL 1}}$	$\overline{\text{DRIVE SELECT 1}}$	O	$\overline{\text{DSEL 1}}$ is used to select drive 2.
29	30	NC	Not connected		
31	32	NC	Not connected		
33	34	$\overline{\text{DIRIN}}$	$\overline{\text{DIRECTION IN}}$	O	$\overline{\text{DIRIN}}$ determines the direction the R/W heads take when stepped. Asserted = in, de-asserted = out.

3.4 DRIVE DATA CONNECTOR

The data is differential in nature and must be connected to each drive with its own cable, J2, J3. It should be a flat ribbon cable, or twisted pair, less than 20 ft. long. The connector is a 20 pin vertical header on .1" center.

TABLE 3.3 DRIVE DATA CONNECTORS — J2, J3

SIG. GND.	SIG. PIN	I/O	SIGNAL NAME
	1		NC
2			GND
	3		NC
4			GND
	5		NC
6			GND
	7		NC
8			GND
	9		NC
10			GND
	11		NC
12			GND
	13	O	+ MFM Write Date
	14	O	– MFM Write Date
15			GND
16			GND
	17	I	+ MFM Read Data
	18	I	– MFM Read Data
19			GND
20			GND

NOTE:

The WD1002-SHD must have Drive 0 connected to J2 and Drive 1 connected to J3.

3.5 POWER CONNECTOR

Power is brought to the WD1002-SHD via P1, a 4-pin Amp 1-480424 connector. The connections are made as shown:

PIN	SIGNAL NAME
1	NOT CONNECTED
2	GROUND
3	GROUND
4	+ 5V REGULATED

3.6 DISK DRIVE CONFIGURATION PARAMETERS

Table 3-4 lists the variable parameters for the major drives supported by the WD1002-SHD. These parameters are the values used in the Initialize Drive Characteristics Command (OC).

TABLE 3-4. DISK DRIVE CONFIGURATION PARAMETER VARIATIONS

MFGR	MODEL #	CYLINDERS	HEADS	REDUCED WRITE CURRENT CYL.	WRITE PRECOMPENSATION CYLINDER
CMI	CM-5205	256 (100)	2	256 (100)	256 (100)
CMI	CM-5410	256 (100)	4	256 (100)	256 (100)
CMI	CM-5616	256 (100)	6	256 (100)	256 (100)
OLI	HD561	180 (B4)	2	128 (80)	180 (B4)
OLI	HD562	180 (B4)	2	128 (80)	180 (B4)
RMS	503	153 (99)	2	77 (4B)	77 (4B)
RMS	506	153 (99)	4	77 (4B)	77 (4B)
RMS	512	153 (99)	8	77 (4B)	77 (4B)
SEA	ST506	153 (99)	4	128 (80)	64 (40)
SEA	ST412	306 (132)	4	128 (80)	64 (40)
TAN	TM602S	153 (99)	4	128 (80)	153 (99)
TAN	TM603S	153 (99)	6	128 (80)	153 (99)
TAN	TM603SE	230 (E6)	6	128 (80)	128 (80)
TI	5 1/4 +	153 (99)	4	64 (40)	64 (40)
RO	101	192 (C0)	2	96 (60)	0 (0)
RO	102	192 (C0)	4	96 (60)	0 (0)
RO	103	192 (C0)	6	96 (60)	0 (0)
RO	104	192 (C0)	8	96 (60)	0 (0)
RO	201	321 (141)	2	132 (84)	0 (0)
RO	202	321 (141)	4	132 (84)	0 (0)
RO	203	321 (141)	6	132 (84)	0 (0)
RO	204	321 (141)	8	132 (84)	0 (0)
MS	1-006	306 (132)	2	153 (99)	0 (0)
MS	1-012	306 (132)	4	153 (99)	0 (0)

DRIVE MANUFACTURERS ABBREVIATIONS:

CMI Computer Memories Inc.
OLI Oliveti
RMS Rotating Memory Systems Inc.
SEA Seagate Technology Inc.
TAN Tandon Inc.
TI Texas Instruments
RO Rodime Ltd.
MS Miniscribe

SECTION IV
COMMANDS

4.1 GENERAL

The WD1002-SHD supports 20 different SCSI commands; 15 operational commands and 5 diagnostic commands. Table 4-1 lists a summary of the supported commands.

4.2 COMMAND BLOCKS

A transaction is initiated by the Host to instruct the WD1002-SHD to execute a given command. During the Command Block Transfer Phase (discussed in Section VI), six bytes of information specifying the command are transferred to the WD1002-SHD. This is known as the Command Block and is illustrated in Figure 4-1.

	BITS							
BYTES	7	6	5	4	3	2	1	0
0	Command Class			Operational Code				
1	Logical Unit Num			Logical Sector Address (High)				
2	Logical Sector Address (Middle)							
3	Logical Sector Address (Low)							
4	Interleave or Block Count							
5	Control Byte							

FIGURE 4-1. COMMAND BLOCK FORMAT

Byte 0 is transferred first and must be specified for all commands. Each command has exactly one Byte 0 value associated with it.

Depending upon the value of Byte 0, each parameter in bytes 1 thru 5 may require specification. Table 4-1 specifies the supported commands and their parameters. It also includes information on data transfers required during execution. All other SASI commands are reserved.

4.2.1 LOGICAL UNIT NUMBER (LUN)

The LUN is contained in the three MSBits of Byte 1. The allowed values are 0 and 1. The designators in the command table are; Drive 0 (LUN = 0) or Drive 1 (LUN = 1).

4.2.2 LOGICAL SECTOR ADDRESS (L)

The Logical Sector Address (High, Middle, and Low) is a 21 bit field contained in Bytes 1, 2, and 3. It is computed from the Cylinder Address (C), Head Address (H), and Sector address (S), as well as the drive parameters Heads per Cylinder (HC) and Sectors per Track (ST):

$$L = \{[(C \times HC) + H] \times ST\} + ST$$

C, H, and S can be derived from L, HC, and ST as follows:

$$S = L \text{ Modulo } ST$$
$$H = [(L - S) / ST] \text{ Modulo } HC$$
$$C = \{[(L - S) / ST] - H\} / HC$$

This field specifies a sector (or beginning sector) for the Read and Write Drive Commands. It specifies a track for the Format and Seek Commands (indicated by L* in Table 4-1). When only a track specification is required, the sector number implied by the Logical Sector Address is ignored.

4.2.3 INTERLEAVE OR BLOCK COUNT

The Interleave or Block Count comprise Byte 4. The Interleave ratio (I in Table 4-1) is specified in the five Format commands. The maximum ratio is equal to the Sectors-per-Track minus 1.

The Block Count (B in Table 4-1) is specified in the Read, Write, Read Long, and Write Long commands. B specifies the number of Logical Sectors to be transferred.

Both Interleave ratio and Block Count use all 8 bits of the Byte to specify their respective parameters.

TABLE 4-1. WD1002-SHD SUPPORTED COMMAND SUMMARY

COMMAND NAME	CLASS, OPCODE	LUN	LOGICAL SECTOR ADDRESS	INTERLEAVE OR BLOCK COUNT	CONTROL BYTE OPTIONS	# SCSI DATA BLOCK TRNSFRS	D.B. SIZE	DIREC-TOR
Test Drive Ready	0,0	W	—	—	—	0	—	—
Restore to Track 0	0,1	W	—	—	—	0	—	—
Req Status	0,3	W	—	—	—	1	4	To Host
FRMT Drive	0,4	W	L*	I	R,P,S,	0	—	—
CHK TR FRMT	0,5	W	L*	I	R,S	0	—	—
Format Drive	0,6	W	L*	I	R,P,S	0	—	—
FRMT Bad TRK	0,7	W	L*	I	R,P,S	0	—	—
Read Drive	0,8	W	L	B	R,A,S	B	SCTR	To Host
Write Drive	0,A	W	L	B	R,S	B	SCTR	To CTLR
Seek	0,B	W	L*	—	R,S	0	—	—
Winchester Parameters	0,C	W	—	—	—	1	8	To CTLR
Return Burst Error Length	0,D	W	—	—	—	1	1	To Host
FRMT ALT TRK	0,E	W	L*	I	R,P,S	1	3	To CTLR
WR SCT BFR	0,F	—	—	—	—	1	—	To CTLR
RD SCT BFR	0,10	—	—	—	—	1	—	To Host
RAM DIAG	7,0	—	—	—	—	0	—	—
Drive DIAG	7,3	W	—	—	R,S	0	—	—
CTLR DIAG	7,4	—	—	—	—	0	—	—
RD Drive Long	7,5	W	L	B	R,S	B	— SECT +4	To Host
WR Drive Long	7,6	W	L	B	R,S	B	— SECT +4	To CTLR

LEGEND

W Winchester
L* Logical sector address used only to specify track
L Logical sector address
I Interleave
B Block count
R Retry enable/disable
A Attempt immediate ECC enable/disable
S Stepping algorythm
P Used with format commands for determining data field patterns

4.2.4 WD1002-SHD CONTROL BYTES

Table 4-2 specifies the Control Byte fields:

TABLE 4-2. CONTROL BYTE FIELDS

FIELD	BIT(S)	FUNCTION
STEP	0-3	Used in all commands that cause a seek. Contains a code corresponding to a seek stepping algorythm. See Fast Step Options.
UNUSED	4	Reserved.
P	5	Format Data (P) is used in the Format Commands. If P = 0, the WD1002-SHD fills the data field with 6C hex. If P = 1, the data field is filled with the pattern in the Sector Buffer.
A	6	Immediate ECC (A) is used in the Read Command. If A = 0, no immediate ECC is performed. If A = 1, immediate ECC is performed.
R	7	Retry (R) is used in all commands that read the ID field. If R = 0 (normal), a maximum of 10 non-restore retries are performed, then Restore, Seek, and 10 more retries are performed if necessary. If R = 1, Retry is disabled and no retries are performed.

NOTE:

If one or more of the above fields are required for a command, then all other fields in that Control Byte must be set to 0. If none of the above are required, all bits in the Control Byte are interpreted as "don't care" bits (X).

4.2.4.1 Fast Step Options

The Fast Step Option field contains an unsigned 3-bit integer. These integers correspond to the Fast Step Algorythms in Table 4-3.

TABLE 4-3.
FAST STEP OPTION ALGORYTHMS

OPTION	ALGORYTHM
0	Default: 3 msec. per step
1	Half-step for Seagate drives
2	3 msec.
3	Half-step for T.I. drives
4	200 usec. per step. This is appropriate for buffered steps on drives made by Computer Memories Inc. and Rotating Memories Inc.
5	70 usec. per step
6	30 usec. per step
7	15 usec. per step
8	2 msec. per step
9	3 msec. per step
B-F	Spare (3 msec. per step)

4.2.4.2 Command Status Byte

At the completion of any command execution, a Command Status Byte is sent by the WD1002-SHD to the Host, whether the command was successful or aborted. The LUN returned is the contents of the LUN field in the drive control block. For those commands that do not use LUN as an input parameter, the LUN returned in the Command Status Byte is meaningless. Figure 4-2 illustrates the contents of the Command Status Byte.

BITS							
7	6	5	4	3	2	1	0
LUN			0	0	0	EF	0

EF (Error Flag): 0 = no error
1 = error

FIGURE 4-2. COMMAND STATUS BYTE

4.2.4.3 Command Completion Byte

The Command Completion Byte is an all zero byte sent by the WD1002-SHD to the Host immediately following each Command Status Byte. It indicates to the Host that the WD1002-SHD has freed the SASI bus.

4.3 COMMANDS

Each command in the Command Summary table is described in the following text.

4.3.1 TEST DRIVE READY (CLASS 0, OPCODE 00)

This command selects a drive and verifies that it is ready. The following shows the Test Drive Ready Command Block format.

	BITS							
BYTES	7	6	5	4	3	2	1	0
0	Command Class 0			Operational Class 00				
1	LUN			X	X	X	X	X
2	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X
4	X	X	X	X	X	X	X	X
5	X	X	X	X	X	X	X	X

Possible Error Codes

No error, invalid command, no seek complete, drive not ready, or write fault.

Action

Select the drive and determine if it is ready. For a Winchester drive, read its status register and test the ready bit and busy bit. For Winchester drives supporting buffered seeks, this command is useful for determining the first drive to reach its target track.

4.3.2 RESTORE TO TRACK 0 (CLASS 0, OPCODE 01)

This command positions the read/write heads to Track 0.

	BITS							
BYTES	7	6	5	4	3	2	1	0
0	Command Class 0			Operational Class 01				
1	LUN			X	X	X	X	X
2	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X
4	X	X	X	X	X	X	X	X
5	X	0	0	0	X	X	X	X

Possible Error Codes

No error, invalid command, Track 0 not found, drive not ready, or write fault.

Action

Position the heads to cylinder 0.

4.3.3 REQUEST STATUS (CLASS 0, OPCODE 03)

The Host must send this command immediately after it detects an error. The command causes the WD1002-SHD to return four bytes of drive and Controller status. When an error occurs on a multiple sector data transfer (read or write), the Request Status Command returns the Logical Sector Address of the failing sector in bytes 1, 2, and 3. If the Request Status Command is issued after any of the format commands or the Check Track Format Command, then the Logical Sector Address points to one sector beyond the last track formatted or checked if there was no error. If there was an error, then the Logical Address returned points to the track in error.

The following is the Request Status Command Block format.

	BITS							
BYTES	7	6	5	4	3	2	1	0
0	Command Class 0			Operational Class 03				
1	LUN			X	X	X	X	X
2	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X
4	X	X	X	X	X	X	X	X
5	X	X	X	X	X	X	X	X

Possible Error Codes

No error or invalid command.

Action

Send the Host 4 bytes; the error byte and a 3-byte Logical Sector Address for the specified drive.

4.3.3.1 Error/Status Response To Host

The following non-drive error codes are treated as Drive 0 errors: RAM Failure (30), ROM failure (31), ECC failure (32). Hence, if the RAM Diagnostic Command or Controller Diagnostic Command detects an error, then status for Drive 0 should be requested.

	BITS							
BYTES	7	6	5	4	3	2	1	0
0	LSAF	0	Error Codes					
1	LUN			Log Sect Address Bits 16-21				
2	Logical Sector Address Bits 8-15							
3	Logical Sector Address Bits 0-7							

LSAF: 0 = Sector Address Not Valid
1 = Sector Address Valid

4.3.3.2 Error Codes

A. DISK DRIVE ERROR CODES
- 00 = No Error
- 03 = Write Fault
- 04 = Drive Not Ready
- 06 = Track 0 Not Found

B. CONTROLLER ERROR CODES
01,02
- 10/14 = Not used because the WD1010 groups CRC with other errors in the ID field as ID Not Found. Therefore, during implied Seeks, these are called seek errors Code 15.
- 11 = Uncorrectable Data Error
- 12 = Address Mark Not Found
- 15 = Seek Error
- 18 = Error Burst Corrected
- 19 = Bad Track
- 1A = Format Error
- 1C = Illegal (Direct) Access To An Alternate Track
- 1D = Alternate Track Already Used
- 1E = Alternate Track Not Marked As Alternate
- 1F = Alternate Track Equals Bad Track

C. COMMAND ERROR CODES
- 20 = Invalid Command
- 21 = Invalid Sector Address

D. MISCELLANEOUS ERROR CODES
- 30 = RAM Failure
- 31 = ROM Failure
- 32 = ECC Hardware Failure

If the most recent non-request-status command to the specified drive required a Logical Sector Address, then the LSA flag is 1, otherwise it is 0 and the Logical Sector Address is meaningless.

4.3.3.3 Error Code Descriptions

No Error (00)

No error detected during the previous operation.

Write Fault (03)

Indicates that there is Write Current to the head when $\overline{WG}$ is de-asserted. This is a very serious problem and should be remedied immediately.

Drive Not Ready (04)

The drive does not respond with a Drive Ready signal after being selected by the WD1002-SHD.

Track 0 Not Found (06)

This error is only returned by the Restore To Track 0 Command. It indicates that Track 0 status from the drive was not asserted within the maximum number of steps towards cylinder 0.

Uncorrectable Data Error (11)

This error indicates that one or more error bursts within the data field (Winchester) were beyond the Error Correction capabilities of the WD1002-SHD. The sector data for this sector is not sent to the Host.

Address Mark Not Found (12)

This error indicates that the header for the Target Sector was found, but its Address Mark was not detected.

Seek Error (15)

The WD1002-SHD detects an incorrect cylinder or track, or both.

Error Burst Corrected (18)

Indicates that ECC was used to successfully correct an error. The corrected sector data is sent to the Host.

Bad Track (19)

This error usually indicates access of a track that was formatted as a bad track. However, there is a very small chance that it indicates that a track formatted as a bad track with alternate is so faulty that none of the multiple, duplicate pointers to the alternate track can be read.

Format Error (1A)

This error code is returned by the Check Track Format Command. It indicates that the track is not formatted with the specified interleave factor, or at least one sector header is unreadable. This error code is returned by the Drive Diagnostic Command to indicate that bad-track-with-alternate does not contain a valid pointer to the alternate track.

Illegal (Direct) Access To An Alternate Track (1C)

Alternate Track Already Used (1D)

This error code is only returned by the Format Alternate Track Command. It indicates that the specified alternate track is already an alternate, or bad track.

Alternate Track Already Used (1D)

This error code is only returned by the Format Alternate Track Command. It indicates that the specified alternate track is already an alternate, or bad track.

Alternate Track Not Marked As An Alternate (1E)

This error code indicates that access of a bad-track-with-alternate caused access to an alternate track which was not marked as an alternate.

Alternate Track Equals Bad Track (1F)

This error code is only returned by the Format Alternate Track Command. It indicates that the same track was specified as the bad track and the alternate track.

Invalid Command (20)

This error code indicates that the Command Code, Interleave Factor, or Fast Step Option was invalid.

Invalid Sector Address (21)

This error code indicates that the WD1002-SHD, detected a Sector Address beyond the maximum range.

RAM Failure (30)

This error code indicates one of the following conditions: (1) The program memory RAM checksum does not match the calculated checksum; (2) The RAM in the Control Processor failed; (3) The Control Processor CPU failed.

ROM Failure (31)

This error code indicates that a ROM checksum error occurred during internal diagnostics.

ECC Hardware Failure (33)

This error code indicates that the ECC Support Device failed during internal diagnostics.

4.3.4 FORMAT DRIVE (CLASS 0, OPCODE 04)

This command formats all sectors with ID and data fields according to the selected interleave factor. This command also writes 6C Hex into the data fields. The starting address is passed into the Control Byte which is read by the WD1002-SHD. The Controller then formats from this address to the end of the disk.

The following is the Format Drive Command Block format.

	BITS							
BYTES	7	6	5	4	3	2	1	0
0	Command Class 0			Operation Code 04				
1	LUN			Log Sec Address Bits 16-21				
2	Logical Sector Address Bits 8-16							
3	Logical Sector Address Bits 0-7							
4	Interleave Factor							
5	R	0	P	0	Fast Step Option			

R Retry Disable: 0 = No Disable
1 = Disable

P Format Data: 0 = 6C Hex
1 = Contents of Sector Buffer

Possible Error Codes

No error, invalid command, invalid Sector Address, drive not ready, seek error, or write fault.

Action

Format from the specified track to the end of the disk. The previous contents of the formatted tracks are ignored.

4.3.5 CHECK TRACK FORMAT (CLASS 0, OPCODE 05)

This command checks the format on the specified track for correct ID and interleave. The command does not read the data field.

The following is the Check Track Format Command Block format.

	BITS							
BYTES	7	6	5	4	3	2	1	0
0	Command Class 0			Operation Code 05				
1	LUN			Log Sec Address Bits 16-21				
2	Logical Sector Address Bits 8-15							
3	Logical Sector Address Bits 0-7							
4	Interleave Factor							
5	R	0	0	0	Fast Step Option			

R Retry Disable: 0 = No Disable
1 = Disable

Possible Error Codes

No error, invalid command, invalid Sector Address, seek error, format error, drive not ready, or write fault.

Action

Verify that the specified track is formatted with the specified interleave factor. Do not read the sector data fields.

4.3.6 FORMAT TRACK (CLASS 0, OPCODE 06)

This command formats a specified track and can be used to clear bad-sector flags in all sectors on the specified track that was previously formatted with the Format Bad Track Command. The command writes 6C Hex into all data fields specified.

The following shows the Format Track Command Block format.

	BITS							
BYTES	7	6	5	4	3	2	1	0
0	Command Class 0			Operation Code 06				
1	LUN			Log Sec Address Bits 16-21				
2	Logical Sector Address Bits 8-15							
3	Logical Sector Address Bits 0-7							
4	Interleave Factor							
5	R	0	P	0	Fast Step Option			

R Retry Disable: 0 = No Disable
1 = Disable

P Format Data: 0 = 6C Hex
1 = Contents of Sector Buffer

Possible Error Codes

No error, invalid command, invalid Sector Address, drive not ready, seek error, or, write fault.

Action

Format the specified track, ignoring the previous contents.

4.3.7 FORMAT BAD TRACK (CLASS 0, OPCODE 07)

This command formats the specified track and sets the bad-sector flag in the ID fields. It does not write to the data fields. The following illustrates the Format Bad Track Command Block format.

	BITS							
BYTES	7	6	5	4	3	2	1	0
0	Command Class 0			Operational Code 07				
1	LUN			Log Sec Address Bits 16-21				
2	Logical Sector Address Bits 8-16							
3	Logical Sector Address Bits 0-7							
4	Interleave Factor							
5	X	0	0	0	Fast Step Option			

Possible Error Codes

No error, invalid command, invalid Sector Address, drive not ready, or write fault.

Action

Format the specified track with a bad block mark in each sector header, ignoring the previous contents. The contents of a bad track are not accessible.

4.3.8 READ (CLASS 0, OPCODE 08)

This command reads the specified number of sectors, starting with the initial Sector Address contained in the Control Byte. The following shows the Read Command Block format.

	BITS							
BYTES	7	6	5	4	3	2	1	0
0	Command Class 0			Operational Code 08				
1	LUN			Log Sec Address Bits 16-21				
2	Logical Sector Address Bits 8-15							
3	Logical Sector Address Bits 0-7							
4	Sector Count							
5	R	A	0	0	Fast Step Option			

R Retry Disable: 0 = No Disable
1 = Disable

A Attempt ECC: 0 = No Immediate Correction
1 = Immediate ECC

Possible Error Codes

No error, invalid command, invalid Sector Address, drive not ready, seek error, bad track, illegal (direct) access to an alternate track, alternate track not marked as an alternate, Address Mark not found, error burst corrected, uncorrectible data error, or write fault.

Action

Read the specified number of consecutive sectors beginning with the specified Sector Address contained in the Control Byte.

4.3.9 WRITE (CLASS 0, OPCODE 0A)

This command writes the specified number of sectors, beginning with the initial sector address contained in the Control Byte. The following shows the Write Command Block format.

	BITS							
BYTES	7	6	5	4	3	2	1	0
0	Command Class 0			Operational Code 0A				
1	LUN			Log Sec Address Bits 16-21				
2	Logical Sector Address Bits 8-15							
3	Logical Sector Address Bits 0-7							
4	Sector Count							
5	R	0	0	0	Fast Step Option			

R Retry Disable: 0 = No Disable
1 = Disable

Possible Error Codes

No error, invalid command, invalid Sector Address, drive not ready, seek error, bad track, illegal (direct) access to an alternate track, alternate track not marked as an alternate, address mark not found, or write fault.

Action

Write the specified number of sectors beginning with the specified Sector Address contained in the Control Byte.

4.3.10 SEEK (CLASS 0, OPCODE 0B)

This command initiates a seek to the track specified in the Control Byte. The drive must be formatted.

The following shows the Seek Command Block format.

	BITS							
BYTES	7	6	5	4	3	2	1	0
0	Command Class 0			Operational Code 0B				
1	LUN			Log Sec Address Bits 16-21				
2	Logical Sector Address Bits 8-15							
3	Logical Sector Address Bits 0-7							
4	X	X	X	X	X	X	X	X
5	X	0	0	0	Fast Step Option			

Possible Error Codes

No error, invalid command, invalid Sector Address, drive not ready, or write fault.

Action

Move the read/write head to the specified cylinder. Do not read any sector header to verify start or end position.

4.3.11 SET PARAMETERS (CLASS 0, OPCODE 0C)

This command enables the Host to configure the WD1002-SHD to work with drives that have different capacities and characteristics. However, both drive 0 and drive 1 must be of the same manufacturer and model number. The following shows the Set Parameters Command Block format.

	BITS							
BYTES	7	6	5	4	3	2	1	0
0	Command Class 0			Operational Code 0C				
1	X	X	X	X	X	X	X	X
2	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X
4	X	X	X	X	X	X	X	X
5	X	X	X	X	X	X	X	X

Possible Error Codes

If parameters are out of range, an INVALID COMMAND error will be set.

Action

Set the following parameters for both Winchester drives (LUN 0 and 1): Number of cylinders; Number of heads; Starting Reduced Write Current cylinder; Starting Write Precompensation cylinder; and the maximum length of an error burst to be corrected. These parameters are sent by the Host to the WD1002-SHD in a parameter block with the following format:

4.3.11.1 Parameter Blocks

After the Host sends the Set Parameters Command Block to the WD1002-SHD, it then sends an 8-byte block of data that contains the required drive parameters. Some parameters occupy two bytes; all two-byte parameters are transferred with the Most Significant Byte first. The following shows the 8-byte Parameter Block format.

BYTES	BITS 7	6	5	4	3	2	1	0
0	MSByte of Number of Cylinders							
1	LSByte of Number of Cylinders							
2	0	0	0	0	Number of Heads			
3	MSByte of Starting RWC Cylinder							
4	LSByte of Starting RWC Cylinder							
5	MSByte of Starting Write Precomp Cylinder							
6	LSByte of Starting Write Precomp Cylinder							
7	0	0	0	0	Max ERR Burst Corrected			

The following parameter defaults are set by power-up and reset:

Number of cylinders = 153
Number of heads = 4
Starting Reduced Write Current Cylinder = 128
Starting Write Precompensation Cylinder = 64
Maximum length of an error burst to be corrected = 11

The acceptable ranges for the following parameters are:

Number of cylinders = 1-1024
Number of heads = 1-8
Starting Reduced Write Current Cylinder = 0-1023
Starting Write Precompensation Cylinder = 0-1023
Maximum length of an error burst to be corrected = 1-11

If one of the parameters is out of range, then all parameters up to, but not including the parameter in error, are set for drive 0 and no parameters are set for drive 1. The error code for this error is INVALID COMMAND.

Starting Reduced Write Current Cylinder

The specified starting Reduced Write Current cylinder number is reduced to the nearest integer multiple of four (i.e. 0, 4, 8, 12, . . . 1020).

Maximum Length Of Error Burst To Be Corrected

For Practically all applications, the maximum length of error burst to be corrected should be five. Correcting longer bursts greatly increases the chance of miscorrecting.

4.3.12 LAST CORRECTED BURST LENGTH (CLASS 0, OPCODE 0D)

This command transfers one byte to the Host containing the values of the ECC burst length detected by the WD1002-SHD during the last Read Command. This byte is only valid after a correctable ECC error (18).

BYTES	BITS 7	6	5	4	3	2	1	0
0	Command Class 0			Operational Code 0D				
1	X	X	X	X	X	X	X	X
2	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X
4	X	X	X	X	X	X	X	X
5	X	X	X	X	X	X	X	X

Possible Error Codes

No error

Action

Send the Host one byte of data containing the length of the most recently corrected error burst. If no error burst has been corrected since the last power-up or reset, then a byte of zeroes is sent to the Host.

4.3.12.1 Error Burst Length Block

BYTES	BITS 7	6	5	4	3	2	1	0
0	Number of bits in last corrected error burst							

4.3.13 FORMAT ALTERNATE TRACK (CLASS 0, OPCODE 0E)

BYTES	BITS 7	6	5	4	3	2	1	0
0	Command Class 0			Operational Code 0E				
1	LUN			Log Sec Address Bits 16-21				
2	Logical Sector Address Bits 8-15							
3	Logical Sector Address Bits 0-7							
4	Interleave Factor							
5	R	0	P	0	Fast Step Option			

R Retry Disable: 0 = No Disable
1 = Disable

P Format Data: 0 = 6C Hex
1 = Contents of Sector Buffer

Possible Error Codes

No error, invalid command, invalid Sector Address, drive not ready, seek error, alternate track already used, alternate track equals bad track, or write fault.

Action

Format the specified track as a bad-track-with-alternate. Format the specified alternate track with the specified interleave factor. The Bad Block Mark is written in each sector header with the alternate address block written into each sector data field. This is done to all sectors of the track. It is not known to the user which sector of the track might be bad. The alternate track is specified by the Host by sending an alternate sector address block to the WD1002-SHD after the Command Block. The alternate track is formatted after the bad-track-with-alternate is formatted. Once the alternate is formatted, the bad track to alternate seeking is transparent to the user.

4.3.13.1 Alternate Sector Address Block

	BITS							
BYTES	7	6	5	4	3	2	1	0
0	0	0	0	LOG SEC Address Bits 16-21				
1	Logical Sector Address Bits 8-15							
2	Logical Sector Address Bits 0-7							

4.3.14 WRITE SECTOR BUFFER (CLASS 0, OPCODE 0F)

	BITS							
BYTES	7	6	5	4	3	2	1	0
0	Command Class 0			Operational Code 0F				
1	X	X	X	X	X	X	X	X
2	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X
4	X	X	X	X	X	X	X	X
5	X	X	X	X	X	X	X	X

Possible Error Codes

No errors.

Action

Write data from the Host to the WD1002-SHD Sector Buffer. The Host must send as many bytes as there are in a sector on drive 0. This data is not written to any drive. This command is used to initialize the format data optionally used by the format commands.

4.3.15 READ SECTOR BUFFER (CLASS 0, OPCODE 10)

	BITS							
BYTES	7	6	5	4	3	2	1	0
0	Command Class 0			Operational Code 10				
1	X	X	X	X	X	X	X	X
2	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X
4	X	X	X	X	X	X	X	X
5	X	X	X	X	X	X	X	X

Possible Error Codes

No error.

Action

Send the Host the present contents of the WD1002-SHD Sector Buffer. The Host must accept as many bytes as there are in a sector on Drive 0.

4.3.16 RAM DIAGNOSTIC (CLASS 7, OPCODE 0)

This command performs a data pattern test on the Sector Buffer. The Host does not preserve the contents of the Sector Buffer. The following shows the RAM Diagnostic Command Block format.

	BITS							
BYTES	7	6	5	4	3	2	1	0
0	Command Class 7			Operational Code 0				
1	X	X	X	X	X	X	X	X
2	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X
4	X	X	X	X	X	X	X	X
5	X	X	X	X	X	X	X	X

Possible Error Codes

No error or RAM failure.

Action

Test the Sector Buffer by writing and reading various patterns into it.

4.3.17 DRIVE DIAGNOSTIC (CLASS 7, OPCODE 3)

This command tests both the drive and the drive-to-Controller interface. The WD1002-SHD sends Restore to Track 0 and Seek commands to the selected drive, and verifies Sector 0 of all tracks on the disk. The

WD1002-SHD does not perform any write operations during this command; the disk is understood to be previously formatted. The following shows the Drive Diagnostic Command Block format.

	BITS							
BYTES	7	6	5	4	3	2	1	0
0	Command Class 7			Operational Code 03				
1	LUN			X	X	X	X	X
2	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X
4	X	X	X	X	X	X	X	X
5	R	0	0	0	Fast Step Option			

R Retry Disable: 0 = No Disable
1 = Disable

Possible Error Codes

No error, invalid command, drive not ready, seek error, format error, or write fault.

Action

Recalibrate the target drive, then scan ID on each track. This command does not write to the disk, nor does it send any sector data to the Host. The effect of the Drive Diagnostic command is to verify that at least one sector header can be read on each track. It does not report an error when it encounters a track that has been formatted as a "Bad Track," "Bad-Track-With-Alternate," or "Alternate Track."

4.3.18 CONTROLLER DIAGNOSTIC (CLASS 7, OPCODE 04)

This command initiates the WD1002-SHD self-test diagnostic routine. The WD1002-SHD tests its Control Processor, Sector Buffer, ECC circuitry, Winchester Controller/Formatter, and the checksum of the Program Memory. The WD1002-SHD does not access the drive during this command. The following shows the Controller Diagnostic Command Block format.

	BITS							
BYTES	7	6	5	4	3	2	1	0
0	Command Class 7			Operational Code 04				
1	X	X	X	X	X	X	X	X
2	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X
4	X	X	X	X	X	X	X	X
5	X	X	X	X	X	X	X	X

Possible Error Codes

No error, ROM failure, RAM failure, or ECC hardware failure.

Action

Calculate a checksum for the program ROM, test the Control Processor, test the Sector Buffer, and test the ECC hardware. This command does not access any disk drive.

4.3.19 READ LONG (CLASS 7, OPCODE 05)

This command transfers the target sector and four bytes of data ECC to the Host. If an ECC error occurs during Read, the WD1002-SHD does not attempt to correct the data field. This command is useful in recovering data from a sector that contains an uncorrectible ECC error. It is also useful during diagnostic operations.

The following shows the Read Long Command Block format.

	BITS							
BYTES	7	6	5	4	3	2	1	0
0	Command Class 7			Operational Code 05				
1	LUN			Log Sec Address Bits 16-21				
2	Logical Sector Address Bits 8-15							
3	Logical Sector Address Bits 0-7							
4	Sector Count							
5	R	0	0	0	Fast Step Option			

R Retry Disable: 0 = No Disable
1 = Disable

Possible Error Codes

No error, invalid command, invalid sector address, drive not ready, seek error, bad track, illegal (direct) access to an alternate track, alternate track not marked as an alternate, address mark not found, or write fault.

Action

Read the specified number of consecutive sectors and their ECC bytes beginning with the specified sector contained in the Control Byte. There are four ECC bytes per sector. This command is only useful for diagnostic purposes.

4.3.20 WRITE LONG (CLASS 7, OPCODE 06)

This command transfers a sector of data and four appended ECC bytes to the disk drive. During this write operation, the Host supplies the four ECC bytes instead of the usual hardware-generated ECC bytes. This command is useful only for diagnostic routines.

The following shows the Write Long Command Block format.

	BITS							
BYTES	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Command Class 7			Operational Code 06				
1	LUN			Log Sec Address Bits 16-21				
2	Logical Sector Address Bits 8-15							
3	Logical Sector Address Bits 0-7							
4	Sector Count							
5	R	0	0	0	Fast Step Option			

R Retry Disable: 0 = No Disable
1 = Disable

Possible Error Codes

No error, invalid command, invalid sector address, drive not ready, seek error, bad track, illegal (direct) access to an alternate track, alternate track not marked as alternate, address mark not found, or write fault.

Action

Write the specified number of consecutive sectors beginning with the specified sector. Following each sector, the Host sends four ECC bytes to the WD1002-SHD to be written to the disk as the ECC bytes for the sector. This command is useful for diagnostic purposes. It allows the generation of a sector containing a correctable ECC error.

SECTION V
TIMING

5.1 GENERAL

This section contains the primary timing parameters associated with the Controller-Host interface. The three main areas of discussion are: Controller-Host acquisition (handshake); Data transfer from Host to Controller; Data transfer from Controller to Host. Also included is a discussion of key miscellaneous timing characteristics unique to the WD1002-SHD Controller. Figure 5-1 illustrates a typical Host-Controller bus transfer, complete with Controller selection.

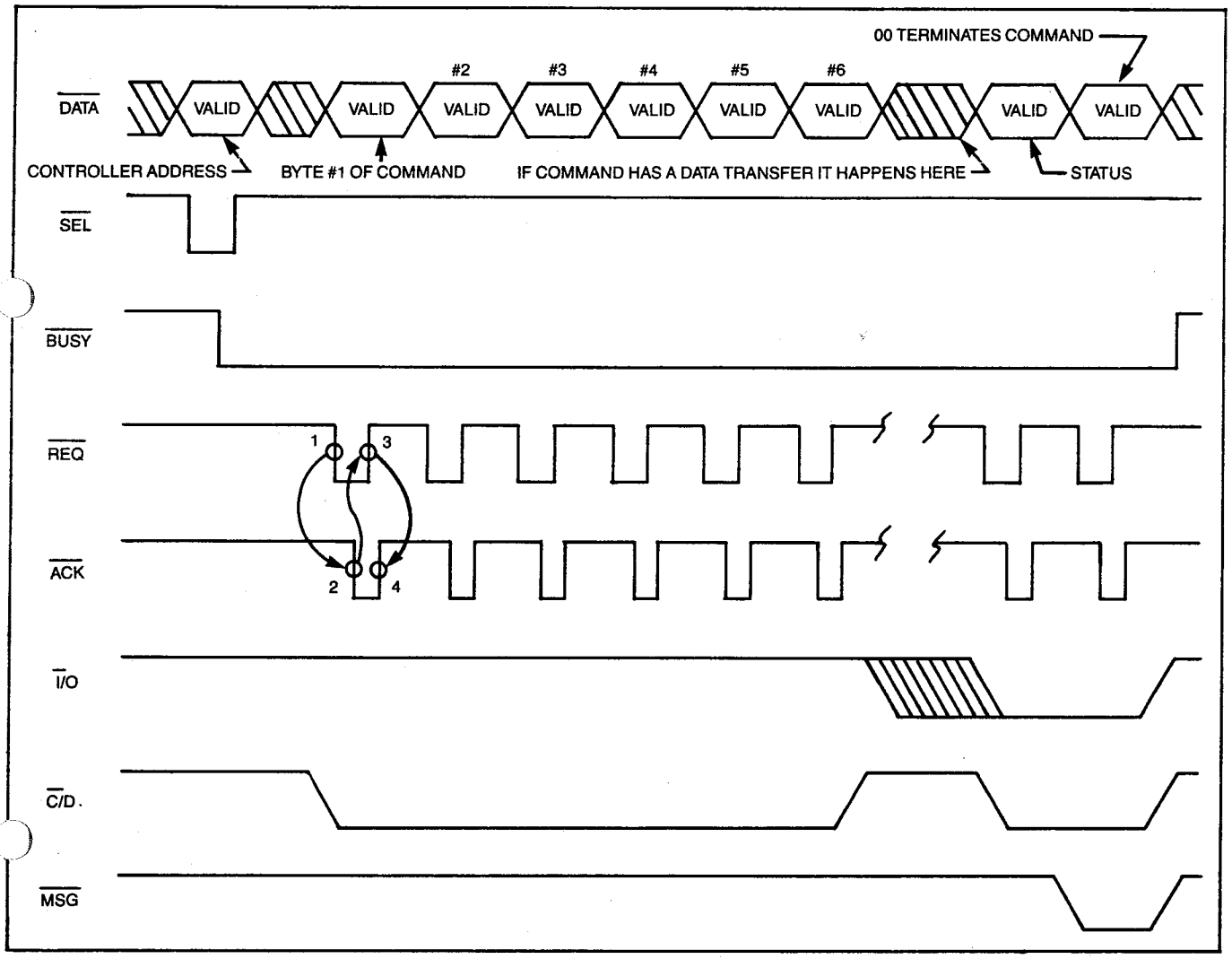
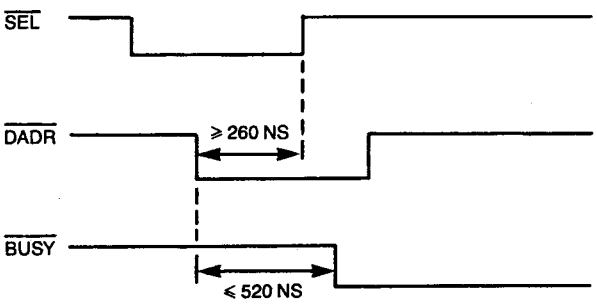


FIGURE 5-1. TYPICAL HOST-CONTROLLER BUS TRANSFER TIMING

5.2 HOST-CONTROLLER SELECTION TIMING

Prior to either command or data transfer, the Host must perform a handshake operation in selecting the Controller. The Host first asserts SEL and places the Controller address bit on the bus (the address bit is preset to DB0 at the factory but can be any bit from DB0 to DB7 in a multiple-Controller environment).

After the Controller recognizes its address bit and SEL being asserted, it then asserts BUSY. During this selection phase, the Host takes full control of the data bus by asserting O (I/O). Once the Controller has asserted BUSY, the selection process is complete. SEL must be de-asserted by the Host at or before the first Command byte to the Controller. Figure 5-2 illustrates the Controller Select timing. Figure 5-3 illustrates the Controller Select Timing Flow.



NOTE:

No restriction on sequence of $\overline{SEL}$ and $\overline{DADR}$ falling edges. Both must be low to ensure controller selection.

FIGURE 5-2. CONTROLLER SELECT TIMING

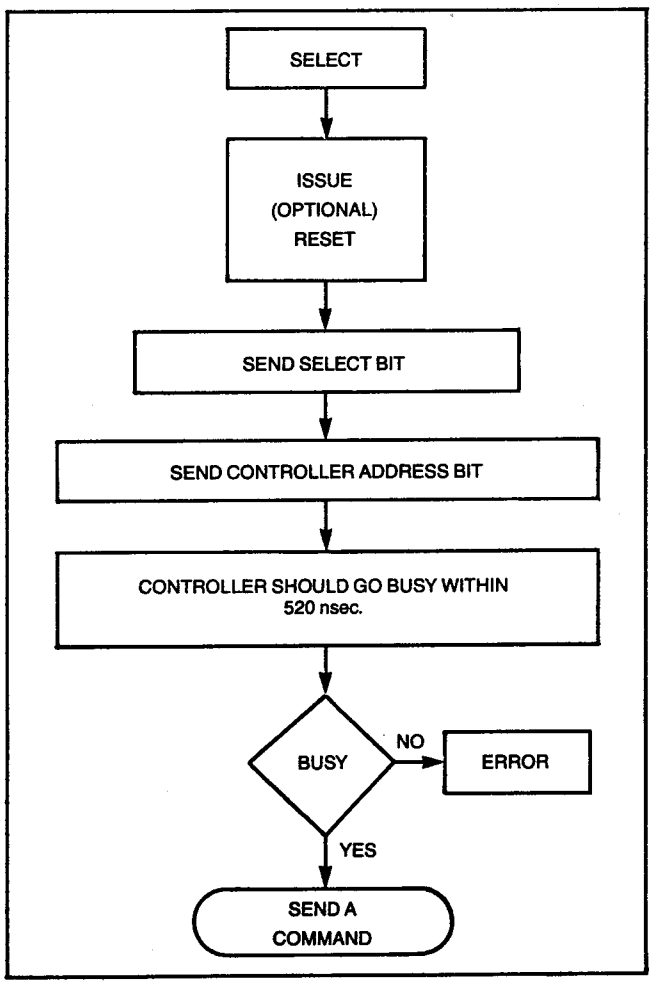


FIGURE 5-3. CONTROLLER SELECT FLOW DIAGRAM

5.3 COMMAND MODE

After Controller selection, the Host can transmit its first command. The Controller receives a command from the Host using a sequence of Handshake recognition signals. The Controller asserts $\overline{C}$ ($\overline{C}$/D) to notify the Host that it is ready to receive a command and asserts O ($\overline{I}$/O) to indicate that the direction is from the Host to the Controller. At this time, $\overline{MSG}$ is in the de-asserted state.

The Controller asserts $\overline{REQ}$ within 10 usec. After asserting O ($\overline{I}$/O), $\overline{C}$ ($\overline{C}$/D), and $\overline{MSG}$ is in the de-asserted state. The Host then answers by asserting $\overline{ACK}$ when it is ready to send a command byte to the Controller. The command byte must be stable on the bus within 250 nsec. of $\overline{ACK}$ being asserted and remain stable until the Controller de-asserts $\overline{REQ}$. After the Controller de-asserts $\overline{REQ}$, the Host de-asserts $\overline{ACK}$ completing the Handshake sequence for the first command byte. The complete handshake sequence must be repeated for each successive command byte from the Host. Table 5-1 lists the relationships of $\overline{I}$/O, $\overline{C}$/D, and $\overline{MSG}$.

TABLE 5-1. HOST BUS SIGNAL STATUS

$\overline{I}$/O	$\overline{C}$/D	$\overline{MSG}$	BUS STATUS
1	0	1	The Controller receives a command from the Host.
1	1	1	The Controller receives data from the Host.
0	1	1	The Controller sends data to the Host.
0	0	1	The Controller sends an Error Status byte to the Host.
0	0	0	The Controller informs the Host that it has completed the command in process.

5.3.1 DATA TRANSFER

Figures 5-4 and 5-5 illustrate the required timing for Host-to-Controller and Controller-to-Host data transfers respectively. These diagrams include the required handshake signals. Tables 5-2 and 5-3 provide the timing parameters for these diagrams.

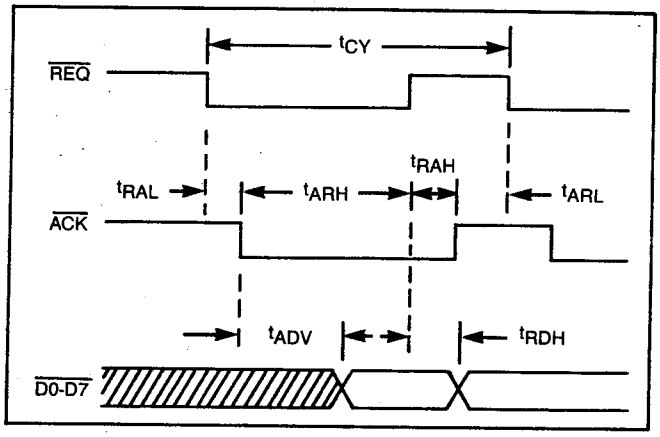


FIGURE 5-4.
HOST-TO-CONTROLLER DATA TRANSFER TIMING

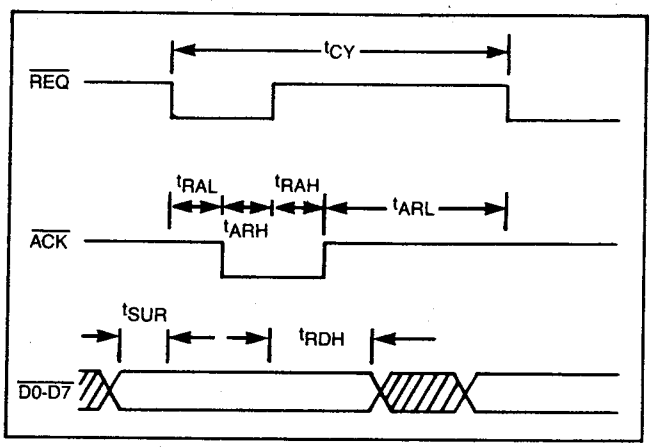


FIGURE 5-5.
CONTROLLER-TO-HOST DATA TRANSFER TIMING

TABLE 5-2.
HOST-TO-CONTROLLER TIMING PARAMETERS

PARAMETER	MIN*	MAX*
t_{CY}**	1152	
t_{RAL}†	0	
t_{ARH}	600	840
t_{RAH}††	0	
t_{ARL}	200	448
t_{ADV}		375
t_{RDH}	0	

*nsec
**If conditions in † and †† are met, then t_{CY}TYP = 1200 nsec and t_{CY} max = 1248 nsec.
†If $t_{RAL} \leq$ 89 nsec, then no wait states are inserted.
††If $t_{RAH} \leq$ 97 nsec, then no wait states are inserted.

TABLE 5-3.
CONTROLLER-TO-HOST TIMING PARAMETERS

PARAMETER	MIN*	MAX*
t_{CY}**	1152	
t_{RAL}†	0	
t_{ARH}	200	448
t_{RAH}††	0	
t_{ARL}	200	848
t_{SUR}	125	
t_{RDH}	152	

*nsec
**If conditions in † and †† are met, then t_{CY}TYP = 120 nsec and t_{CY} max = 1248 nsec.
†If $t_{RAL} \leq$ 497 nsec, then no wait states are inserted.
††If $t_{RAH} \leq$ 200 nsec, then no wait states are inserted.

5.3.2 STATUS BYTES

After every command, the Controller sends two status bytes to the Host. The first byte of information contains the error status code for that command and the second byte contains all zeroes, indicating that the command has been completed. The formats for these status bytes are provided in Section IV. Figure 5-6 illustrates the timing sequence for Command Termination. Figure 5-7 illustrates the timing flow for sending and terminating a command, and Figure 5-8 illustrates Status Request Timing Flow.

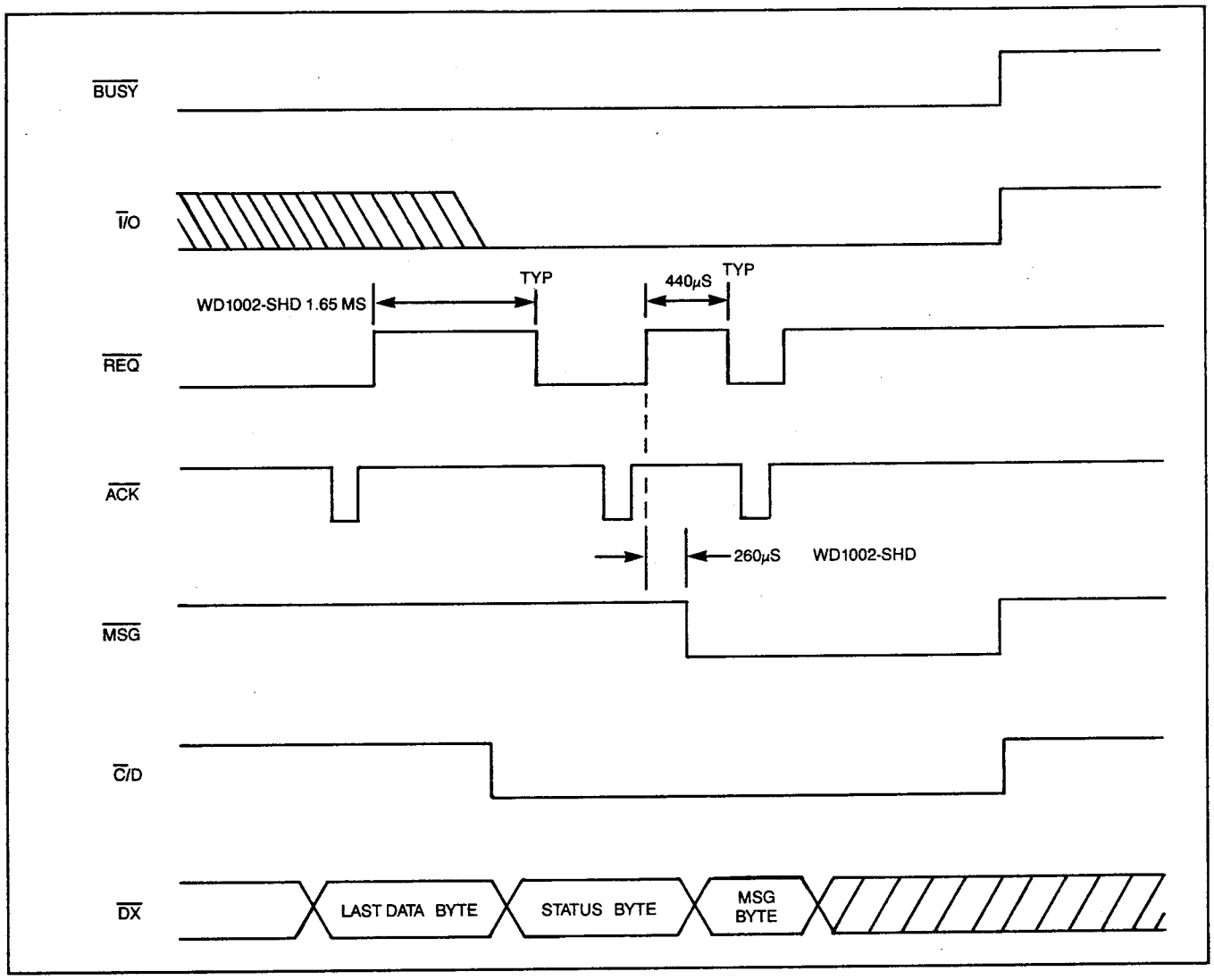


FIGURE 5-6.
COMMAND TERMINATION TIMING

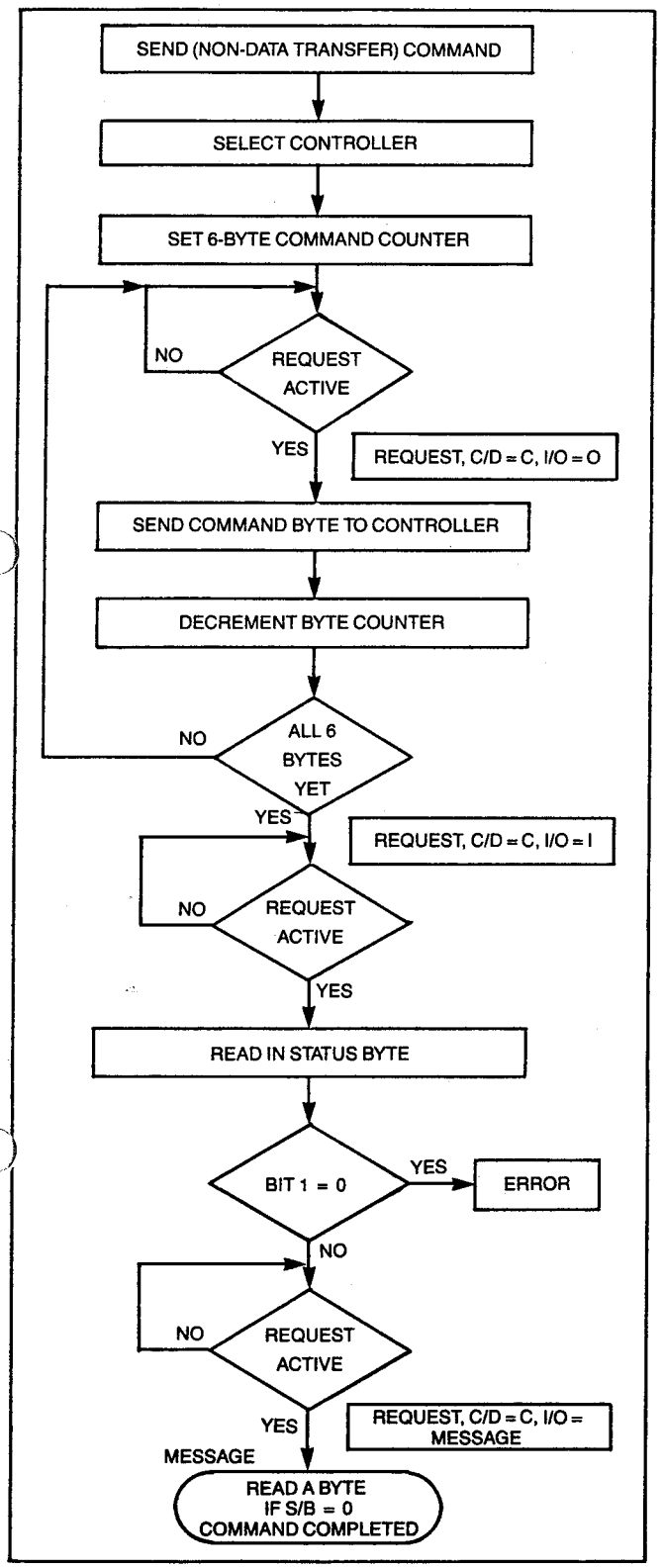


FIGURE 5-7.
COMMAND SEQUENCE TIMING FLOW DIAGRAM

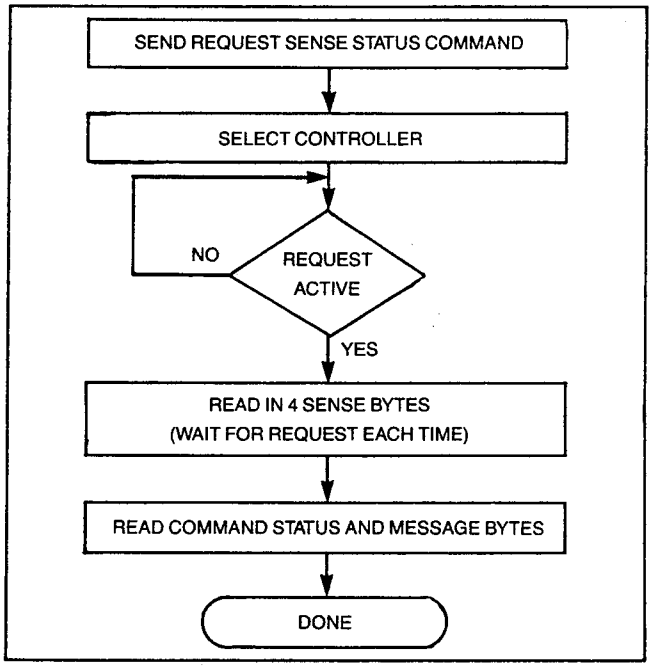


FIGURE 5-8.
REQUEST STATUS COMMAND
TIMING FLOW DIAGRAM

5.4 MISCELLANEOUS TIMING

The following is a list of specific timing parameters that must be met for proper operation of the WD1002-SHD:

A. **CONTROLLER RESET** — Power-On-Reset (POR) is less than 120 msec. and Reset ($\overline{RST}$) is less than 120 usec. During either of these periods, the Host is inhibited from selecting the Controller. If selection is attempted, the Controller does not assert BUSY.

B. **SELECT TO $\overline{C}$/D** — After $\overline{RST}$ or POR, the Controller runs its internal diagnostic routines until it is selected by the Host, at which point the Controller exits the diagnostic routine being run. While in the diagnostic loop, THE CONTROLLER CAN TAKE AS LONG AS 340 msec. AFTER IT ASSERTS $\overline{BUSY}$, BEFORE ASSERTING $\overline{C}$ ($\overline{C}$/D). However, once the Controller has left the diagnostic loop, no more than 80 usec. is required for the Controller to assert $\overline{C}$ ($\overline{C}$/D) after $\overline{BUSY}$ is asserted.

C. **$\overline{C}$/D TO FIRST $\overline{REQ}$ TIMING PULSE** — When the Controller first asserts $\overline{C}$ ($\overline{C}$/D) until the first $\overline{REQ}$ pulse is asserted is typically 120 usec.

D. **WAIT STATE** — One wait state equals 200 nsec.

NOTE:
All SASI protocol must be adhered to (i.e. a $\overline{REQ}$/$\overline{ACK}$ handshake must precede every byte transferred).

SECTION VI
FUNCTIONAL THEORY OF OPERATION

6.1 GENERAL

The WD1002-SHD SASI Winchester Controller Board performs all functions necessary to control Seagate Technology ST506 Winchester disk drives, or their compatible equivalents, via a SASI bus interface. The WD1002-SHD (illustrated in Figure 6-1) is comprised of six functional groups:

1. Host Interface
2. Control Processor
3. Sector Buffer
4. Winchester Control
5. Data Separator
6. Error Checking and Correction (ECC)

6.2 HOST INTERFACE

The Host Interface manages all incoming and outgoing bus traffic between the Host and the WD1002-SHD. Communications, consisting of control signals and an 8-bit, bi-directional bus to and from the Host, are made via computer access ports. All data, status information, and command parameters are transferred via these access ports.

The State Sequencer provides the necessary address decoding and control logic to synchronize the Host Interface and the Sector Buffer with the SASI bus operation.

The SASI bus operation is partitioned into the following mutually exclusive time phases:

A. Reset Phase
B. Bus Free Phase
C. Target Selection Phase — Transactional
D. Information Transfer Phase — Phases
E. Bus Release Phase

6.2.1 BUS PHASE SEQUENCING

A Reset Phase may occur at any time. It is followed by the Bus Free Phase. In the absence of a Reset Phase, the bus alternates between the Bus Free Phase and the transactional portion of the bus phases which are always completed in the following sequence:

1. One Target Selection Phase
2. One or more Information Transfer Phases
3. One Bus Release Phase

These bus phases constitute the SASI Bus protocol recognized by the WD1002-SHD. The relationship and definitions of these phases are described in the following text. The Information Transfer Phase is sub-divided into its mutually exclusive categories. These categories are also polled.

RESET PHASE is defined as the time that $\overline{\text{RESET}}$ is asserted. It is used by the Host to force all devices on the bus to the same state as that following power-on initialization (Power-on Reset is 110 msec. while $\overline{\text{RST}}$ from the Host is only 100 usec.).

BUS FREE PHASE is defined as the time period between completion of one transaction (Bus Release Phase) and initiation of a new transaction (Target Selection Phase). It can also be considered that time during which no device has control of the bus, all eight control lines are de-asserted, and all Data lines are in an undefined state.

TARGET SELECTION PHASE is defined as that time period commencing when the Host places a Target Address on the SASI bus. The Host then asserts $\overline{\text{SEL}}$. The Target Selection Phase terminates when the Target addressed recognizes its selection and responds by asserting $\overline{\text{BUSY}}$ (the Host must de-assert $\overline{\text{SEL}}$ before completion of the current transaction or the end of the next Bus Release Phase).

TABLE 6-1. INFORMATION TRANSFER PHASE CONFIGURATIONS

CONTROL BITS			TRANSFER TYPE	# OF BYTES
$\overline{\text{I/O}}$	$\overline{\text{C/D}}$	$\overline{\text{MSG}}$		
1	0	1	Command Block From Host	6
1	1	1	Data Block From Host	3,8,256,260,512, or 516
0	1	1	Data Block To Host	1,4,256,260,512, or 516
0	0	1	Status Byte To Host	1
0	0	0	Message Byte To Host	1

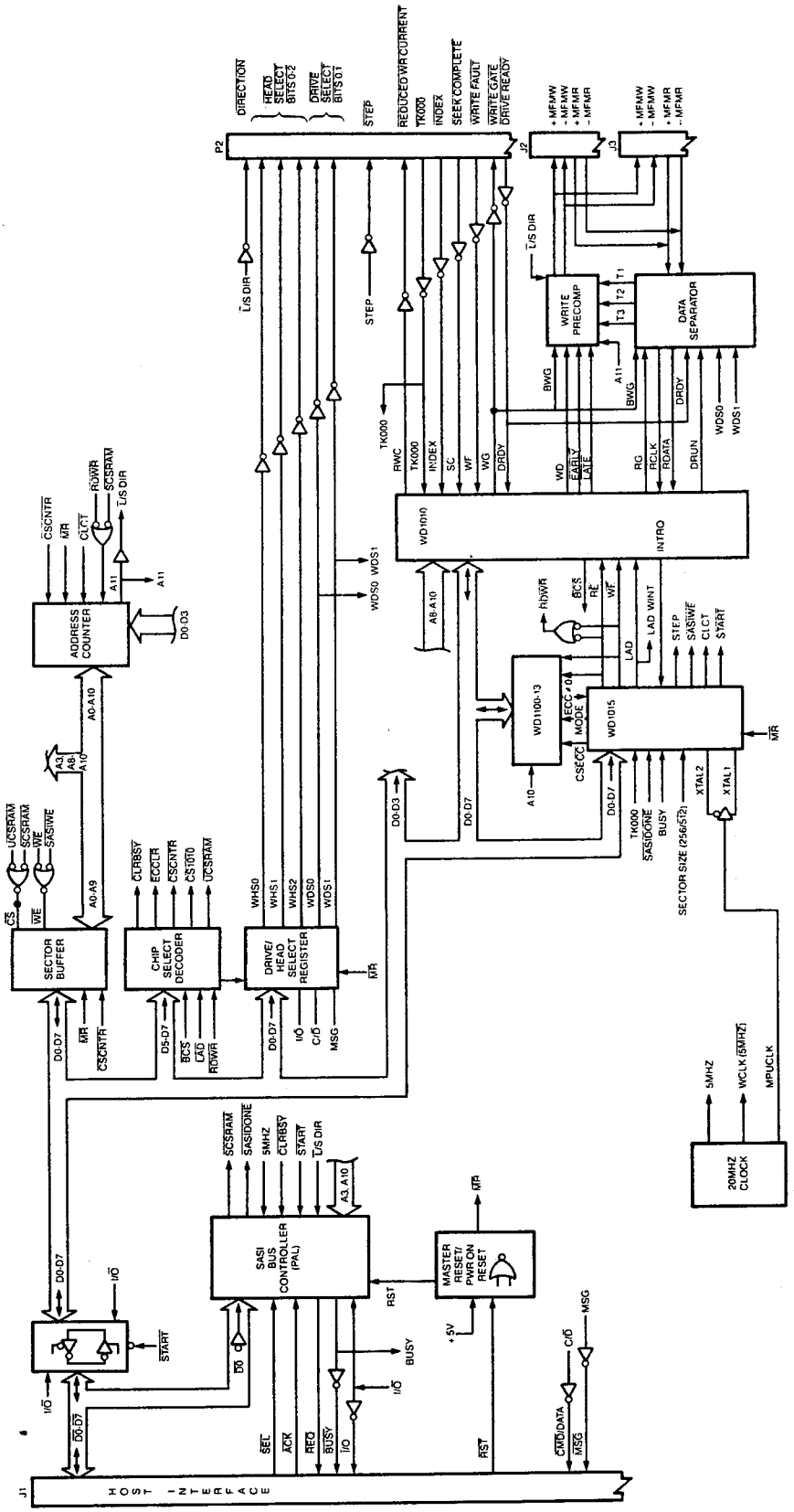


FIGURE 6-1. WD1002-SHD FUNCTIONAL BLOCK DIAGRAM

INFORMATION TRANSFER PHASE is used to transfer one or more bytes over the bus from Host-to-Controller or Controller-to-Host. The phase begins when the currently selected controller sets I/O, C/D, and MSG to one of the five legal combinations listed in Table 6-1. This signals the Host as to which type of byte transfer(s) will follow. For each byte transferred, the following events must occur in sequence in order to perform the asynchronous handshake required by the SASI bus: The WD1002-SHD asserts REQ; The Host asserts ACK; The WD1002-SHD de-asserts REQ; The Host de-asserts ACK.

For Controller-to-Host transfers, the byte being transferred must be valid on the bus at least 100 nsec. before REQ is asserted. For Host-to-Controller transfers, the byte being transferred must be valid on the bus no later than 250 nsec. after ACK is asserted (it is helpful to know that the byte being transferred is valid on the bus at the trailing edge of REQ during any transfer).

The Command Block Transfer is used to send a block of parameters to the Controller that defines the operation to be performed. The Data Block Transfer is used to send one or more sectors of data (with or without ECC) in either direction, as well as an extra block of parameters to the Controller or bytes of Controller operational information to the Host. The Status Byte Transfer is used to send encoded error status bytes to the Host. The Message Byte Transfer is used to send a byte of all zeroes to the Host to satisfy SASI Bus Protocol.

BUS RELEASE PHASE is defined as the period during which the Controller has completed a transaction and no longer has control of the bus. The Host is notified of the Bus Release Phase with the trailing edge of BUSY.

6.2.2 TRANSACTION SEQUENCE

During a Transaction, all Data Block Transfers are in the same direction and of the same size. In more detail, a Transaction always consists of the following sequence of events:

1. One Target Selection Phase
2. One Command Block Transfer
3. Zero or more Data Block Transfers (type and number determined by the preceeding Command Block parameters)
4. One Status Byte Transfer
5. One Message Byte Transfer
6. One Bus Release Phase

6.3 CONTROL PROCESSOR

All operations on-board the WD1002-SHD are controlled by the 5MHz, WD1015-02 Control Processor. The Control Processor contains all necessary instructions within its ROM, as well as a 256 byte scratch pad, to manage all commands and communications with the Host, as well as control of all on-board traffic management. The Control Processor provides all buffer management for the WD1010 Winchester Controller/Formatter and the WD1100-13 ECC Support Device used on the WD1002-SHD.

The Control Processor decodes and executes all SASI commands received by the WD1002-SHD and controls all necessary on-board operations required. When an ECC error has been detected, the Control Processor performs the operation of error correction. If the error is uncorrectable, the Control Processor terminates the operation. During status reporting, the Control Processor encodes the normal completion status from the Controller/Formatter with the current ECC Support Device status into a form consistent with SASI protocol and sends it to the Host. If an error exists at the time, the Host is required to send a Request Status Command to the WD1002-SHD.

6.3.1 CONTROL PROCESSOR SELECTION

The WD1002-SHD is in the Bus Free Phase when it is waiting for selection. When the State Sequencer receives a select signal with the correct address select bit in parallel, it asserts controller BUSY. The Control Processor, monitoring this signal, is informed of its selection.

6.3.2 HOST/CONTROLLER RECOGNITION

Once selected, the Control Processor asserts BUSY and START. When START is detected, the State Sequencer asserts REQ and transmits it to the Host. If the data transfer is to the Host, the Control Processor provides data in parallel with REQ to the Host. Upon receipt of the data and REQ, the Host then asserts ACK, acknowledging receipt to the WD1002-SHD. If the data transfer is from the Host to the WD1002-SHD, when the Host recognizes REQ asserted, it will in turn assert ACK and transmit the data in parallel with ACK to the WD1002-SHD. This REQ/ACK handshake is required for every byte transferred on the SASI bus.

Along with the REQ/ACK handshake, the Control Processor asserts the proper control signals to determine direction of transfer (I/O) and type of transfer (C/D). The last byte of all transfers is always zeroes and is transferred in parallel with MSG asserted. This byte indicates to the Host that the command is compete.

6.4 SECTOR BUFFER

The on-board Sector Buffer (RAM) provides storage during data transfers between Host and drive in order to prevent data overruns. The Sector Buffer also buffers all other information transmitted across the SASI bus (i.e., sector data, status bytes, command bytes, and drive parameter characteristics).

6.4.1 SECTOR BUFFER ACCESS

In order to read from or write to the Sector Buffer, the Control Processor asserts SASIWE, indicating an SASI bus access, or WE is asserted by the Control Processor or the Controller/Formatter, indicating access with that device. Data is fed into the Sector Buffer with the trailing edge of CE. CE is generated when the Control Processor or the Controller/Formatter asserts UCSRAM, or the State Sequencer asserts SCSRAM. Both of these signals are enabled when BCS is asserted and A10 is de-asserted.

6.4.2 SECTOR BUFFER ADDRESSING

The Sector Buffer lower address counter is used to preset the count for 1, 3, 4, 6, or 8 byte transfers when a small magnitude of data is to be transferred (8 bytes or less). The counter is first cleared, then the Control Processor initiates the required dummy reads or writes to external memory. These, in turn, preset the address counter to the desired count. When the terminal count is reached after completion of the actual command, the address counter notifies the State Sequencer, which in turn asserts SASIDONE, signaling the Control Processor the desired number of bytes have been transferred. The Sector Buffer upper address counter is used to determine the sector size to be transferred (the counter can be preset for 128, 256, 512, or 1024 byte sector sizes) and when a sector has been read or written. It is also used to select the Controller/Formatter registers.

6.5 WINCHESTER INTERFACE AND CONTROL

The Winchester drive interface consists of the Winchester Controller/Formatter (WD1010), Data Separator, Write Precompensation logic, and appropriate drivers and receivers. The Winchester Controller/Formatter interfaces with the Winchester Drive(s) via 20 control and data lines that form the actual interface. The WD1002-SHD uses a multiplexed data/address bus to share Sector Buffer access with the Winchester Controller/Formatter, the Control Processor, the Host Interface, and ECC.

6.5.1 DATA SEPARATOR

The WD1002-SHD utilizes a discrete Data Separator designed to process incoming MFM data from the Winchester drive using data separation. In order to provide maximum data recording density and storage efficiency, data is recorded on the disk using Modified Frequency Modulation (MFM) technique. This technique requires clock bits to be recorded only when two successive data bits are zeroes in the data stream. This reduces the total number of bits (clock and data) required to record a given amount of information on the disk. This effectively doubles the amount of data capacity, hence the term double density.

Due to the fact that clock bits are not recorded with every data bit cell, circuitry is required that can remain in sync with the data stream during the absence of clock bits. Synchronous decoding of MFM data streams requires the decoder circuitry to synthesize clock bit timing when clock bits are not present, and synchronize the clock bits when they are present. This is accomplished using a phase locked oscillator employing an error amplifier/filter to sync onto, and hold a specific phase relationship to the data and clock bits in the data stream. The synthesized clock (RCLK) can then be used to separate data bits from clock bits and to shift the resultant serial data into registers for byte parallelization (done in the WD1010).

6.5.1.1 Reference Clock

The reference clock is derived from the Write Clock (WCLK) crystal oscillator. This oscillator uses a fundamental crystal that oscillates at four times the RCLK frequency. The 4X output is then divided by 2 to produce both a 2X clock (2X DR) which is used as a reference and a 1X clock (WCLK) which is used to produce MFM Write Data for the disk. The crystal frequency is 20,000 MHz for ST506 compatible drives.

6.5.1.2 Incoming Data Selection

Serial data is received from one or two radially connected Winchester drives, via an RS-422 differential receiver, by the WD1002-SHD. The receiver converts differential input data to TTL levels for use by the controller. The data from the selected drive is then routed to the data separator circuit via a one-shot. The one-shot provides a consistent data pulse width and is used due to the fact that different drives produce varying data pulse widths. At this point, data and clock bits are still combined and appear as 110 nsec. nominal active high pulses spaced at intervals of 1.0, 1.5, and 2 times the RCLK period. This data is presented to the Data Separator which will gate either MFM data or a reference clock into the first stage of the Voltage Controlled Oscillator (VCO) error amplifier circuitry.

6.5.1.3 Clock Gating

The gating of RCLK and MFM data into the Data Separator is dependent upon the status of Read Gate (RG) and the spacing of the data in the serial stream after RG is asserted. It is necessary to run the VCO at a rate 2X Data Clock (RCLK) due to the techniques employed to separate data from clocks. The VCO is set to an open loop frequency of 2XRCLK. Any variations in this rate due to differences in disk rotational speed must be compensated for by the VCO. However, instantaneous shifts in data due to the effect of adjacent bit cells on the disk and minor noise must be ignored. The response of the VCO must also be adjusted to effectively ride over missing clock bits which occur as a result of the MFM recording technique. The resultant compromise between response and reject requirements of the VCO causes the VCO to have a tendency to become locked onto harmonics of the data rate easily. This is likely to occur if the VCO is connected to a data stream over a field of data which has data bits spaced at 1.5 or 2.0 times RCLK intervals.

To provide protection against this undesirable condition, the VCO is connected to a harmonic clamp providing a 2X RCLK frequency lock wherever the WD1002-SHD is not actually reading data. Care is taken to switch in Read Data to the VCO error detector only when it is known that the data stream frequency is equal to the RCLK frequency. This can occur only when the data stream is a solid stream of all zeroes or all ones.

6.5.1.4 High Frequency Detection

When 16 consecutive ones or zeroes (high frequency) are detected on the raw MFM data stream, the DRUN one-shot remains triggered. The one-shot is set for a pulse width of 1.25X RCLK period (270 nsec. for ST506 compatible drives).

Each clock or data bit on the serial stream triggers the one-shot. If the time between successive triggers is less than the one-shot time constraint, the one-shot remains triggered. If any data bit fails to reach the one-shot before the end of its time constraint, the one-shot is reset.

6.5.1.5 Sample On Phase Detection

When an input signal is received by the WD1002-SHD, phase relationship is detected by the Data Separator. The function of this phase detector is to provide windows, during which the leading edge of the incoming MFM data can be compared to the leading edges of the VCO clock. The windows are approximately 50 nsec. in length. The windows are initiated by the leading edge of any data bit entering the frequency detector. They are terminated by the same data bit edge, delayed by 60 nsec. or the VCO output (OSC). When both the delayed data bit and the nearest VCO leading edge arrive at the detector, the detector is reset until the next data bit arrives on the MFM data stream. The delayed data bit sets its half of the frequency detector latches to produce a pump-up condition at the error amplifier. The VCO clock edge sets its half of the Frequency detector latches to produce a pump-down condition. When the circuit is balanced, both pumps are either on or off, producing no net pump-up or pump-down pulses to the error amplifier.

6.5.1.6 Error Amplifier/Filter

Control of the VCO is accomplished by the Error Amplifier/Filter. The Error Amplifier is a balanced current mirror, whose output sources or sinks current to the filter stage. Whenever the VCO is running slow, the Error Amplifier receives pulses from the data bits before pulses from the VCO clock. This causes the Error Amplifier to produce pump-up pulses to the filter. The filter integrates these pulses, producing an average increase in the voltage to the VCO. The filter output voltage is buffered by a unity gain op amp prior to being sent to the VCO. Whenever the VCO is running too fast, the Error Amplifier produces pump-down pulses to the filter, which in turn lowers the voltage to the VCO.

6.5.1.7 VCO

The WD1002-SHD uses a single chip VCO which simplifies circuitry and adjustments. The operating frequency of the VCO is initially set by adjusting the variable capacitor for a 10 MHz output center frequency (when using 5 MHz drives) and a frequency control voltage of 2.5 $\pm$ 0.5 VDC.

The output of the Error Amplifier/Filter to the VCO represents how much deviation there is between the VCO frequency and that of the incoming data signal. The error signal, which is proportional to this difference, allows the VCO frequency to shift from center frequency to the frequency of the incoming signal. When the loop is in lock, the frequency difference component (error voltage) is DC and will be passed by the low pass filter. Thus the lock range is limited by the range of the error voltage that can be generated. The lock range is essentially a DC parameter and is not affected by the band edge of the low pass filter. It can be defined as the frequency range, usually centered about the VCO initial free running frequency, over which the loop can track the input signal once lock has been accomplished.

Frequency control is usually a matter of frequency range. The difference component may fall outside the band edge of the low pass filter and be removed along with the sum frequency component. If this is the case, no information is transmitted around the loop and the VCO remains at the initial free running frequency. As the input frequency approaches that of the VCO, the frequency of the difference component decreases and approaches the band edge of the low pass filter. Now, some of the difference component is passed, which tends to drive the VCO towards the frequency of the input signal. This, in turn, decreases the frequency of the difference component and allows more information to be transmitted through the low pass filter to the VCO. This is essentially a positive feedback, which causes the VCO to lock with the input signal. With this in mind, the term capture range can be defined as the frequency range centered about the VCO initial free running frequency over which the loop can acquire lock with the input signal. By setting the center frequency equal to two times the data rate, the VCO lock to the data and gives an exact synchronized clock.

6.5.1.8 Window Extension

Once the VCO has locked onto the phase of the incoming data, the actual separation of data and clocks occurs using a technique called window extension. This technique causes data bits to have their leading edges first shifted into the center of the RCLK half cycles, and then latched or extended until the next rising edge of RCLK. The VCO clocks a pair of latches.

If an MFM data bit enters the latches while RCLK is low, it is be extended as a data bit. If RCLK is high, it is extended as a clock bit. Due to this extension technique, bits can jitter up to one fourth of RCLK period without being lost.

6.5.1.9 Address Mark Detection

It is impossible to know whether serial data bits are actually data or clock bits just by looking at the data stream. It is also equally impossible to determine byte boundries within the data stream. This problem is solved by a uniquely recorded data/clock pattern called an Address Mark. The Address Mark consists of a data pattern of hexadecimal A1 with a missing clock pattern of hexadecimal OA. Normally a data byte of A1 hex requires a clocking pattern of OE hex.

The Address Mark is used to uniquely identify the start of a field of information (data or ID field) within each sector. Preceeding each Address Mark on the disk, there is always a long stream of zeroes. Zeroes have a clock bit for every RCLK. When attempting to read information from the disk, the WD1002-SHD first requires phase lock over a field of zeroes. After phase lock acquisition is achieved, the WD1002-SHD then detects the Address Mark.

6.5.2 WRITE PRECOMPENSATION

The generation of MFM Write Data takes place in the Winchester Controller/Formatter (WD1010). The WD1010 accepts a byte of data and a Write Clock (WCLK) to produce MFM data through internal circuitry that detects when and where to write clock pulses in the serial data stream based on the MFM encoding technique described earlier. The MFM data is now totally compatible with the required format for transmission to the disk via drivers with one exception; due to the decreasing radius on the physical surface of the disk, the inside tracks have less circumference and therefore exhibit an increased recording flux density over the outside tracks. This increase in flux density aggravates a problem known as "dynamic bit shift."

Dynamic bit shift comes about as a result of one bit on the disk (a flux reversal) influencing an adjacent bit. The result is to shift the leading edge of both bits closer together or further apart depending on the relative polarity. The net result is that enough jitter is added to the data recorded on the inside tracks to make them harder to recover without error.

Write Precompensation is used to reduce the effect of dynamic bit shift on the recorded data. It is a method of predicting which direction a particular bit will be shifted and intentionally writing that bit out of position in the opposite direction from the expected shift. This is performed by examining two data bits: the last one written and the present one to be written to the disk. A comparison of these bits produces one of three signals: $\overline{\text{EARLY}}$, NOMINAL, or $\overline{\text{LATE}}$. These signals are used in conjunction with a delay line to cause the leading edge of the data or clock bit to be written $\overline{\text{EARLY}}$, $\overline{\text{LATE}}$, or on time (NOMINAL).

The State Sequencer can enable or disable the generation of these Write Precomp signals by controlling the L/S DIR signal. When the signal is high, Write Precomp is enabled, Conversely, when the signal is low, Write Precomp is disabled, and the NOMINAL output is held true.

The delay performs the Write Precomp with the use of an AND/OR/INVERT gate. MFM Write pulses are applied to the input of the delay line and, depending upon which of the three Write Precomp signals is present, the AND/OR/INVERT gate selects the appropriate tap on the delay line. EARLY data is tapped from the first tap, NOMINAL from the second, and LATE from the third. From here, The MFM data is sent to the RS-422 driver where it is converted to a differential form and then transmitted to the disk drive.

6.6 ERROR DETECTION AND CORRECTION (ECC)

6.6.1 ECC GENERATION

The ECC Support Device (WD1100-13) is used to both generate and check the ECC bits appended to the data stream written to the disk. The ECC Support Device functions the same during both write (ECC generation) and Read (ECC checking) operations except that the Control Processor asserts WE at the end of the data field, enabling the ECC Support Device to append the computed ECC bytes to the data field, as opposed to producing a syndrome (RE).

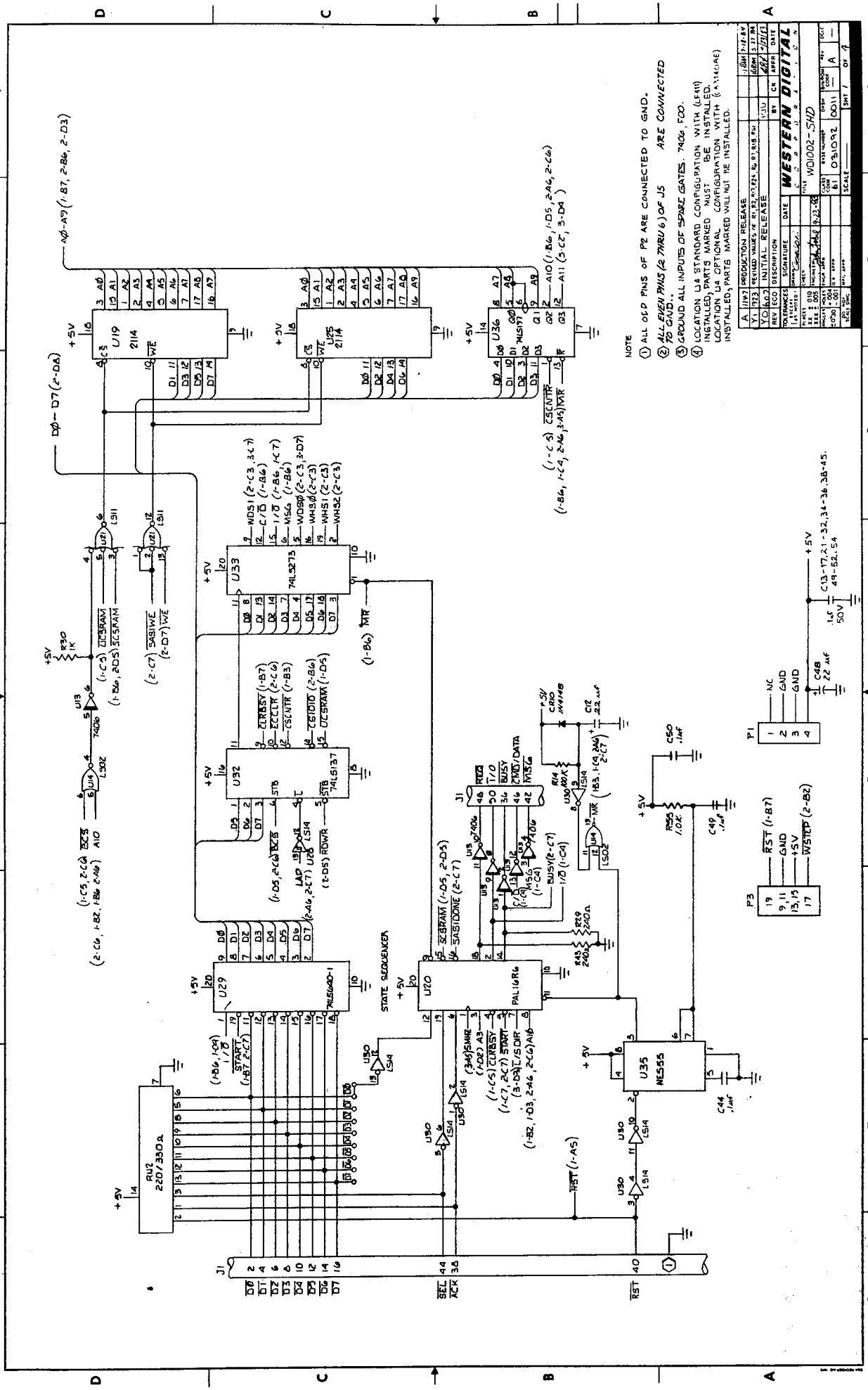
6.6.2 ECC

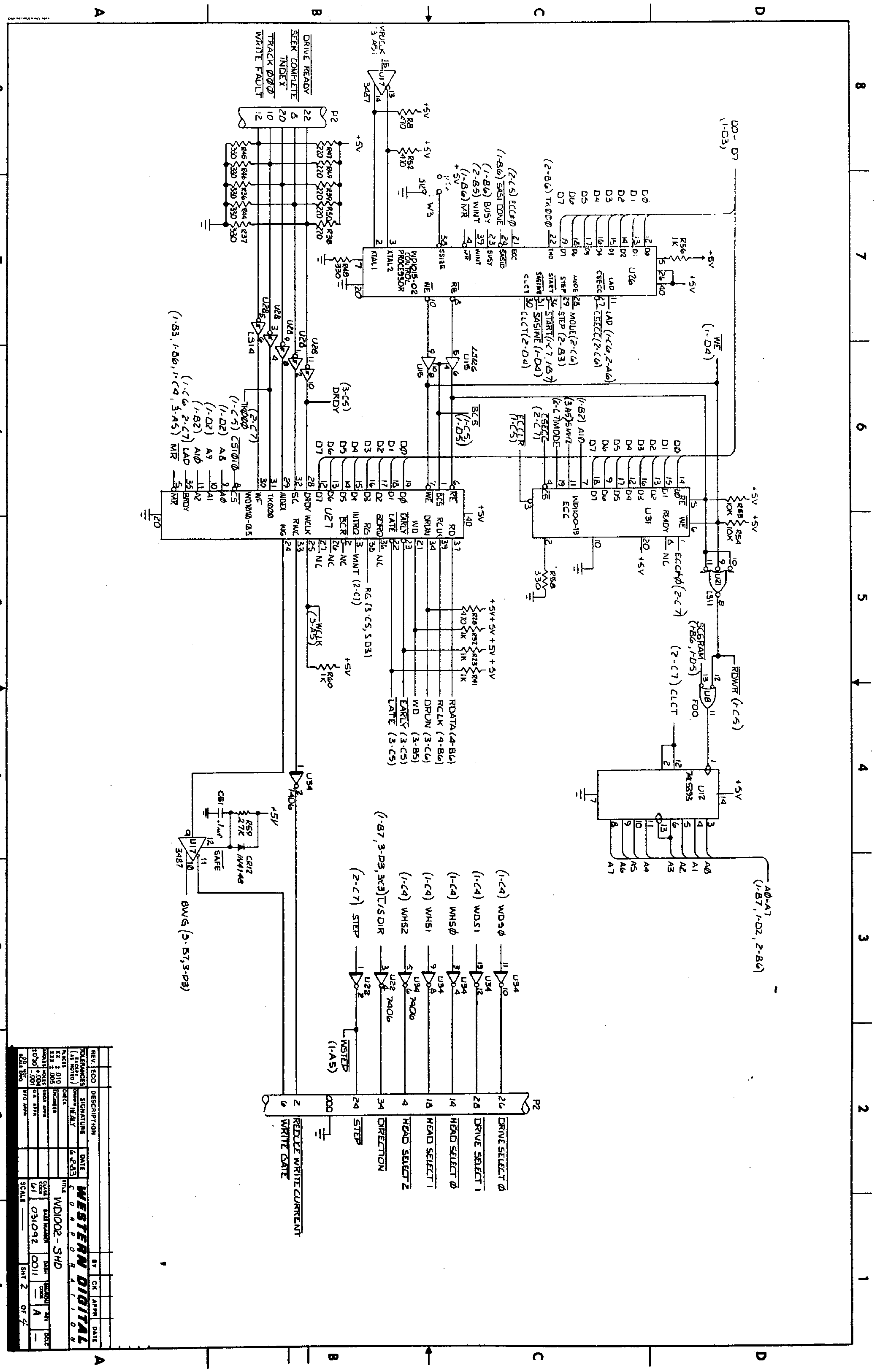
Data recorded on Winchester disk media is prone to several types of errors which could corrupt data integrity if some form of data correction were not available. Error Detection is performed on the WD1002-SHD for all data transfers from the disk. The data fields have a special 32-bit Error Correction Code (ECC) appended to them when they are first written to the disk. The ECC Support Device that generated these ECC bytes is the same device used by the WD1002-SHD to check the ECC code during a Read operation (enabled when the Control Processor asserts RE). The following is the ECC polynomial used by the WD1002-SHD:

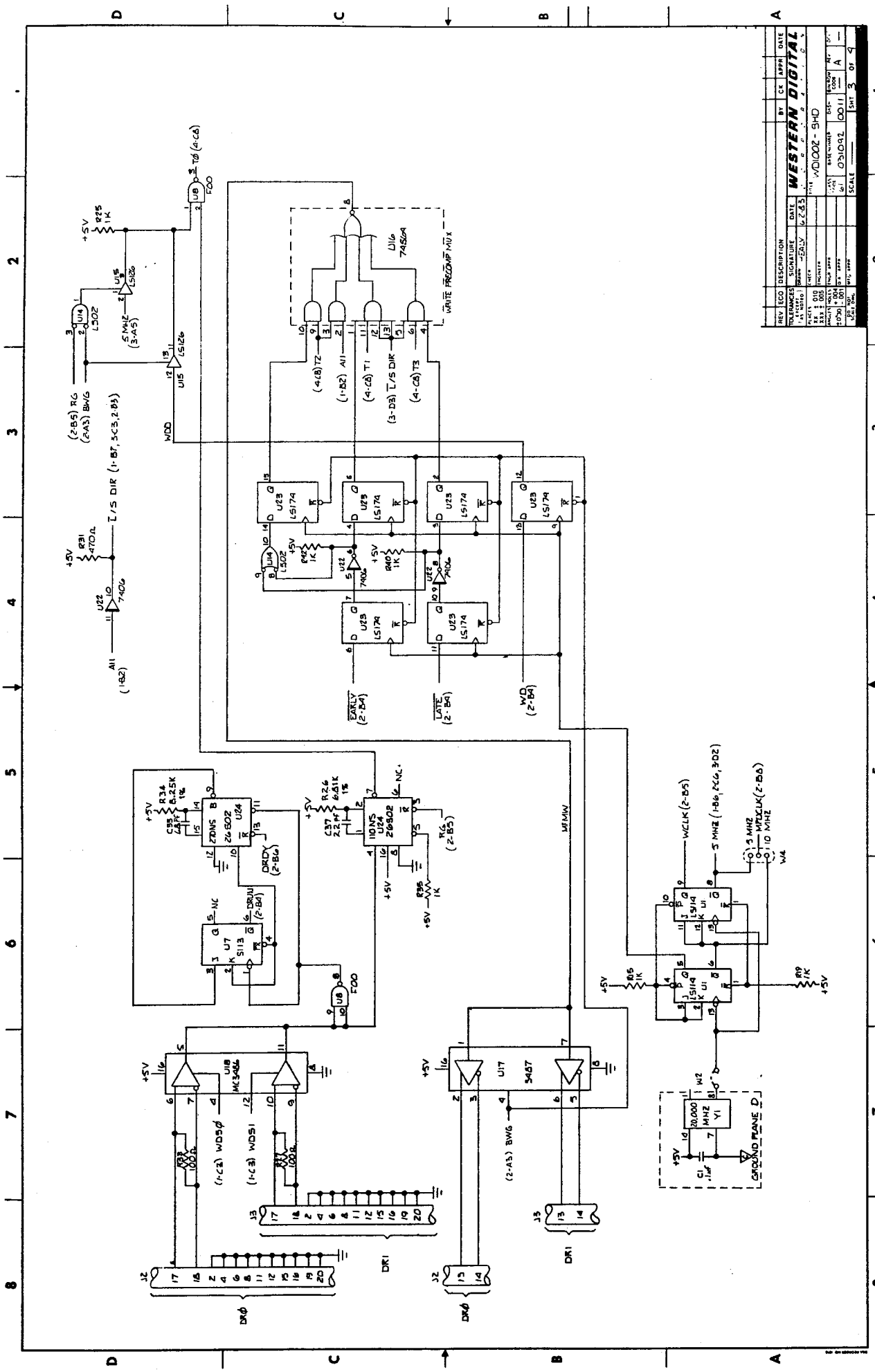
$$ECC = X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^{6} + X^{2} + 1$$

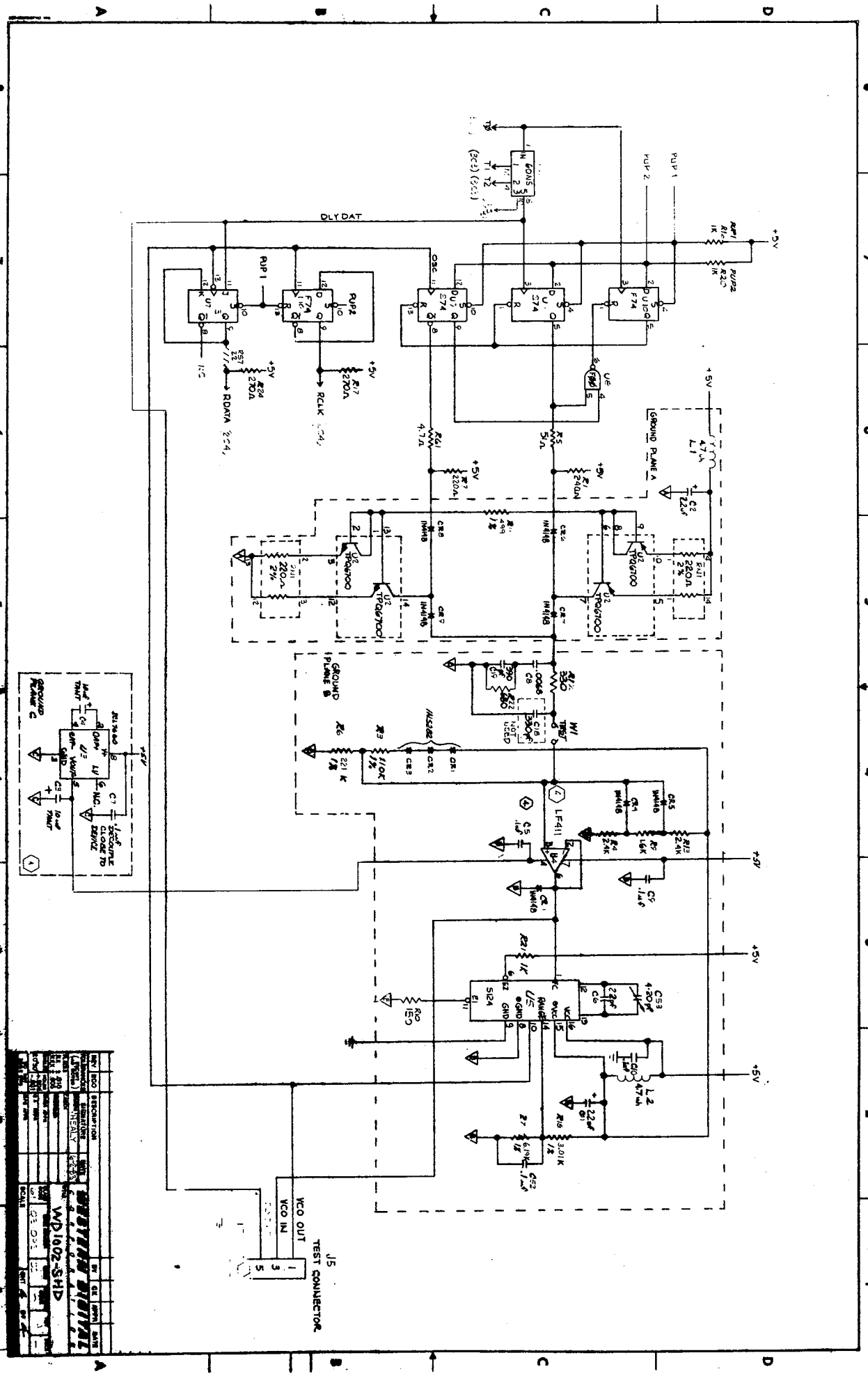
As data is being read from the disk, the ECC Support Device re-generates the original ECC code and exclusively ORs it with the ECC characters read from the disk at the end of the data field. The resultant syndrome (comparison) should be all zeroes if there are no errors in the data field. If, however, the syndrome contains a result other than zero, the ECC Support Device rereads the data field and looks for two consecutive syndromes that compare. If the device continues to read error syndromes that don't compare with each other, it raises an uncorrectable error flag. If it reads two consecutive error syndromes that compare, it raises a correctable error flag and the Control Processor then uses the error syndrome to attempt error correction, if ECC is enabled (Byte 5, bit 6 of the Command Block). If, after the first error syndrome, all retries are normal, no error is indicated.

The error syndrome is used by the Control Processor to compute the displacement and error vector within the sector. This information is then used to correct the corrupted burst of information in the data field. Multiple bursts of corrupt data can be detected, however, no more than a single burst detected (up to 5 bits in length) can have correction attempted.


WESTERN DIGITAL
WD1002-SHD
NOTE
1. ALL O.D. PINS OF P2 ARE CONNECTED TO GND.
2. ALL EVEN PINS (2 THRU 6) OF J5 ARE CONNECTED TO GND..
3. GROUND ALL INPUTS OF SPARE GATES. 7406, F00.
4. LOCATION U4 STANDARD CONFIGURATION WITH (LF41) INSTALLED, PARTS MARKED MUST BE INSTALLED. LOCATION U4 OPTIONAL CONFIGURATION WITH (LF4116AE) INSTALLED, PARTS MARKED WILL NOT BE INSTALLED.
PRODUCTION RELEASE
INITIAL RELEASE
U19 2114
U25 2114
U36 74LS197
U33 74LS273
U32 74LS137
U29 74LS640-1
U20 PAL16R6
U35 NE555
RN2 220/330Ω
U13 74S04
U14 LS02
U30 LS14
P1
P3
STATE SEQUENCER


WESTERN DIGITAL
CORPORATION
WD1002-SHD
031092
SHT 2 OF 4
DRIVE READY
SEEK COMPLETE
INDEX
TRACK 000
WRITE FAULT
WD1015-02 CONTROL PROCESSOR
WD1010-05
WD100-13 ECC
74LS393
DRIVE SELECT 0
DRIVE SELECT 1
HEAD SELECT 0
HEAD SELECT 1
HEAD SELECT 2
DIRECTION
STEP
REDUCE WRITE CURRENT
WRITE GATE


WESTERN DIGITAL
WD1002 - SHD
SCALE
SHT 3 OF 4
WRITE PRECOMP MUX
WRMW
WCLK (2-B5)
5 MHZ (1-B6, 2C6, 3D2)
MFMCLK (2-B5)
10 MHZ
20.000 MHZ
Y1
GROUND PLANE
DR1
DR0
(2-B5) RG
(2-A3) BWG
T/S DIR (1-B7, 3C3, 2-B5)
(1-B2) A11
(4-C8) T0
(4-C8) T1
(4-C8) T2
(4-C8) T3
(3-D8) T/S DIR
WDD
EARLY (2-B4)
LATE (2-B4)
WD (2-B4)
DRDY (2-B4)
DRQ (2-B4)
(1-C2) WDSØ
(1-C3) WDS1


DLY DAT
PUP 1
PUP 2
RDATA
RCLK
+5V
GROUND PLANE A
GROUND PLANE B
GROUND PLANE C
LF411
VCO OUT
VCO IN
J5
TEST CONNECTOR
WD1002-SHD