P3800-031

service information | FIELD CHANGE | Philips Data Systems

system series: P3000 **model:** **main assy:** PMU186-M **nr.** P3500-069
P3800-031

units affected: **est.inst.time:**

date: 850716 **revised:**

title: PMU186 as master.

note: **this change is:** Retrofit on failure

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1. CONDITION : PMU186 will also be used as master (Release 6).

2. CORRECTION : New firmware om PMU186 - 256k 5112 291 92624.

3. REMOVE : IC 1: 5112 208 01593
IC 2: 5112 208 01603

4. ADD : IC 1: 5112 208 01594
IC 2: 5112 208 01604

5. ADJUSTMENTS : None.

6. PARTS : PROM (2764) 12NC: 5112 208 01594
PROM (2764) 12NC: 5112 208 01604

7. STATUS CHANGE : PMU186-256k New 12NC: 5112 291 92625.
Service 12NC (sandwich!) 5322 214 40238 not changed.

8. TEST FACILITIES AFFECTED : None.

9. DOCUMENTS AFFECTED : None.

10. REMARKS : 1. Strapsettings (on PMU186 - CPV).

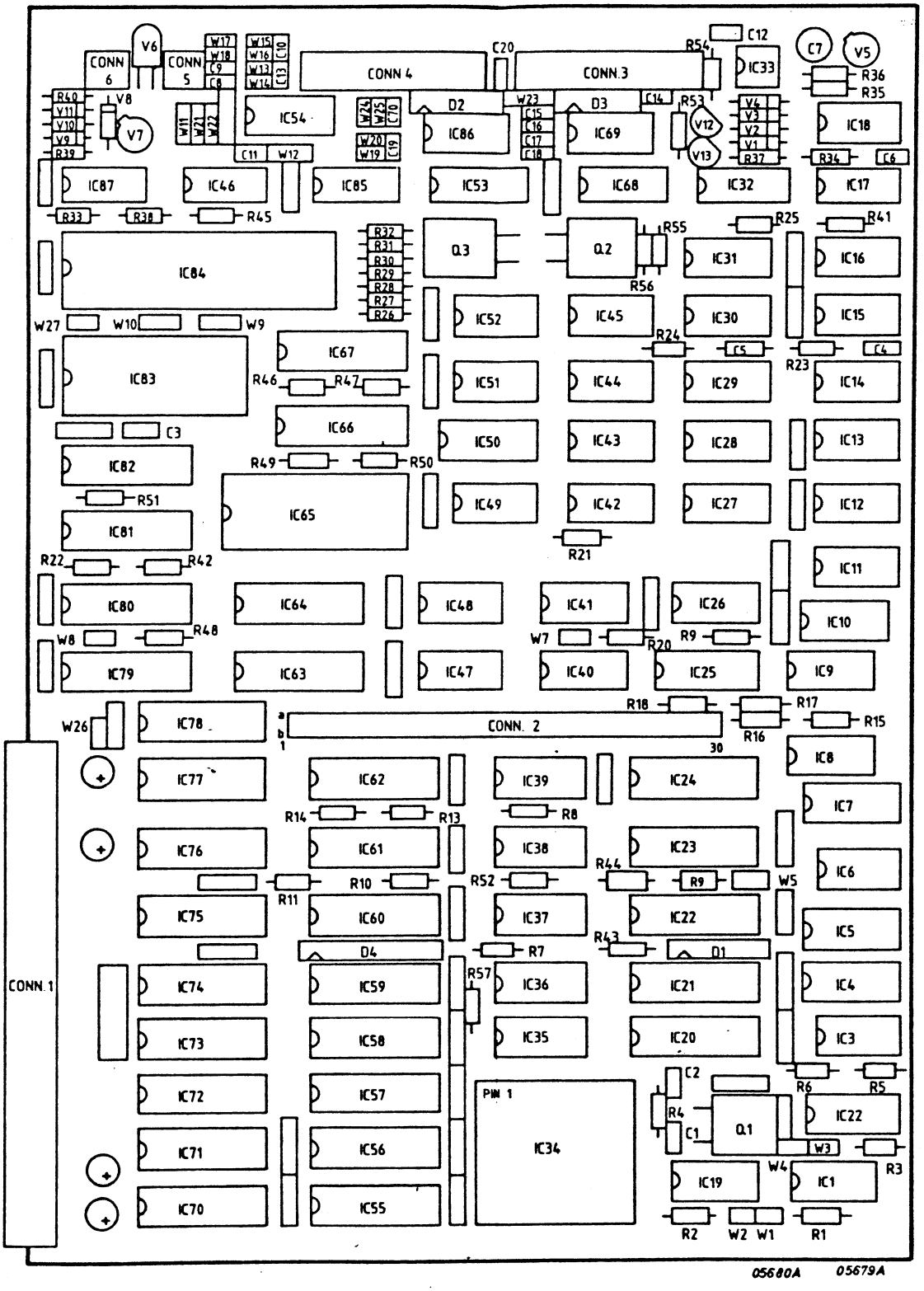
	Master	Slave
W26	Closed	Open
W22	Open	Closed (see manual)
W11	Open	Closed (see manual)

2. PMU186 will be delivered with straps in master position.

3. PROMs can be ordered at:

TDS Apeldoorn
Dept.: CS-MM
Att.: Mr. C. Hilgersom

COMPONENT LOCATION PMU186 CPV



NAME: PMU186 CPV 12NC: 5112 291 9565x	CONFIGURATION INDEX								
CONTENTS	MODIFICATION LEVEL x								
PAGE	1	2	3	4	5	6	7	8	9
	. . .	850301							
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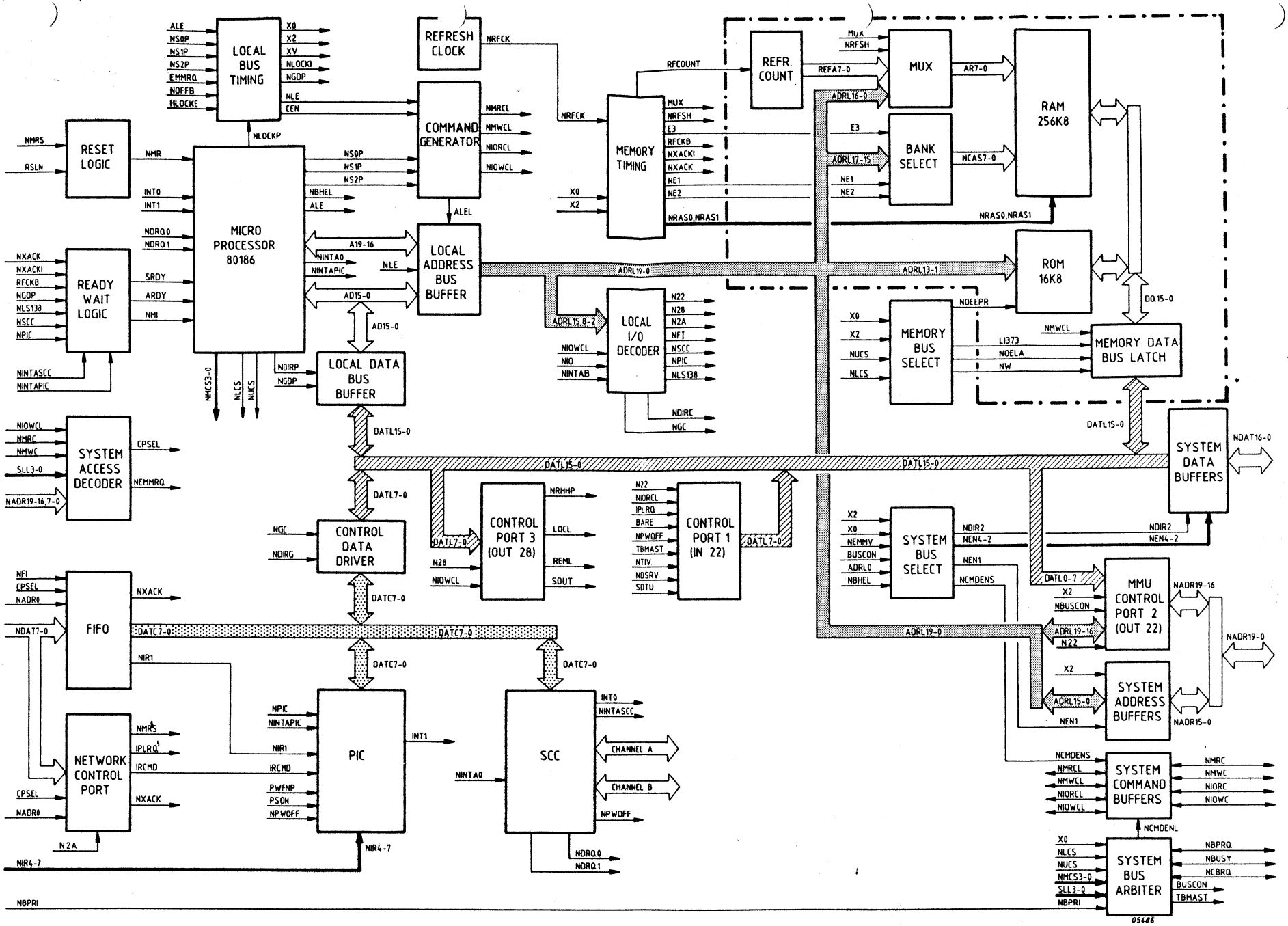
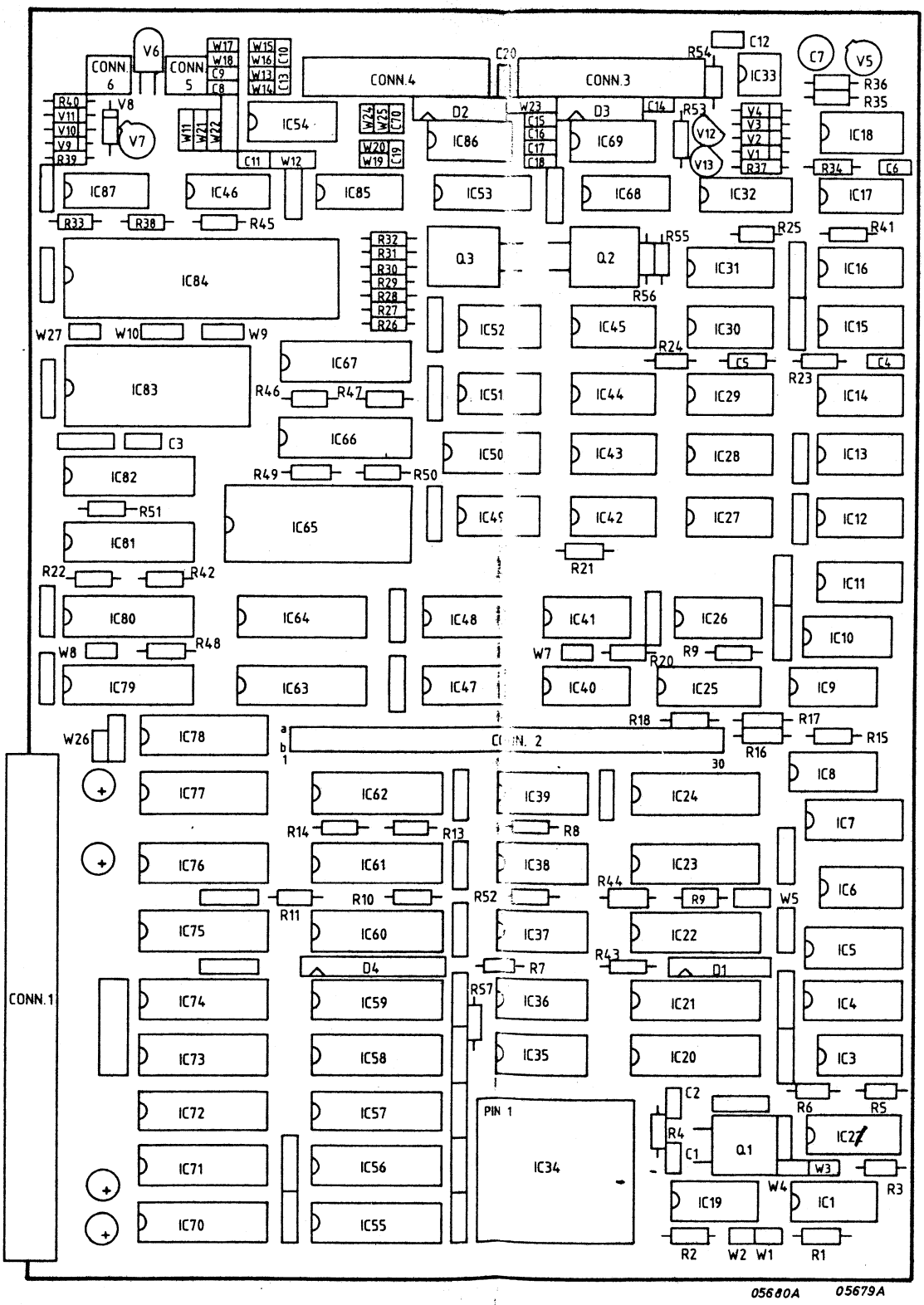
RELEVANT SI-NUMBER: P3500-									
: P3800-									



BLOCK DIAGRAM PMU186 CPV


CONN. 6
CONN. 5
CONN.4
CONN.3
CONN. 2
CONN.1
IC84
IC83
IC82
IC81
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IC79
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IC85
IC86
IC87
IC68
IC69
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Q2
Q3
D1
D2
D3
D4
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V7
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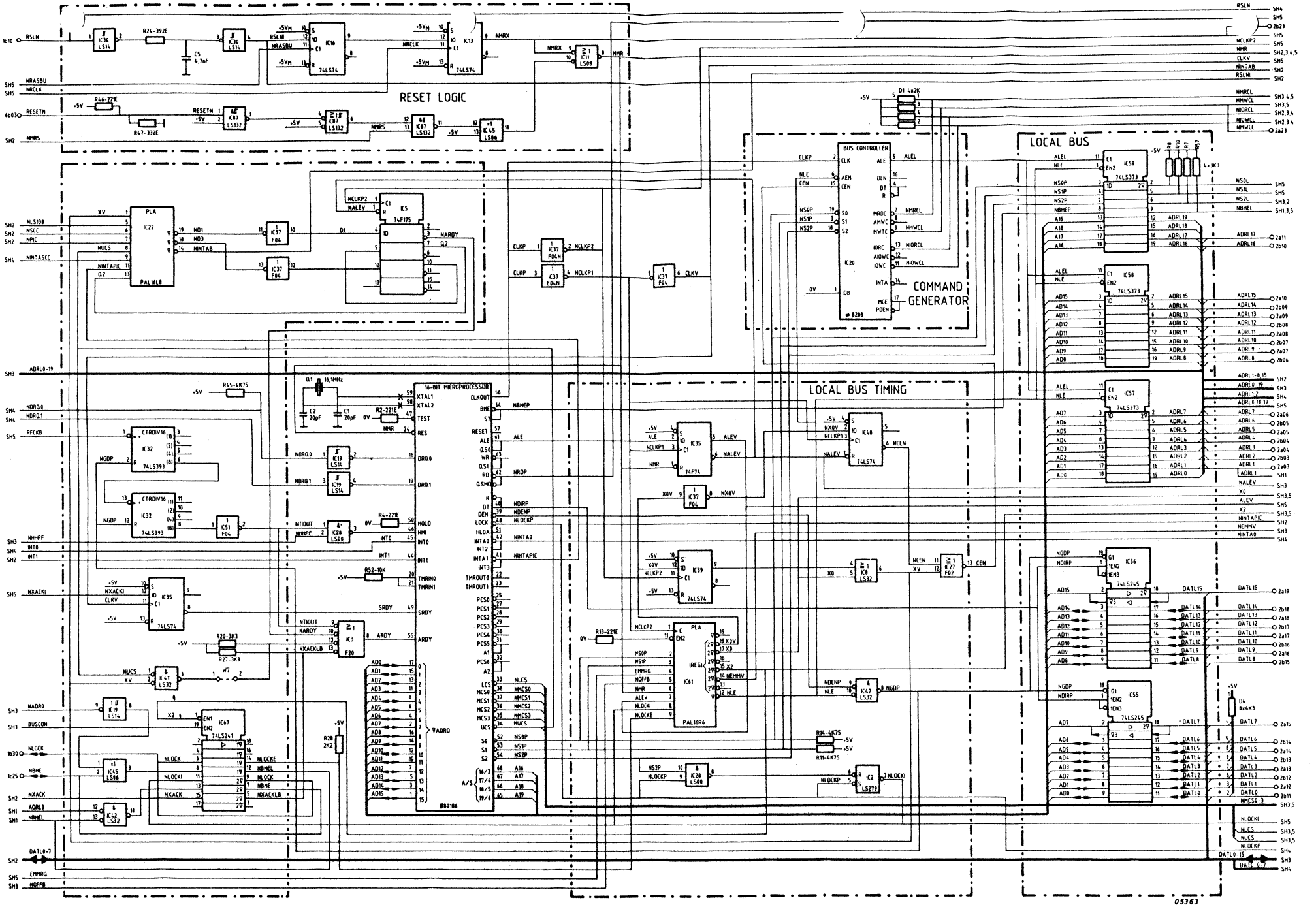
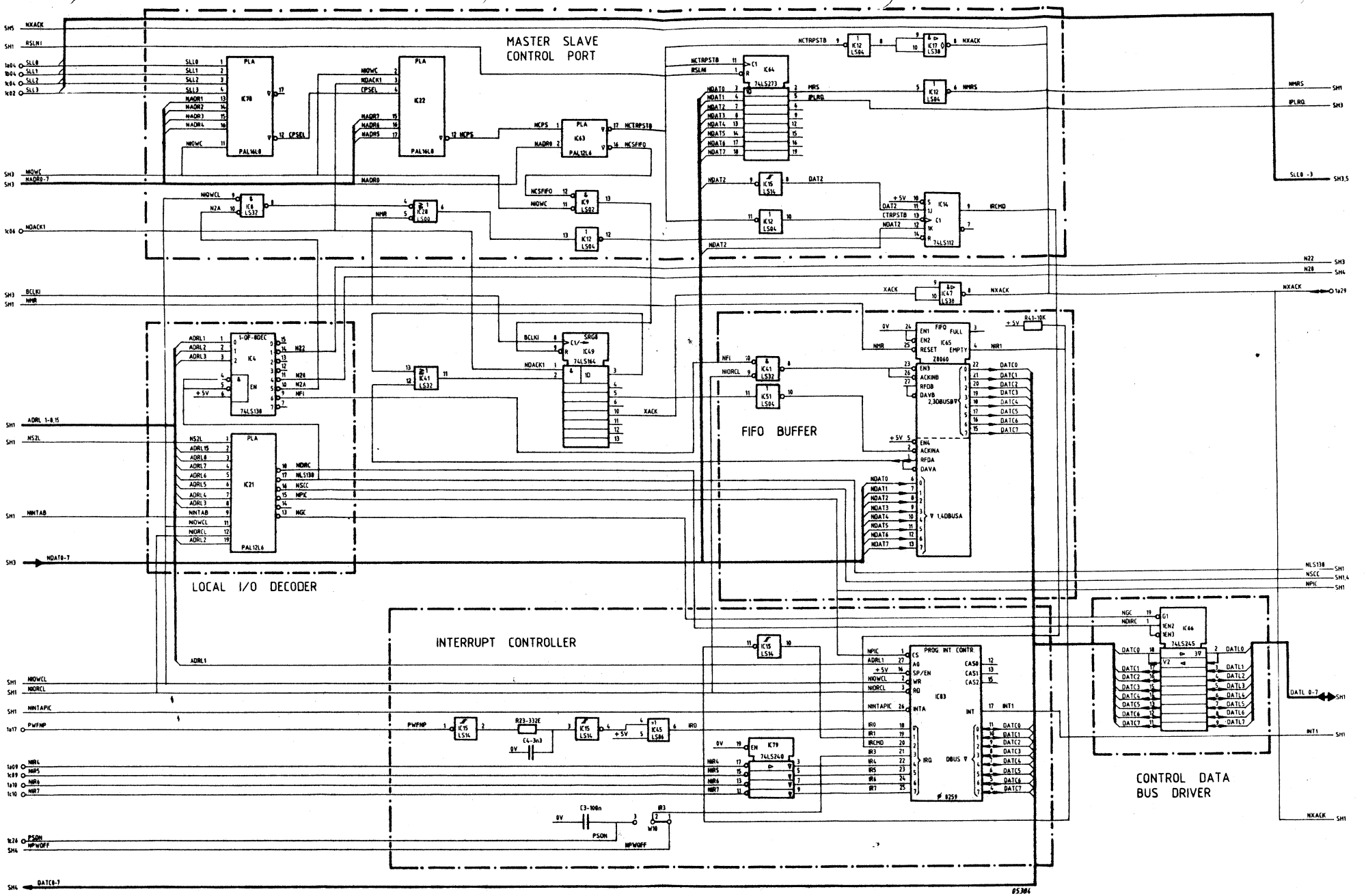
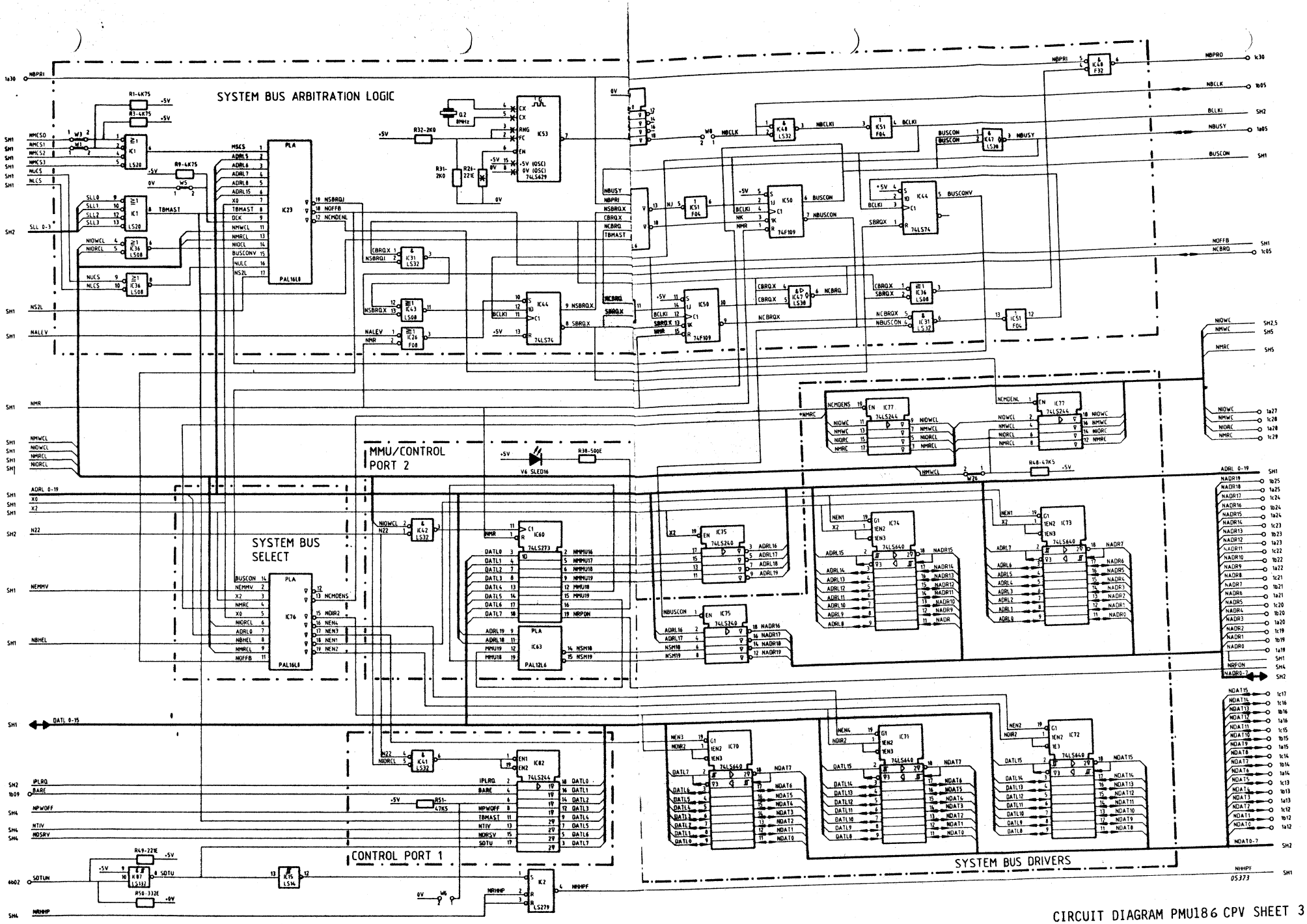


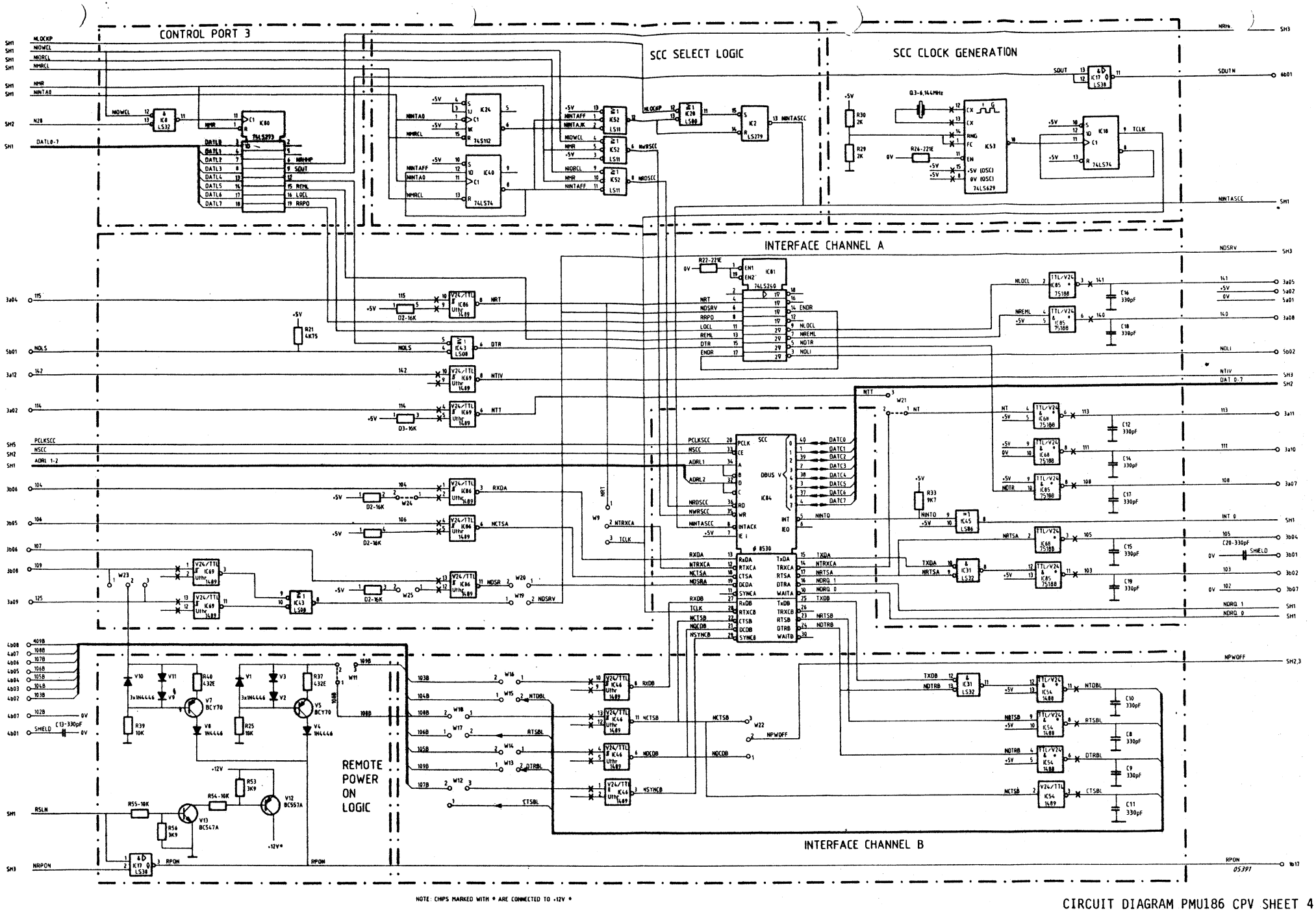
CIRCUIT DIAGRAM PMU186 CPV SHEET 1



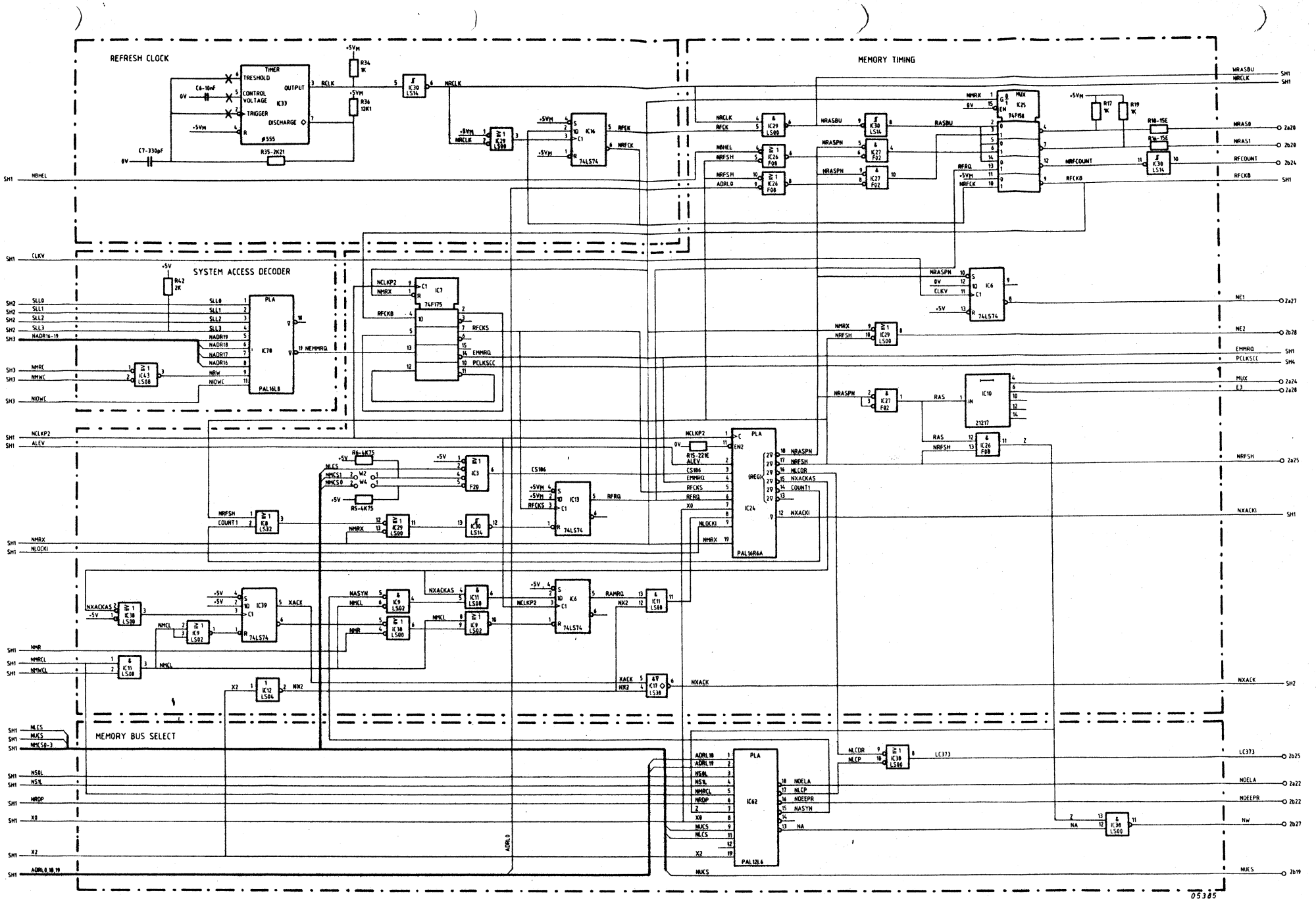
CIRCUIT DIAGRAM PMU186 CPV SHEET 2



CIRCUIT DIAGRAM PMU186 CPV SHEET 3



CIRCUIT DIAGRAM PMU186 CPV SHEET 4



CIRCUIT DIAGRAM PMU186 CPV SHEET 5

PAL DESCRIPTION

IC 21 (PAL 12L6)

$\overline{16} = \overline{01}.\ \overline{02}.\ \overline{03}.\ \overline{04}.\ \overline{05}.\ \overline{06}.\ \overline{07}.\ \overline{08}$

$\overline{15} = \overline{01}.\ \overline{02}.\ \overline{03}.\ \overline{04}.\ \overline{05}.\ \overline{06}.\ \overline{07}.\ 08.\ \overline{19}$

$\overline{18} = \overline{01}.\ \overline{02}.\ \overline{03}.\ \overline{04}.\ \overline{05}.\ \overline{06}.\ \overline{07}.\ \overline{12}$
$+ \overline{01}.\ \overline{09}$
$+ \overline{01}.\ \overline{02}.\ \overline{03}.\ \overline{04}.\ \overline{05}.\ 06.\ \overline{07}.\ 08.\ 19.\ \overline{12}$

$\overline{17} = \overline{01}.\ \overline{02}.\ \overline{03}.\ \overline{04}.\ \overline{05}.\ 06.\ \overline{07}.$

$\overline{13} = \overline{01}.\ \overline{02}.\ \overline{03}.\ \overline{04}.\ \overline{05}.\ \overline{06}.\ \overline{07}.$
$+ \overline{01}.\ \overline{09}$
$+ \overline{01}.\ \overline{02}.\ \overline{03}.\ \overline{04}.\ \overline{05}.\ 06.\ \overline{07}.\ 08.\ 19$

IC 22 (PAL 12L6)

$\overline{19} = \overline{08}.\ \overline{01} + 13.\ \overline{01}$

$\overline{18} = \overline{06}.\ \overline{01} + \overline{09}.\ \overline{01} + \overline{11}.\ \overline{01} + \overline{05}.\ \overline{01}$

$\overline{12} = 17.\ \overline{16}.\ 15.\ \overline{02}.\ 03.\overline{04}$

$\overline{14} = \overline{09} + \overline{11}$

IC 23 (PAL 16L8)

$\overline{19} = \overline{18}.\ \overline{11}.\ \overline{07} + \overline{18}.\ \overline{13}.\ \overline{07} + \overline{18}.\ \overline{14}.\ \overline{07}$

$\overline{12} = 01.\ \overline{07}\ 15$
$+ 03.\ \overline{06}.\ \overline{05}.\ \overline{07}.\ 15.\overline{17}$
$+ 04.\ \overline{06}.\ \overline{05}.\ \overline{07}.\ 15.\overline{17}$
$+ \overline{04}.\ \overline{06}.\ \overline{05}.\ \overline{07}.\ 15.\ \overline{17}.\ 03.\ \overline{02}$
$+ \overline{06}.\ 05.\ \overline{07}.\ \overline{17}.\ 15$
$+ 16.\ \overline{11}.\ \overline{07}.\ \overline{09}.\ 15.$
$+ 16.\ \overline{13}.\ \overline{07}.\ \overline{09}.\ 15$

$\overline{18} = 01.\ \overline{07}$
$+ 03.\ \overline{06}.\ \overline{05}.\ \overline{07}.\ \overline{17}.\ \overline{08}$
$+ 04.\ \overline{06}.\ \overline{05}.\ \overline{07}.\ \overline{17}.\ \overline{08}$
$+ \overline{04}.\ \overline{06}.\ \overline{05}.\ 03.\ \overline{02}.\ \overline{07}.\ \overline{17}.\ 08$
$+ \overline{06}.\ 05.\ \overline{07}.\ \overline{17}$
$+ 16.\ \overline{11}.\ \overline{07}.\ \overline{09}$
$+ 16.\ \overline{13}.\ \overline{07}.\ \overline{09}$

IC 24 (PAL 16R6)

$\overline{17} = \overline{07}.\ 02.\ 05.\ \overline{03}.\ 06$
$+ \overline{07}.\ 02.\ 06.\ \overline{05}$
$+ 07.\ \overline{08}.\ \overline{05}.\ 06$
$+ \overline{07}.\ \overline{03}.\ \overline{08}.\ 06.\ \overline{05}.\ 13$
$+ \overline{17}.\ 13.\ 19$

$\overline{18} = + \overline{07}.\ 02.\ \overline{04}.\ 05.\ 03.\ 17$
$+ \overline{07}.\ 02.\ \overline{04}.\ \overline{05}.\ 03.\ 17$
$+ \overline{07}.\ 02.\ \overline{04}.\ \overline{05}.\ 03.\ 17.\ \overline{06}$
$+ \overline{07}.\ 02.\ \overline{09}.\ \overline{05}.\ 03.\ 17.\ \overline{06}$
$+ \overline{07}.\ \overline{02}.\ 03.\ 13.\ 17$
$+ \overline{18}.\ 14.\ 13$
$+ \overline{17}.\ 14.\ 13$
$+ 07.\ 08.\ 14.\ 15.\ 17.\ 04$

$\overline{16} = \overline{18}.\ 14.\ 19.\ 17$

$\overline{14} = \overline{18}.\ 14.\ 19$

$\overline{15} = 08.\ 17.\ \overline{18}.\ \overline{14}.\ 07.\ 19$

$\overline{13} = 17.\ \overline{18}.\ \overline{07}.\ 19 + \overline{17}.\ \overline{18}.\ \overline{14}.\ 19$

$\overline{12} = \overline{07}.\ \overline{18}.\ 03.\ 17$

IC 61 (PAL16R6)

$\overline{17}: = \overline{19}.\ 15.\ 13.\ 17.\ \overline{04}.\ 16.\ 06$
$+ \overline{19}.\ 15.\ 13.\ \overline{17}.\ 07.\ \overline{04}.\ 06$
$+ \overline{19}.\ 15.\ 13.\ \overline{17}.\ 07.\ 04.\ \overline{18}.\ 16.\ 06$
$+ \overline{19}.\ 15.\ 13.\ \overline{17}.\ \overline{07}.\ 06.$
$+ \overline{19}.\ 15.\ 13.\ \overline{17}.\ \overline{07}.\ \overline{05}.\ 16.\ 06$
$+ \overline{19}.\ 15.\ 13.\ \overline{17}.\ \overline{07}.\ 05.\ 16.\ 06$

$\overline{16}: = \overline{07}.\ \overline{05}.\ \overline{19}.\ \overline{17}.\ 15.\ 13.\ 16.\ \overline{02}.\ 06$
$+ \overline{07}.\ \overline{05}.\ \overline{19}.\ \overline{17}.\ 15.\ 13.\ 16.\ \overline{03}.\ 06$
$+ \overline{07}.\ \overline{05}.\ \overline{19}.\ \overline{17}.\ 15.\ 13.\ \overline{16}.\ \overline{02}.\ 06$
$+ \overline{07}.\ \overline{05}.\ \overline{19}.\ \overline{17}.\ 15.\ 13.\ \overline{16}.\ \overline{03}.\ 06$

$\overline{13}: \quad 04.\ 13.\ 15.\ \overline{17}.\ 07.\ 08$
$+ 04.\ 13.\ 15\ \ 17.\ \overline{16}.\ 06$

$\overline{15}: = 13.\ 15.\ 16.\ 17.04.\ 08.\ 06$
$+ 13.\ \overline{15}.\ 16.\ 17.\ 04$
$+ 13.\ \overline{15}\ .16.\ 17.\ \overline{09}$
$+ \overline{13}.\ 15.\ 16.\ 17$

$\overline{18}: = \overline{17}$

$\overline{14}: = \overline{15}$

$\overline{19}: = 07.\ \overline{02} + 07.\ \overline{03} + \overline{07}.19$

$\overline{12} = \overline{17} + \overline{16}$

IC 62 (PAL12R6)

$\overline{16} = \overline{06}.\ \overline{08}\ \overline{09}$

$\overline{15} = \overline{19}.\ \overline{01}\ \overline{02}$

$\overline{17} = \overline{06}.\ \overline{08}\ \overline{09}$

$\overline{18} = 08.\ 05.\ \overline{19} + \overline{06}.\ \overline{09} + \overline{08}.\ \overline{06}.\ \overline{11}$

$\overline{13} = 08 + 03 + \overline{04}$

IC 63 (PAL 12R6)

$\overline{15} = \overline{09}.\ 11 + 09.\ \overline{11}.\ \overline{19}$

$\overline{14} = 19.\ \overline{11}.\ \overline{12}$

$\overline{13} = 03.\ \overline{04}.\ 06 + 03.\ \overline{04}.\ 07.\ \overline{08}$

$\overline{18} = \overline{07}.\ \overline{06}$

$\overline{17} = \overline{01}.\ 02$

$\overline{16} = \overline{01}.\ \overline{02}$

IC 76 (PAL16L8)

$\overline{19} = 14.\ \overline{07}.\ \overline{08} + \overline{03}.\ \overline{07}.\ \overline{08}$

$\overline{17} = 14.\ \overline{07} + \overline{03}.\ \overline{07}$

$\overline{16} = 14.\ 07.\ \overline{08}.\ + \overline{03}.\ 07.\ \overline{08}$

$\overline{15} = 14.\ \overline{11}.\ 09 + 14.\ \overline{11}.\ 06 + \overline{03}.\ 14$

$\overline{13} = \overline{03}.\ \overline{02}$

$\overline{18} = \overline{03}.\ 14$

IC 78 (PAL16L8)

$\overline{18} = \overline{09}.\ 05.\ 04.\ 06.\ 03$
$+ \overline{09}.\ \overline{05}.\ \overline{04}.\ 06.\ 03$
$+ \overline{09}.\ 05.\ 04.\ \overline{06}.\ \overline{03}$
$+ \overline{09}.\ \overline{05}.\ \overline{04}.\ \overline{06}.\ \overline{03}$

$\overline{19} = \overline{18}.\ 07.\ 02.\ 08.\ 01$
$+ \overline{18}.\ \overline{07}.\ \overline{02}.\ 08.\ 01$
$+ \overline{18}.\ 07.\ 02.\ \overline{08}.\ \overline{01}$
$+ \overline{18}.\ \overline{07}.\ \overline{02}.\ \overline{08}.\ \overline{01}$

$\overline{17} = \overline{11}.\ 16.\ 04.\ 15.\ 03$
$+ \overline{11}.\ \overline{16}.\ \overline{04}.\ 15.\ 03$
$+ \overline{11}.\ 16.\ 04.\ \overline{15}.\ \overline{03}$
$+ \overline{11}.\ \overline{16}.\ \overline{04}.\ \overline{15}.\ \overline{03}$

$\overline{12} \quad \overline{17}.\ 14.\ 02.\ 13.\ 01$
$+ \overline{17}.\ \overline{14}.\ \overline{02}.\ 13.\ 01$
$+ \overline{17}.\ 14.\ 02.\ \overline{13}.\ \overline{01}$
$+ \overline{17}.\ \overline{14}.\ \overline{02}.\ \overline{13}.\ \overline{01}$

CIRCUIT DIAGRAM PMU186 CPV SHEET 6

PAL description

IC 21 (PAL 12L6)

```
/16 = /01./02./03./04./05./06./07./08
/15 = /01./02./03./04./05./06./07. 08./19
/18 = /01./02./03./04./05./06./07./12
     +/01./09
     +/01./02./03./04./05. 06./07. 08. 19./12
/17 = /01./02./03./04./05. 06./07.
/13 = /01./02./03./04./05./06./07.
     +/01./09
     +/01./02./03./04./05. 06./07. 08. 19.
```

IC 22 (PAL 12L6)

```
/19 = /08./01 +  13./01
/18 = /06./01 + /09./01 + /11./01 + /05./01
/12 =  17./16. 15./02. 03./04
/14 = /09 + /11
```

IC 23 (PAL 16L8)

```
/19 = /18./11./07 + /18./13./07 + /18./14./07
/12 =  01./07. 15
     + 03./06./05./07. 15./17
     + 04./06./05./07. 15./17
     +/04./06./05./07. 15./17.03./02
     +/06. 05./07./17. 15
     + 16./11./07./09. 15
     + 16./13./07./09. 15
/18 =  01./07
     + 03./06./05./07./17./08
     + 04./06./05./07./17./08
     +/04./06./05. 06./02./07./17. 08
     +/06. 05./07./17
     + 16./11./07./09
     + 16./13./07./09
```

IC 24 (PAL 16R6)

```
/17 = /07. 02. 05./03. 06
     +/07. 02. 06./05
     + 07./08./05. 06
     +/07./03./08. 06./05. 13
     +/17. 13. 19
/18 = /07. 02./04. 05. 03. 17
     +/07. 02./04./05. 03. 17
     +/07. 02./04./05. 03. 17./06
     +/07. 02./09./05. 03. 17./06
     +/07./02. 03. 13. 17
     +/18. 14. 13
     +/17. 14. 13
     + 07. 08. 14. 15. 17. 04
/16 = /18. 14. 19. 17
/14 = /18. 14. 19
/15:=  08. 17 ./18./14. 07. 19
/13:=  17./18./07. 19 +/17./18./14. 19
/12 = /07./18. 03. 17
```

```
IC 61 (PAL16R6)      /17:= /19. 15. 13. 17./04. 16. 06
                          +/19. 15. 13./17. 07./04. 06
                          +/19. 15. 13./17. 07. 04./08. 16. 06
                          +/19. 15. 13./17./07. 06
                          +/19. 15. 13./17./07./05. 16. 06
                          +/19. 15. 13./17./07. 05. 16. 06
                     /16:= /07./05./19./17. 15. 13. 16./02. 06
                          +/07./05./19./17. 15. 13. 16./03. 06
                          +/07./05./19./17. 15. 13./16./02. 06
                          +/07./05./19./17. 15. 13./16./03. 06
                     /13:=  04. 13. 15./17. 07. 08
                          + 04. 13. 15. 17./16. 06
                     /15:=  13. 15. 16. 17. 04. 08. 06
                          + 13./15. 16. 17. 04
                          + 13./15. 16. 17./09
                          +/13. 15. 16. 17
                     /18:= /17
                     /14:= /15
                     /19:=  07./02+ 07./03 +/07./19
                     /12 = /17+/16

IC62 (PAL12L6)       /16 = /06./08./09
                     /15 = /19./01./02
                     /17 = /06./08./09
                     /18 =  08. 05./19 +/06./09 +/08./06./11
                     /13 =  08+ 03+/04

IC63 (PAL12L6)       /15 = /09. 11 + 09./11./19
                     /14 =  09./11./12
                     /13 =  03./04. 06 + 03./04. 07./08
                     /18 = /07./06
                     /17 = /01. 02
                     /16 = /01./02

IC76 (PAL16L8)       /19 =  14./07./08 +/03./07./08
                     /17 =  14./07 +/03./07
                     /16 =  14. 07./08 +/03. 07./08
                     /15 =  14./11. 09 + 14./11. 06 +/03. 14
                     /13 = /03./02
                     /18 = /03. 14

IC78 (PAL16L8)       /18 = /09. 05. 04. 06. 03
                          +/09./05./04. 06. 03
                          +/09. 05. 04./06./03
                          +/09./05./04./06./03
                     /19 = /18. 07. 02. 08. 01
                          +/18./07./02. 08. 01
                          +/18. 07. 02./08./01
                          +/18./07./02./08./01
                     /17 = /11. 16. 04. 15. 03
                          +/11./16./04. 15. 03
                          +/11. 16. 04./15./03
                          +/11./16./04./15./03
                     /12 = /17. 14. 02. 13. 01
                          +/17./14./02. 13. 01
                          +/17. 14. 02./13./01
                          +/17./14./02./13./01
```

CONNECTOR 1

	a	b	c
1	+ 5V	+ 5V	+ 5V
2	OV	+ 5V	SLL3
3	OV	OV	OV
4	SLL0	SLL1	SLL2
5	NBUSY	NBCLK	NCBRQ
6	NDRQ1	NIR3	NDACK1 (SLL9)
7	NDRQ2	SYN	NTC1 (SLL10)
8	NIR0	TOUT 2	NIR1
9	NIR4	BARE	NIR5
10	NIR6	RSLN	NIR7
11	OV	OV	OV
12	NDAT0	NDAT1	NDAT2
13	NDAT3	NDAT4	NDAT5
14	NDAT6	NDAT7	NDAT8
15	NDAT9	NDAT10	NDAT11
16	NDAT12	NADAT13	NADAT14
17	PFWN	RPON	NDAT15
18	OV	OV	OV
19	NADR0	NADR1	NADR2
20	NADR3	NADR4	NADR5
21	NADR6	NADR7	NADR8
22	NADR9	NADR10	NADR11
23	NADR12	NADR13	NADR14
24	NADR15	NADR16	NADR17
25	NADR18	NADR19	NBHE
26	NAIOWC	RESV1	RESV5
27	NIOWC	RESV2	NAMWC
28	NIORC	RESV3	NMWC
29	NXACK	RESV4	NMRC
30	NBPRI*	NLOCK	NBPRO
31	+12V	+ 5VM	+ 5VM
32	-12V	- 5V	NBREQ

CONNECTOR 2

	a	b
1	OV	OV
2	+5VM	+5VM
3	ADRL1	ADRL2
4	ADRL3	ADRL4
5	ADRL5	ADRL6
6	ADRL7	ADRL8
7	ADRL9	ADRL10
8	ADRL11	ADRL12
9	ADRL13	ADRL14
10	ADRL15	ADRL16
11	ADRL17	DATL0
12	DATL1	DATL2
13	DATL3	DATL4
14	DATL5	DATL6
15	DATL7	DATL8
16	DATL9	DATL10
17	DATL11	DATL12
18	DATL13	DATL14
19	DATL15	NUCSI
20	NRAS0	NRASI
21	X	X
22	NOELA	NOEEPR
23	NMWCL2	NMRX
24	MUX	RFCOUNT
25	NRFSH	LC373
26	X	X
27	NE1	NW
28	E3	NE2
29	+5V	+5V
30	OV	OV

CONNECTOR 3

	a	b
1		A101
2	A114	A103
3		A104
4	A115	A105
5	A141	A106
6		A107
7	A108.2	A102
8	A140	A109
9	A125	
10	A111	
11	A113	
12	A142	
13	///////	

CONNECTOR 4

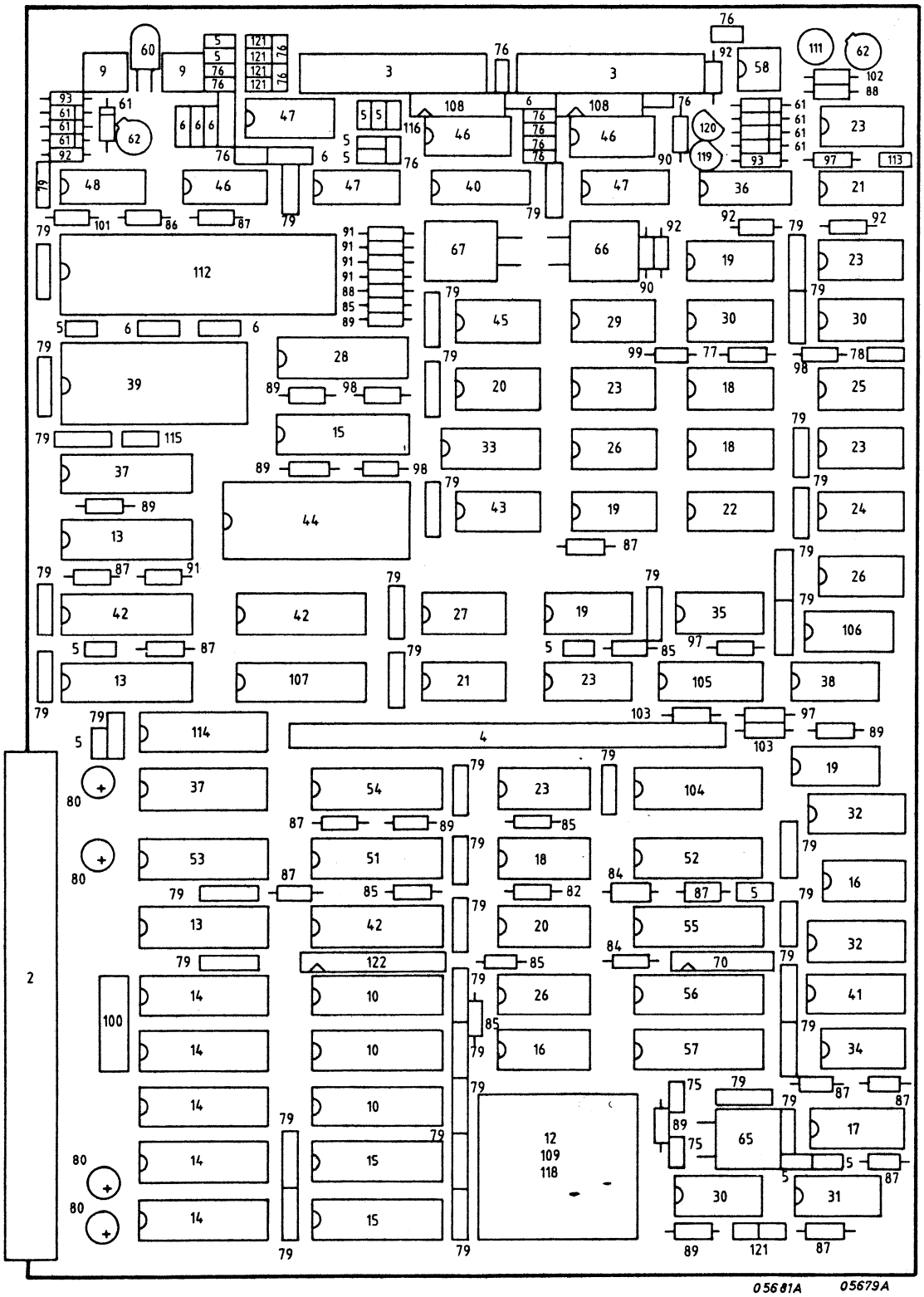
	a	b
1		B101
2		B103
3		B104
4		B105
5		B106
6		B107
7	B108.2	B102
8		B109
9		
10		
11		
12		
13	///////	

CONNECTOR 5

	a	b
1	OV	NOLS
2	+5V	NOLI
3	DUMMY	

CONNECTOR 6

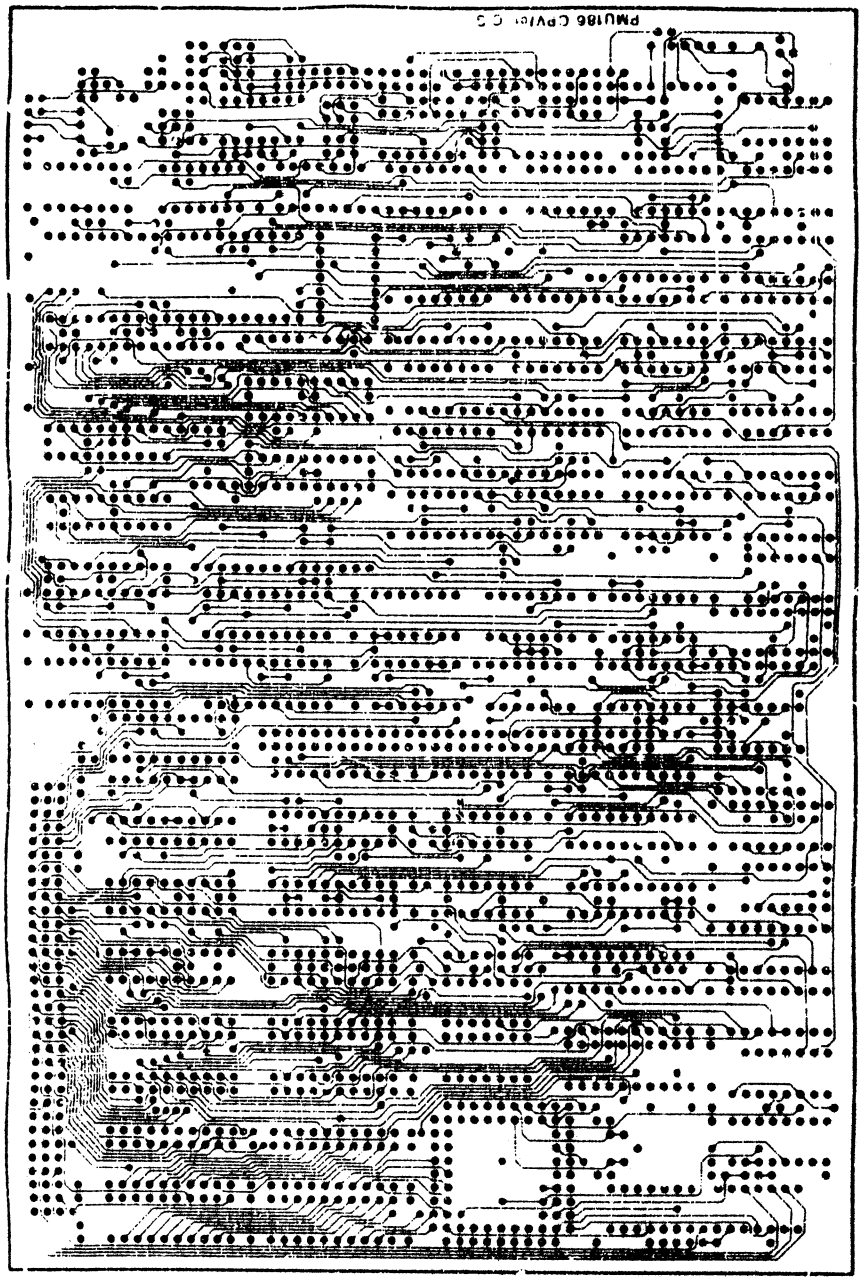
	a	b
1	OV	SDUTN
2	OV	SDTUN
3	DUMMY	RESETN


05681A
05679A

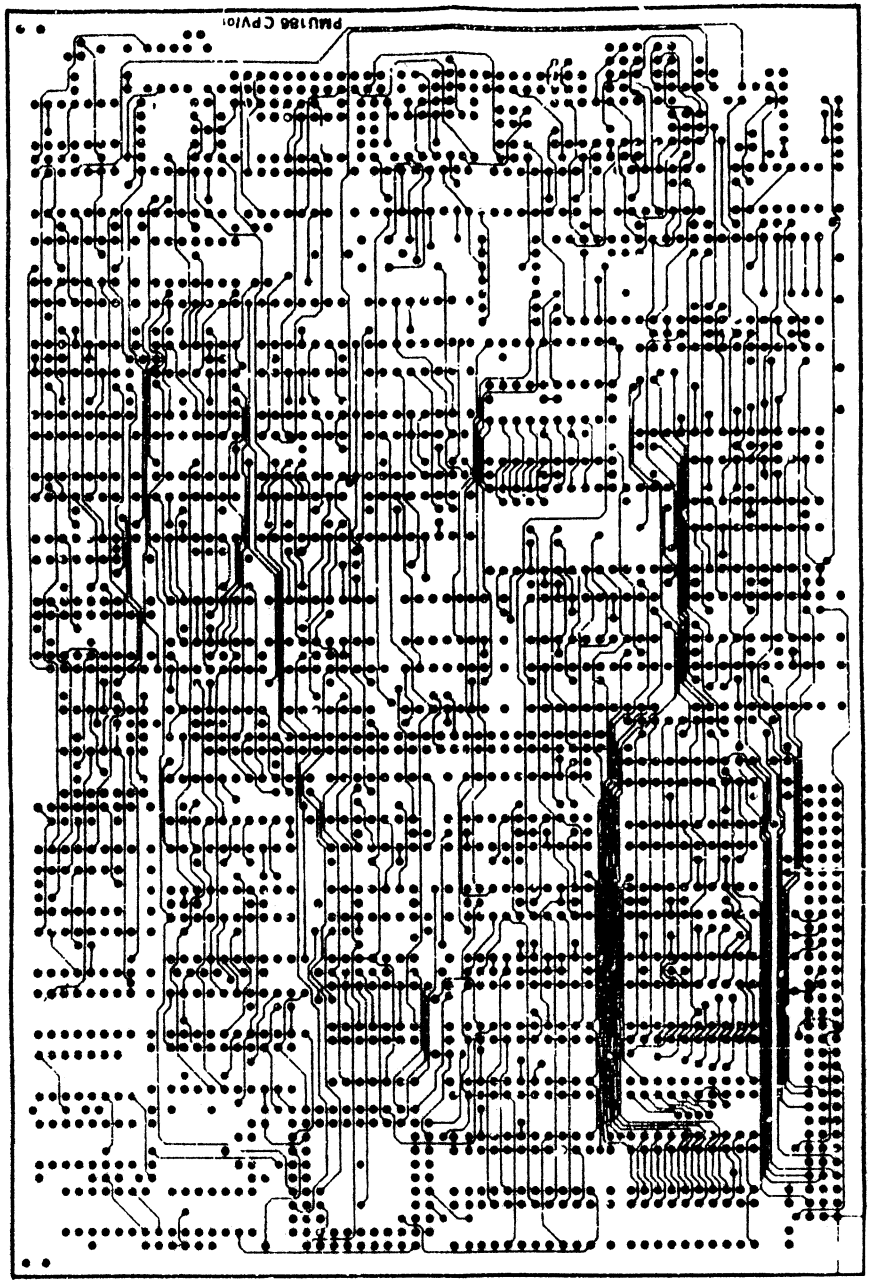
PARTS LIST PMU186 CPV (5112 291 9565x)

POSNR:	12NC:	SPEC:
2	5322 265 64104	MALE PLUG 96POL
3	5322 267 54179	CONN
5	5322 265 64028	CONN 2P
6	5322 265 64028	CONN 3P
7	5322 263 64007	CONN 2POL
9	5322 267 50537	CONN 5POL
10	5322 209 86062	IC SN74LS373J
12	5322 209 82174	IC IAPX186
13	5322 209 85862	IC SN74LS240N
14	5322 209 81572	IC SN74LS640N
15	5322 209 86225	IC 74LS245N
16	5322 209 81474	IC 74F74PC
17	5322 209 85346	IC SN74LS279N
18	5322 209 84823	IC SN74LS00N
19	5322 209 85311	IC N74LS32N
20	5322 209 81577	IC 74F04PC
21	5322 209 85605	IC 74LS38
23	4822 209 80782	IC SN74LS74AN
24	4822 209 80783	IC SN74LS04N
25	5322 209 84971	IC N74LS112N
26	5322 209 84995	IC SN74LS08N
27	5322 209 81529	IC 74F32PC
28	5322 209 85873	IC SN74LS241N
29	5322 209 84997	IC SN74LS86N
30	5322 209 85199	IC SN74LS14N
31	5322 209 85549	IC SN74LS20N
32	5322 209 81542	IC 74F175PC
33	5322 209 81669	IC 74F109PC
34	5322 209 82013	IC 74F20PC
35	5322 209 81574	IC 74F08PC
36	4822 209 80447	IC SN74LS393N
37	5322 209 86017	IC SN74LS244N
38	5322 209 85312	IC N74LS02N
39	5322 209 86492	IC P8259A
40	5322 209 81589	IC SN74LS629N-00
41	5322 209 85647	IC N74LS138N
42	5322 209 85792	IC SN74LS273N
43	5322 209 81487	IC N74LS164N
44	5322 209 82024	IC Z8060PS
45	5322 209 85604	IC SN74LS11N
46	5322 209 86103	IC SN75189AN
47	5322 209 84307	IC SN75188N
48	5322 209 85201	IC SN74LS132N
51	5322 209 82157	IC PAL16R6CNSHRP-1
52	5322 209 82186	IC PAL16L8CNSHRP-2
53	5322 209 82158	IC PAL16L8CNSHRP-3
54	5322 209 82159	IC PAL12L6CNSHRP-4

(TO BE CONTINUED)

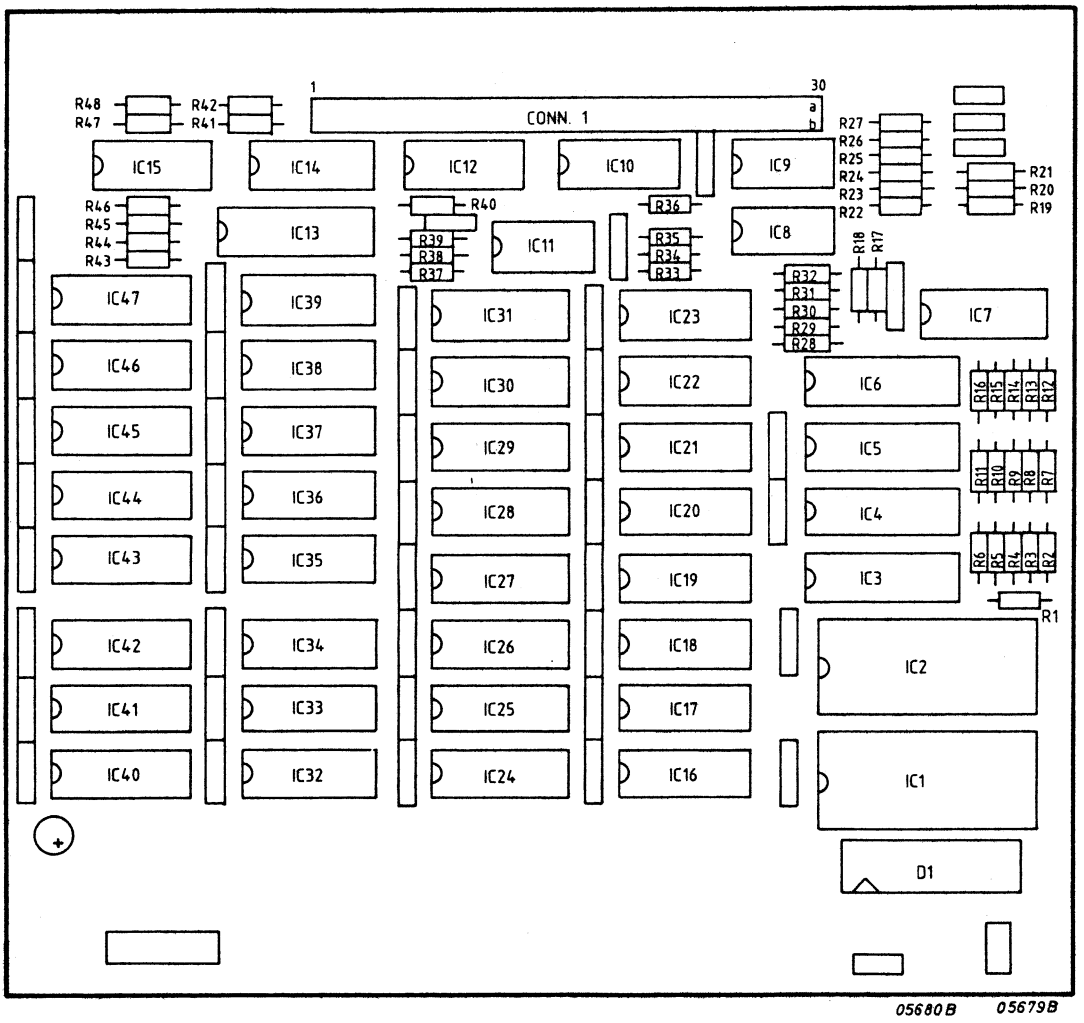


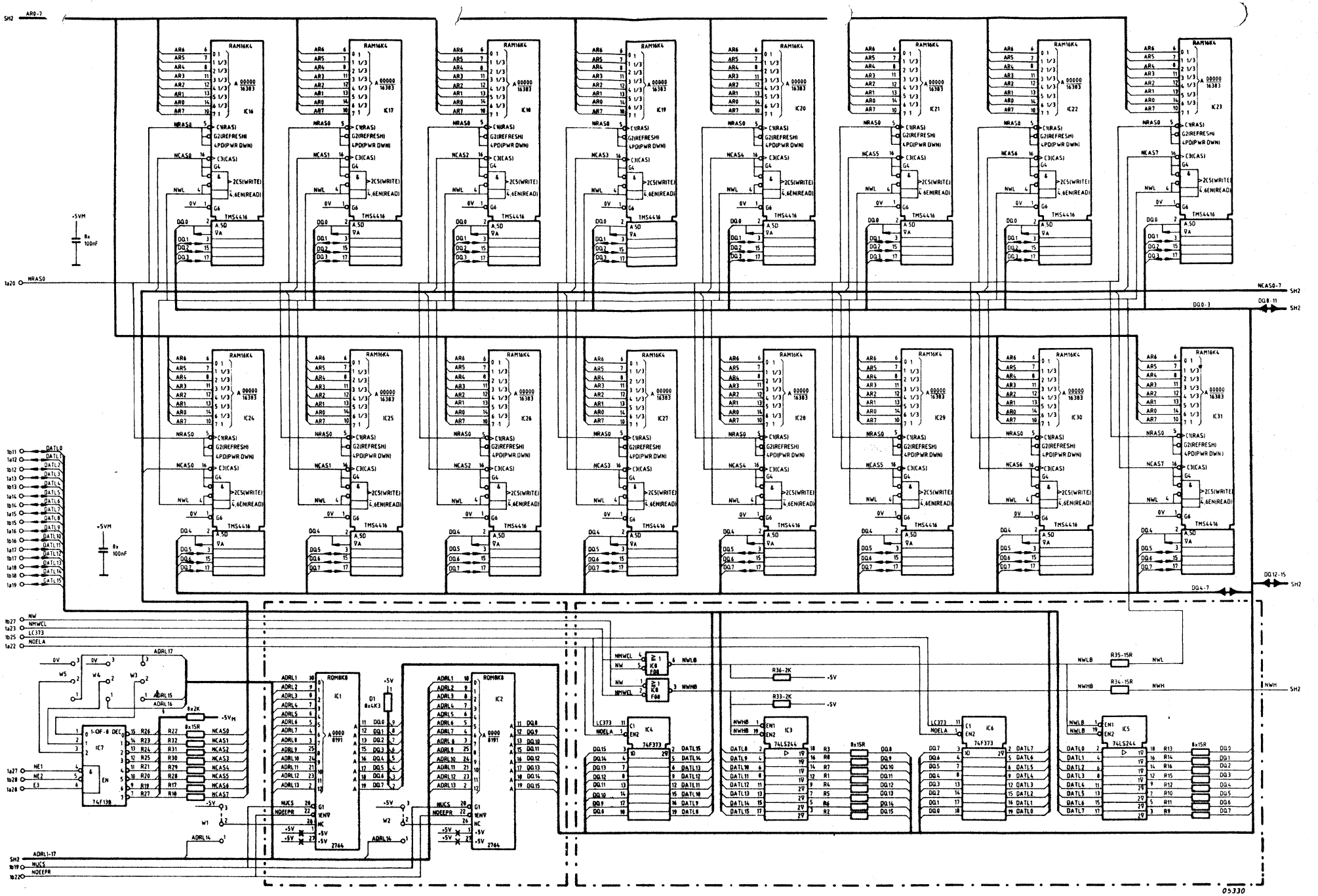
Layer 2



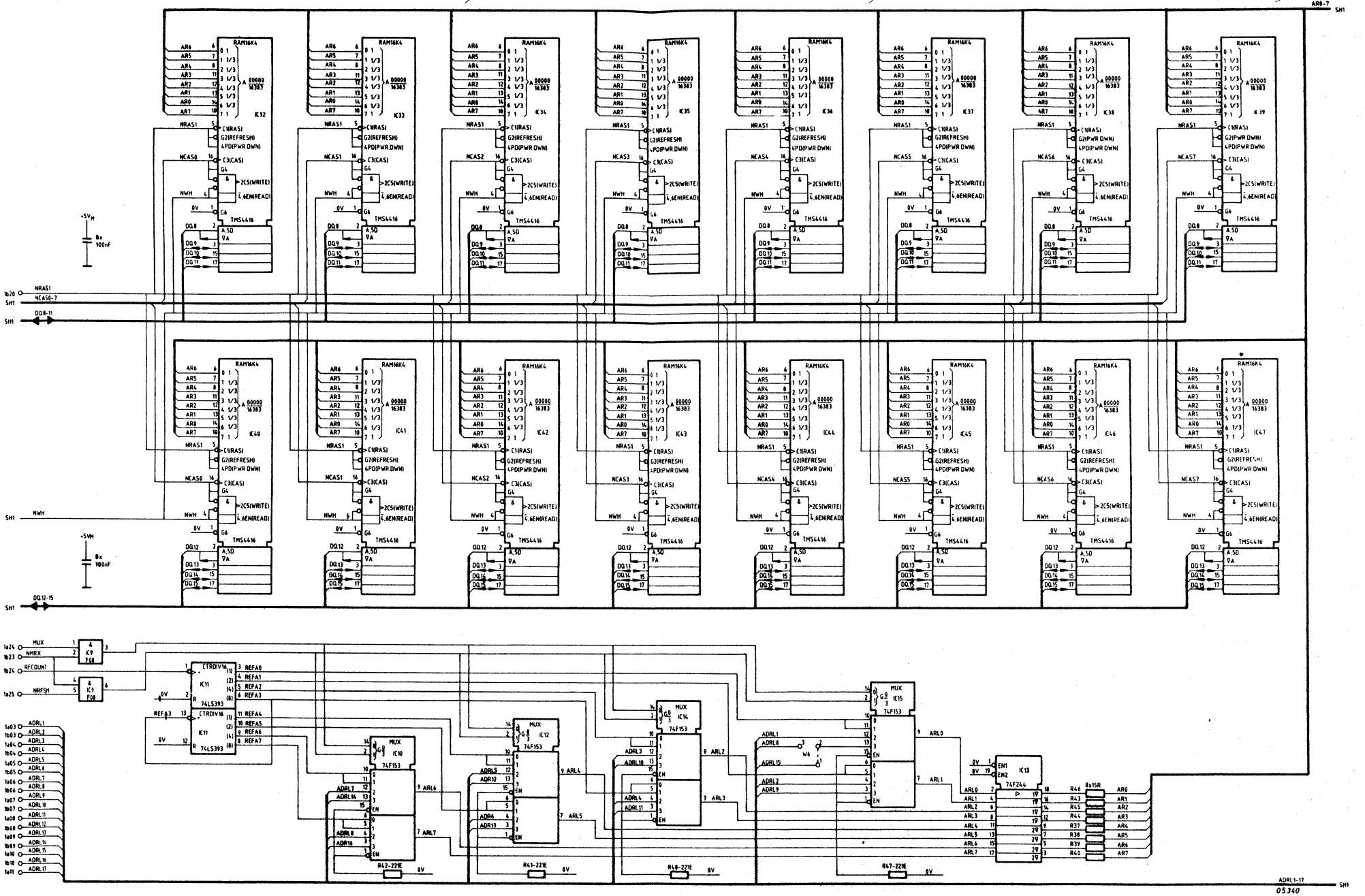
Layer 1

NAME: PMU186M 12NC: 5112 291 9262x	CONFIGURATION INDEX								
CONTENTS	MODIFICATION LEVEL x								
	PAGE	1	2	3	4	5	6	7	8	9
- Contents	6- 1	. . . . .			850301					
- Component Location	6- 2	. . . . .			850301					
- Circuit Diagram Sheet 1	6- 3	. . . . .			850301					
Sheet 2	6- 5	. . . . .			850301					
- Connector Layout	6- 7	. . . . .			850301					
- Parts Location	6- 8	. . . . .			850301					
- Parts List	6- 9	. . . . .			850301					
- Printed Wiring	6-11	. . . . .			850301					
RELEVANT SI-NUMBER: P3500-										
: P3800-										


1
30
CONN. 1
a
b
R48
R47
R42
R41
R27
R26
R25
R24
R23
R22
R21
R20
R19
IC15
IC14
IC12
IC10
IC9
R46
R45
R44
R43
R40
R36
R39
R38
R37
IC13
IC11
R35
R34
R33
IC8
R18
R17
R32
R31
R30
R29
R28
IC7
IC47
IC39
IC31
IC23
IC46
IC38
IC30
IC22
IC6
R16
R15
R14
R13
R12
IC45
IC37
IC29
IC21
IC5
R11
R10
R9
R8
R7
IC44
IC36
IC28
IC20
IC4
IC43
IC35
IC27
IC19
IC3
R6
R5
R4
R3
R2
R1
IC42
IC34
IC26
IC18
IC2
IC41
IC33
IC25
IC17
IC40
IC32
IC24
IC16
IC1
D1
05680B
05679B



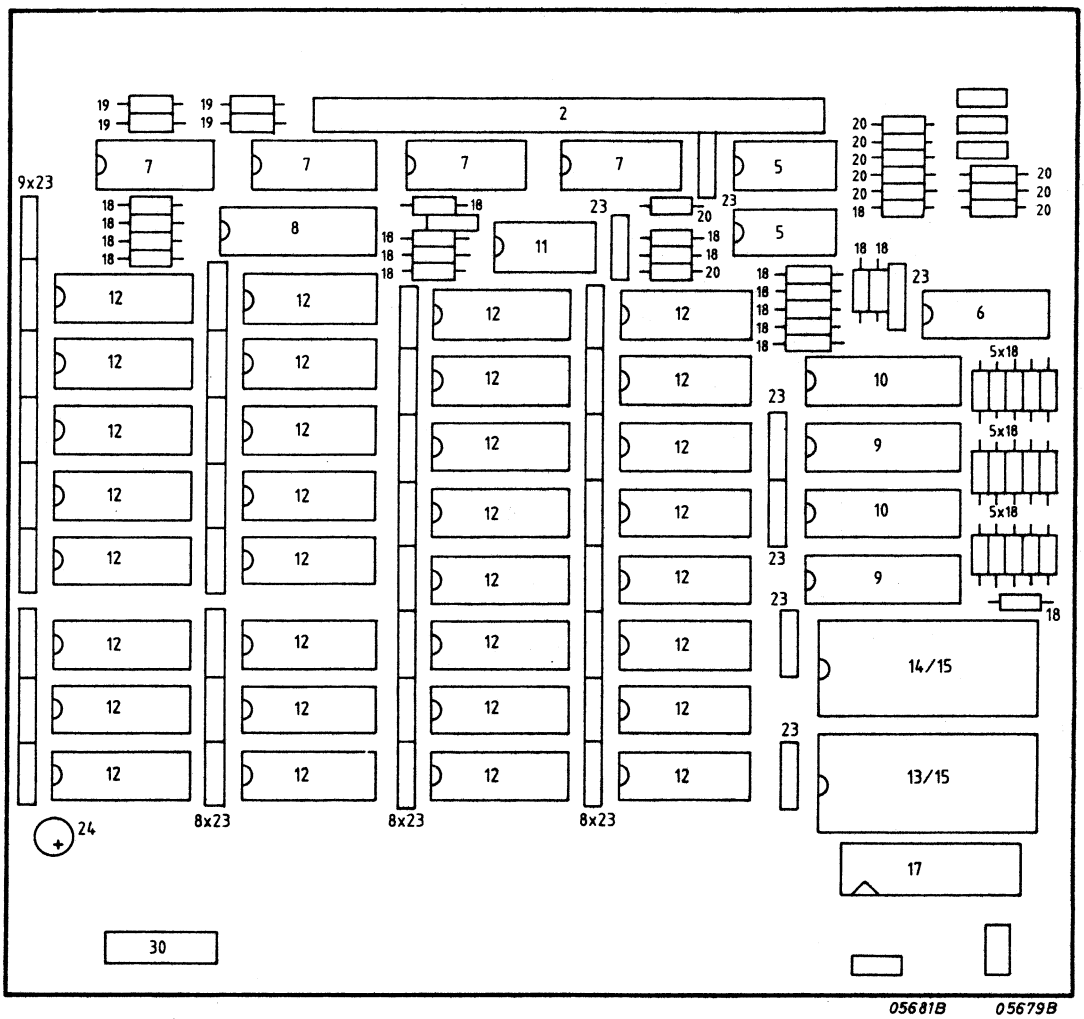
CIRCUIT DIAGRAM PMU186M-256K SHEET 1



CIRCUIT DIAGRAM PMU186M-256K SHEET 2

CONNECTOR 1

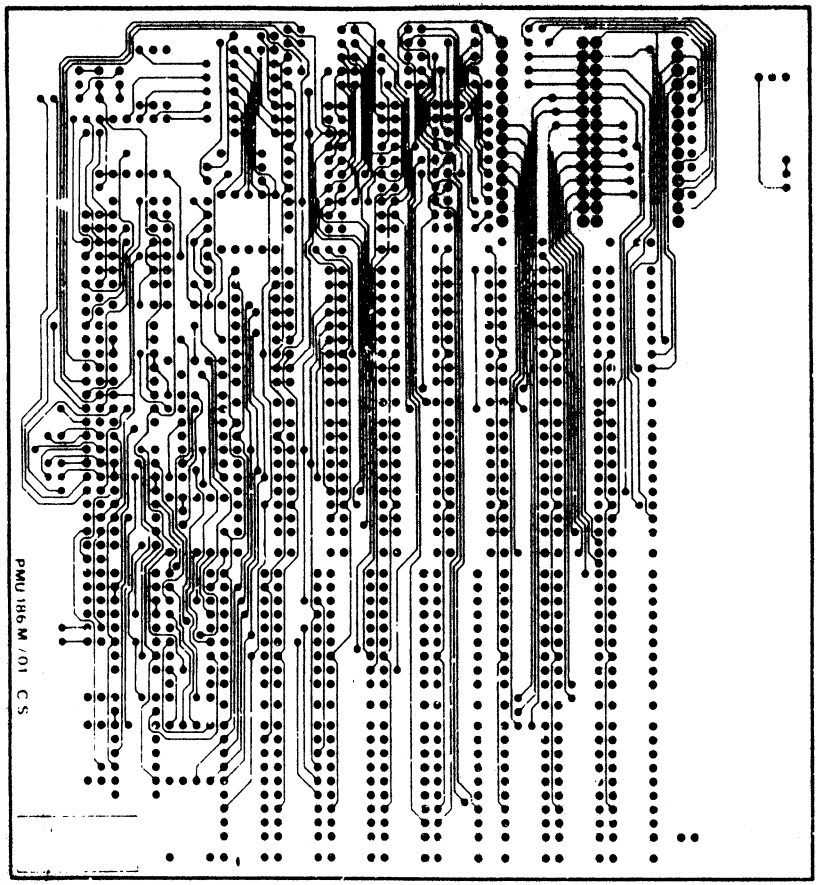
	a	b
1	0V	0V
2	+5VM	+5VM
3	ADRL1	ADRL2
4	ADRL3	ADRL4
5	ADRL5	ADRL6
6	ADRL7	ADRL8
7	ADRL9	ADRL10
8	ADRL11	ADRL12
9	ADRL13	ADRL14
10	ADRL15	ADRL16
11	ADRL17	DATL0
12	DATL1	DATL2
13	DATL3	DATL4
14	DATL5	DATL6
15	DATL7	DATL8
16	DATL9	DATL10
17	DATL11	DATL12
18	DATL13	DATL14
19	DATL15	NUCS
20	NRAS0	NRAS1
21		
22	NOELA	NOEEPR
23	NMWCL2	NMRX
24	MUX	RFCOUNT
25	NRFSH	LC373
26		
27	NE1	NW
28	E3	NE2
29	+5V	+5V
30	0V	0V


19
19
19
19
2
7
7
7
7
5
20
20
20
20
20
18
20
20
20
9x23
18
18
18
18
8
18
18
18
11
23
20
23
18
18
20
5
18 18
23
18
18
18
18
18
6
12
10
5x18
9
10
9
14/15
13/15
17
8x23
8x23
8x23
24
30
05681B
05679B

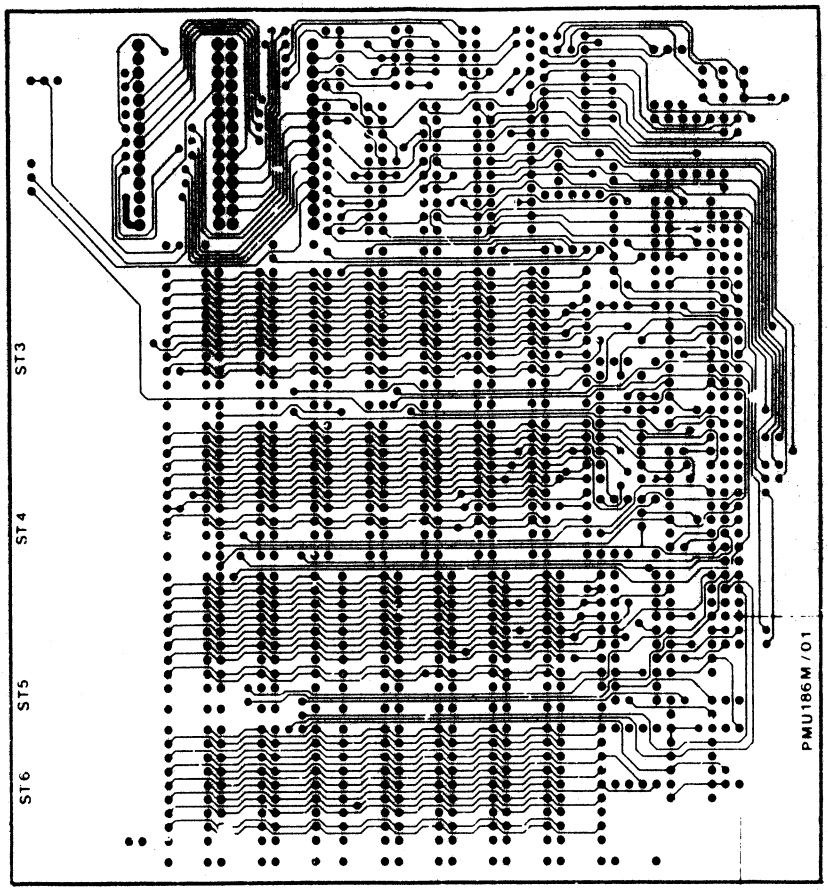
PARTS LIST PMU186M-256K

POSNR:	12NC:	SPEC:
5	5322 209 81574	IC 74F08PC
6	5322 209 82366	IC 74F138PC
7	5322 209 81575	IC 74F153PC
8	5322 209 81128	IC 74F244PC
9	5322 209 86017	IC N74LS244N
10	5322 209 82035	IC 74F373PC
11	4822 209 80447	IC N74LS393N
12	4822 209 10571	IC TMS4416-15NL
18	4822 116 51221	RES 15E 1% 0.4W
19	4822 116 51223	RES 221E 1% 0.4W
20	5322 116 54572	RES 2KO 1% 0.4W
23	5322 122 10313	CAP 100NF
24	5322 124 21335	CAP 33UF 25V
13	(5112 208 01594)	PROM PMU186M-256K-1
14	(5112 208 01604)	PROM PMU186M-256K-2
17	5322 111 90483	RNW 332191 (DICK)

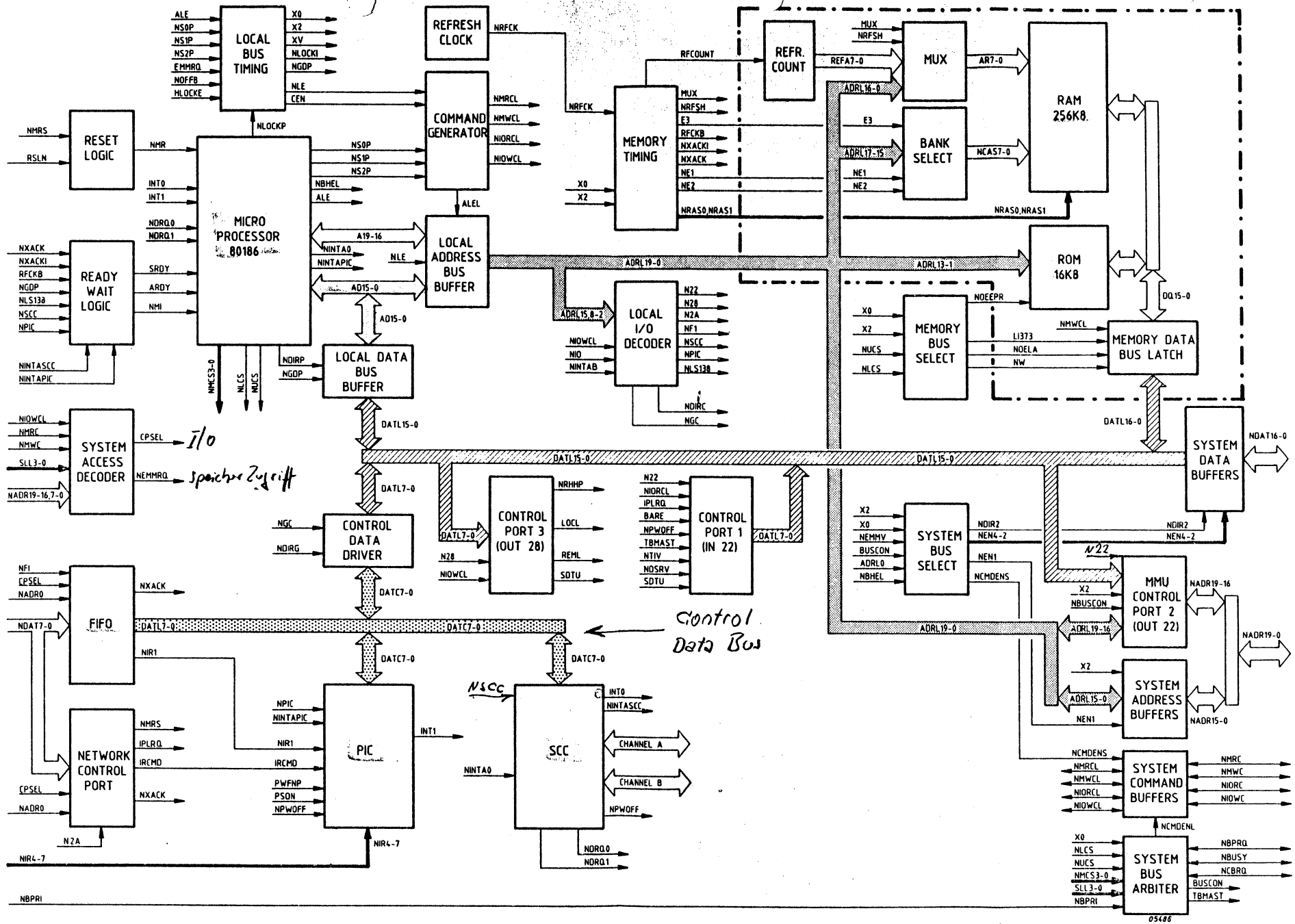
( ) means Factory Nr. This item cannot be ordered via Concern Service

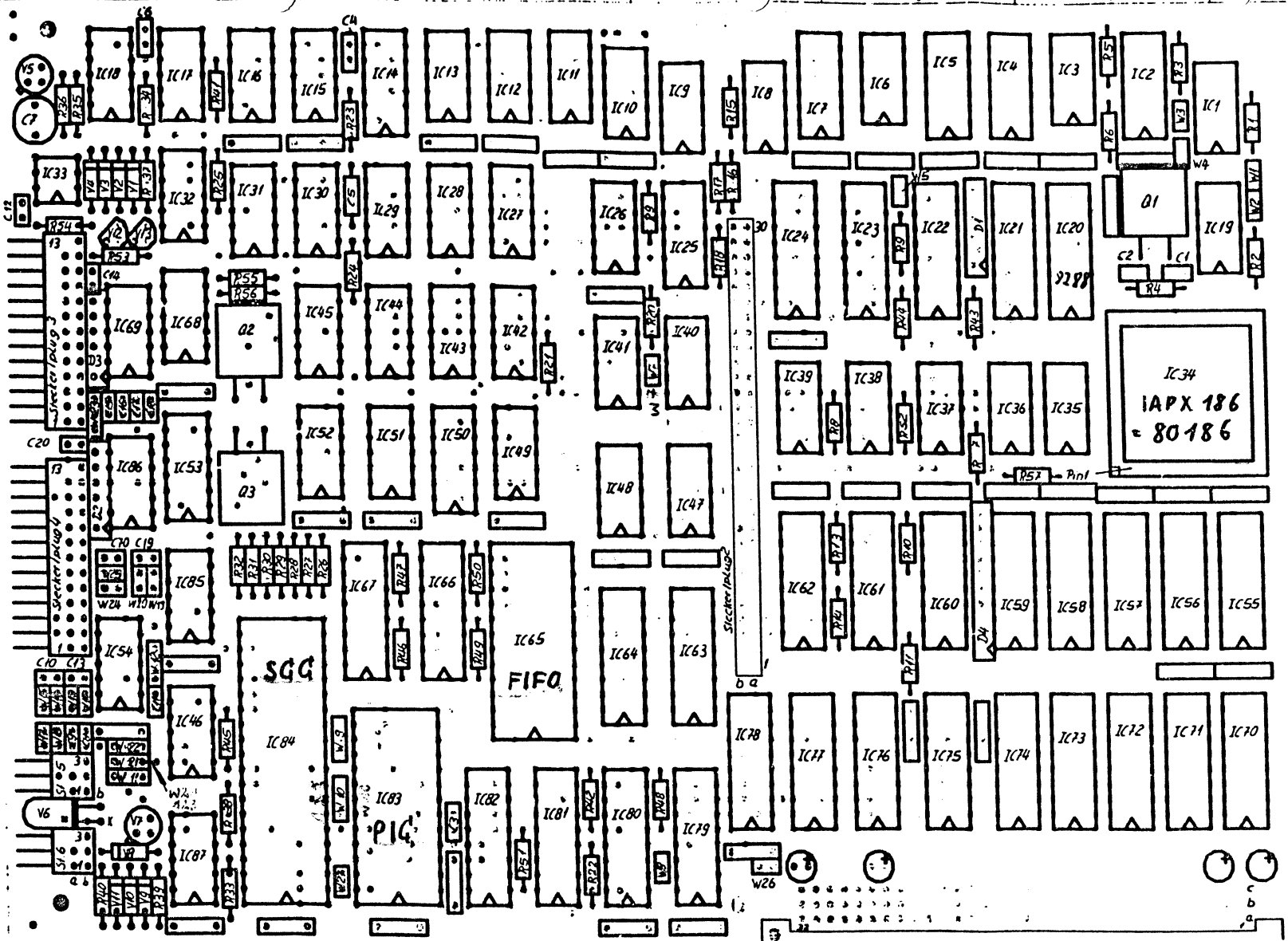


Layer 2



Layer 1


LOCAL BUS TIMING
REFRESH CLOCK
COMMAND GENERATOR
RESET LOGIC
MICRO PROCESSOR 80186
READY WAIT LOGIC
LOCAL ADDRESS BUS BUFFER
MEMORY TIMING
REFR. COUNT
MUX
RAM 256K8
BANK SELECT
ROM 16K8
LOCAL DATA BUS BUFFER
LOCAL I/O DECODER
MEMORY BUS SELECT
MEMORY DATA BUS LATCH
SYSTEM ACCESS DECODER
SYSTEM DATA BUFFERS
CONTROL DATA DRIVER
CONTROL PORT 3 (OUT 28)
CONTROL PORT 1 (IN 22)
SYSTEM BUS SELECT
FIFO
MMU CONTROL PORT 2 (OUT 22)
NETWORK CONTROL PORT
PIC
SCC
SYSTEM ADDRESS BUFFERS
SYSTEM COMMAND BUFFERS
SYSTEM BUS ARBITER
I/O
Speicher Zugriff
Control Data Bus
NSCC
05486



Abblock-Kondensatoren nicht gekennzeichnet

blocking capacitors are not marked

V-Version

Stecker/plug 1

1	67168	Brücken W19, W10 geändert	14.5.84	PB			
	4434	Freigabe	16.4.84		2	6891	Anpassung an PMU186CPX
Ind.	KM	Änderung	Dat	Name Ind	KM	Änderung	

Rauheit UN D 28 DIN ISO 1302 — Zul. Abweichung für Maße ohne Toleranzangabe: DIN 184, UN D 603

allgemeine Rauheit — Einheit mm — Werkstoff — Modell Nr.

Maßstab — Europ. Proj. — Benennung — Auftrags Nr.

CLASS

PRINT PMU 186 CPV

(PRINT PMU 186 CPX)

5112 291 95650

IND KM

Abblock - Kondensatoren nicht gekennzeichnet

blocking capacitors are not marked

V-Version

1. 6788	Brücken W49, W10 geändert	14.5.84	PB			
6884	Freigabe	16.4.84		2	6891	Anpassung an PMU186CPX
Ind. KM	Änderung	Dat.	Name/Ind.	KM		Änderung

Rauheit DIN ISO 1302 — Ersatz-Abweichung für Maße ohne Toleranzangabe: DIN 7184, UN-D 603

allgemeine Rauheit — Einheit: mm — Maßstab — Europ. Proj. — Blatt-Anzahl — Maßstab: — Auftrags-Nr.

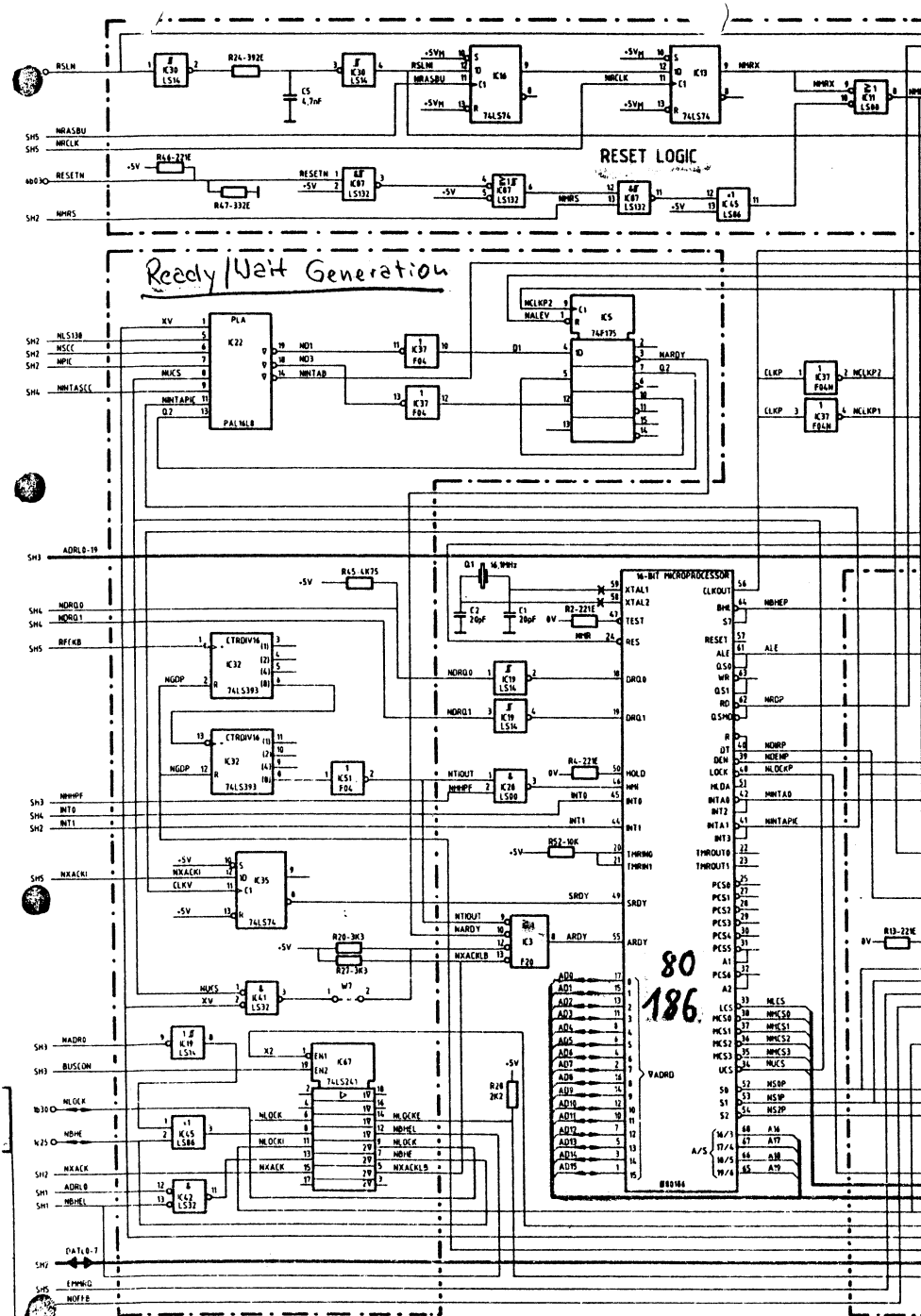
CLASS

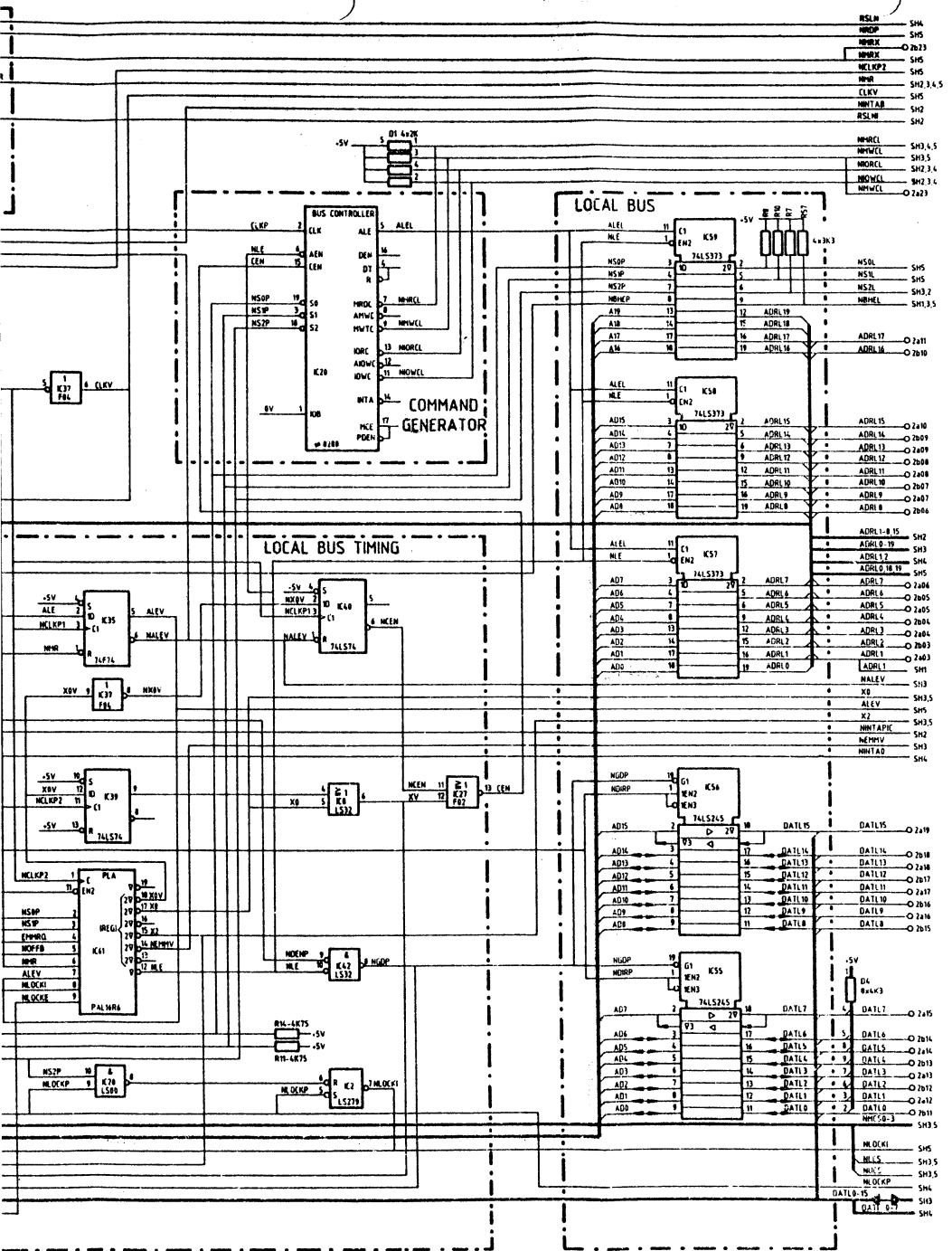
PRINT PMU 186 CPV

(PRINT PMU 186 CPX)

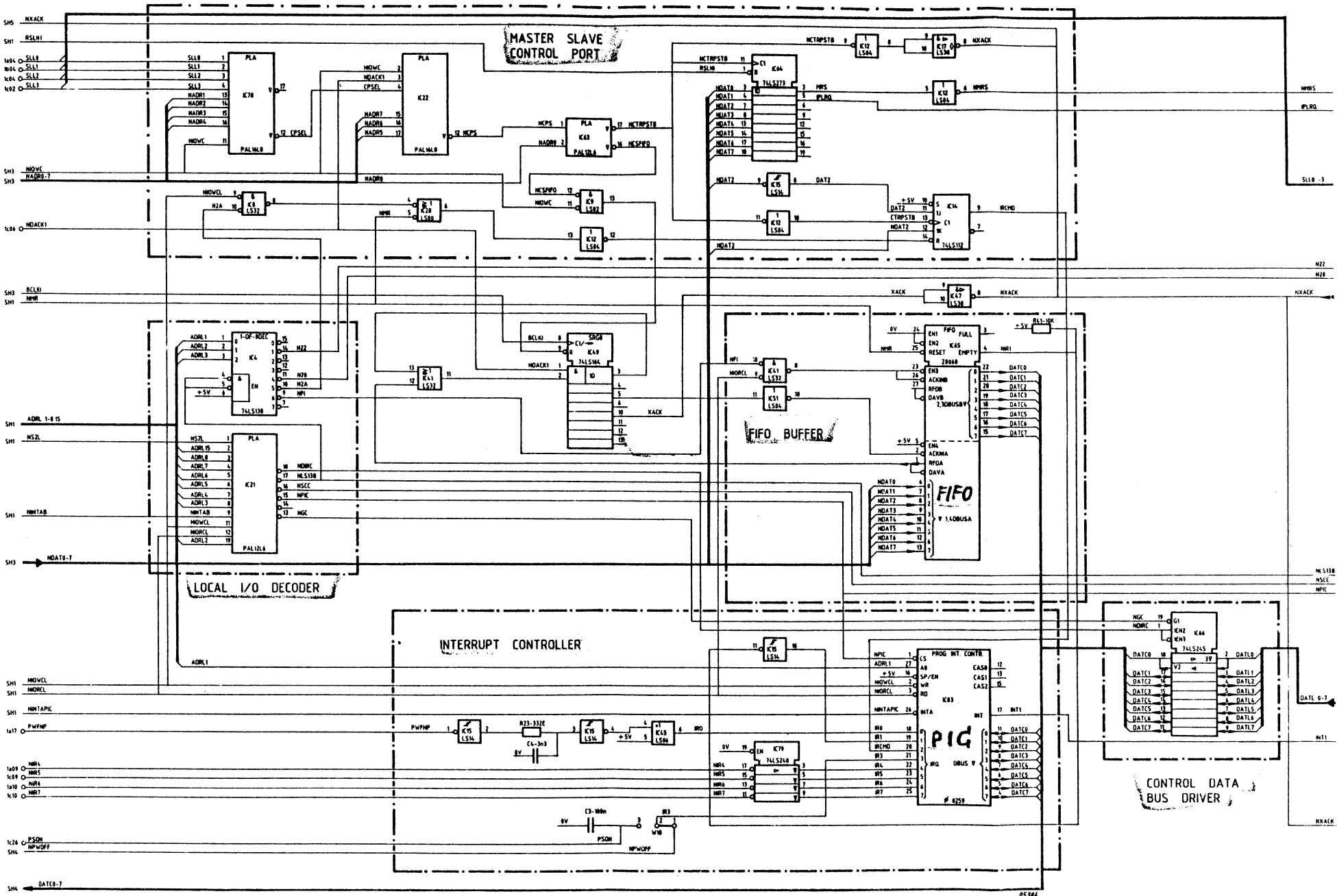
5112 291 95650

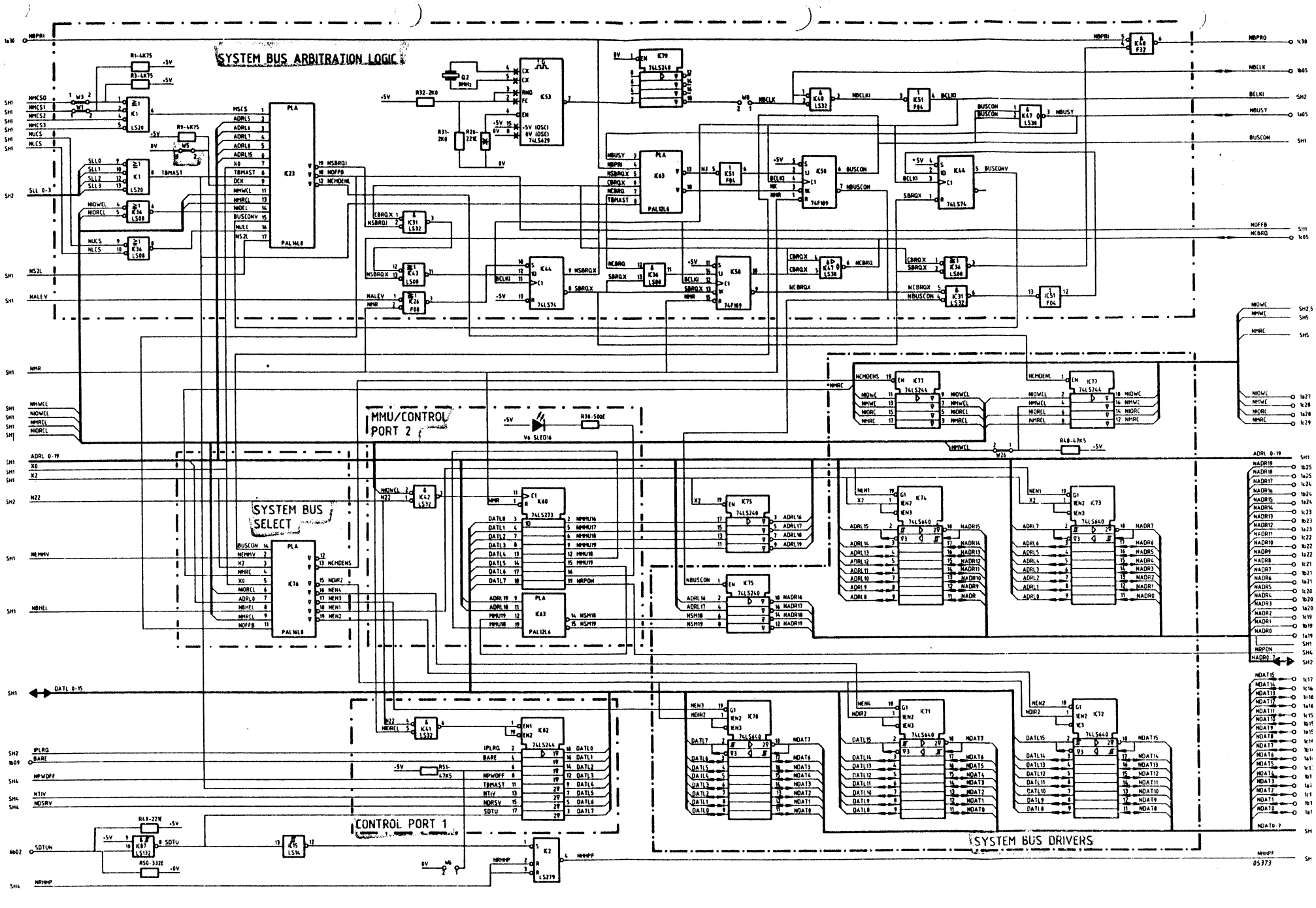
IND. KM


RESET LOGIC
Ready/Wait Generation
80
186

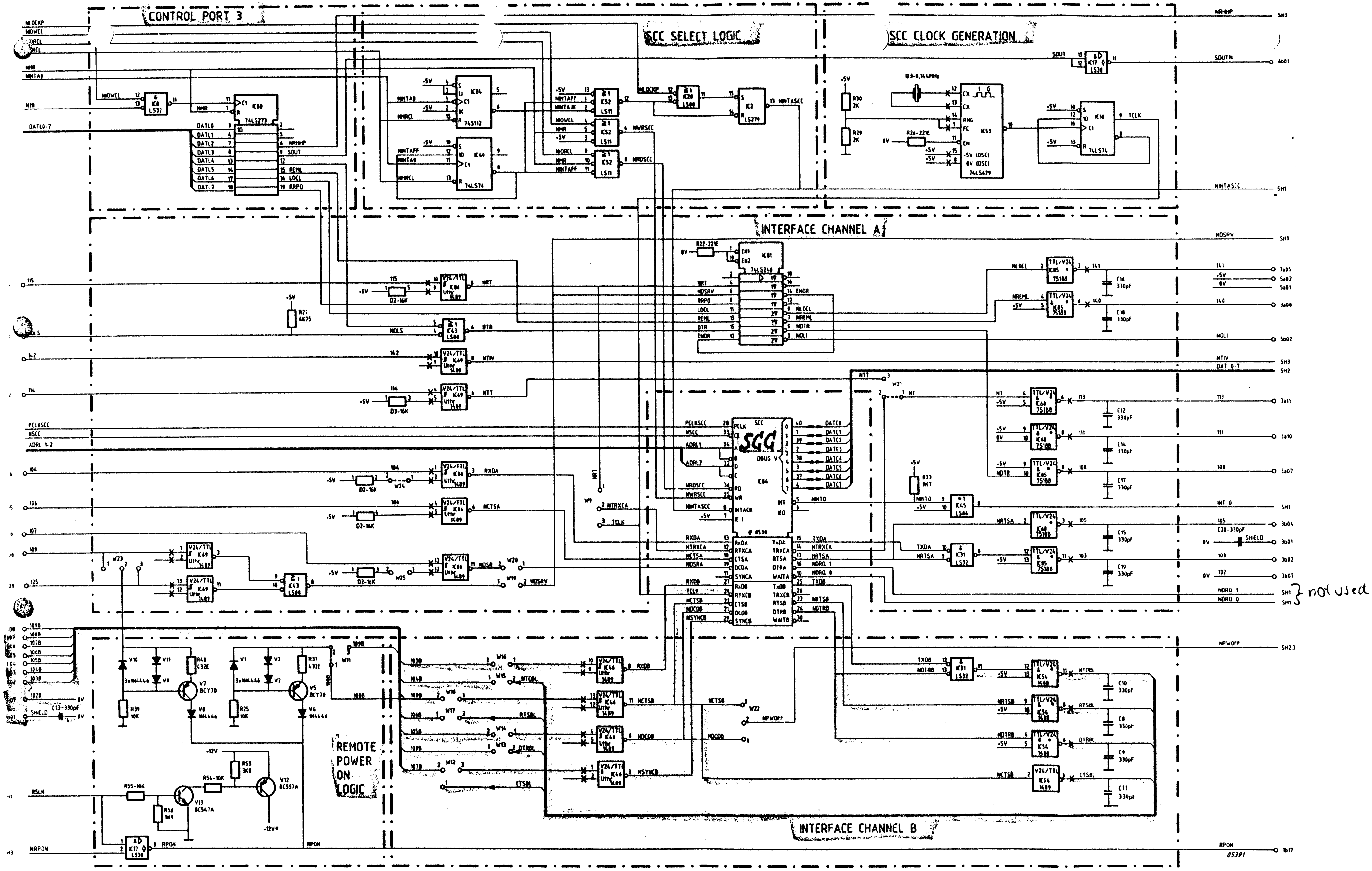

LOCAL BUS
BUS CONTROLLER
COMMAND GENERATOR
LOCAL BUS TIMING
IC20
IC59
IC58
IC57
IC56
IC55
IC35
IC40
IC39
IC41
IC42
IC0
IC27
IC70
IC2
PAL16R6
74LS373
74LS245
74LS74
74F74
LS32
LS279
LS00
05363

SHEET 1


MASTER SLAVE CONTROL PORT
FIFO BUFFER
LOCAL I/O DECODER
INTERRUPT CONTROLLER
CONTROL DATA BUS DRIVER
PLA
IC70
IC22
IC63
PAL16L8
PAL12L6
1-OF-8DEC
IC4
74LS138
SRG8
IC49
74LS164
FIFO
IC65
Z8060
2.30BUSB
1.40BUSA
PROG INT. CONTR.
IC83
8259
74LS273
74LS112
74LS240
74LS245
SHEET 2

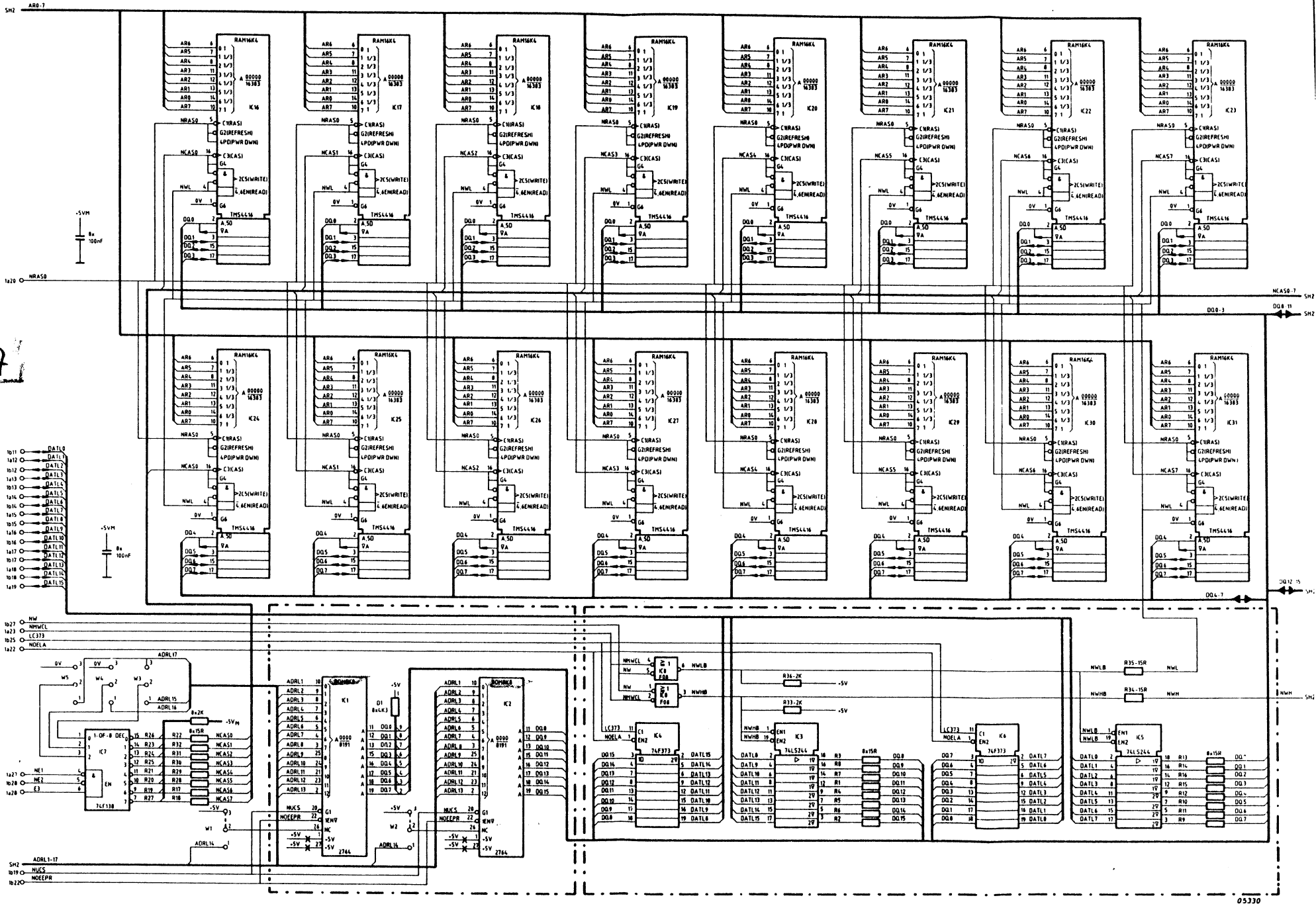

SYSTEM BUS ARBITRATION LOGIC
MMU/CONTROL PORT 2
SYSTEM BUS SELECT
CONTROL PORT 1
SYSTEM BUS DRIVERS
PLA
IC23
PAL16L8
IC16
IC63
PAL12L6
IC53
74LS629
IC79
74LS240
IC44
74LS74
IC50
74F109
IC74
IC73
IC72
IC71
IC70
74LS640
IC77
74LS244
IC75
74LS240
IC60
74LS273
IC62
74LS244
IC2
LS279
IC15
LS14
IC87
LS132
IC41
LS32
IC42
LS32
IC31
LS32
IC36
LS08
IC43
LS32
IC1
LS20
IC36
LS00
IC51
F04
IC49
F32
IC48
LS32
IC47
LS30
IC34
LS04
IC26
F00
R1-4K75
R3-4K75
R9-4K75
R49-221E
R50-332E
R51-47K5
R48-47K5
R30-500E
A32-2K0
R31-2K0
R26-221E
Q2
8MHz
V6 SLED16
W1
W3
W5
W6
W26
NBPRI
NBPRO
NBCLK
BCLKI
NBUSY
BUSCON
BUSCONV
NOFFB
NCBRQ
NMWCL
NIOWCL
NMRCL
NIORCL
NMR
NS2L
NALEV
NCMDENS
NCMDEMI
NSBRQI
SBRQX
CBRQX
NCBRQX
NBUSCON
TBMAST
SLL 0-3
NMCS0
NMCS1
NMCS2
NMCS3
NUCS
NLCS
MSCS
ADRL5
ADRL6
ADRL7
ADRL8
ADRL15
X0
DCK
NMWCL
NMRCL
NUCL
NS2L
BUSCONV
NMEMV
NBHEL
NOFFB
NCMDENS
NDIR2
NEN4
NEN3
NEN1
NEN2
NMRC
NIORC
NMWC
NMRC
ADRL 0-19
NADR19
NADR18
NADR17
NADR16
NADR15
NADR14
NADR13
NADR12
NADR11
NADR10
NADR9
NADR8
NADR7
NADR6
NADR5
NADR4
NADR3
NADR2
NADR1
NADR0
NADR0-7
NRPON
DATL 0-15
NDAT15
NDAT14
NDAT13
NDAT12
NDAT11
NDAT10
NDAT9
NDAT8
NDAT7
NDAT6
NDAT5
NDAT4
NDAT3
NDAT2
NDAT1
NDAT0
NDAT0-7
IPLRQ
BARE
NPWOFF
NTIV
NDSRV
SDTU
SDTUN
NRHHP
NHHPF
NBHEL
NMEMV
NSM18
NSM19
NMMU16
NMMU17
NMMU18
NMMU19
NMMU18
NMMU19
05373

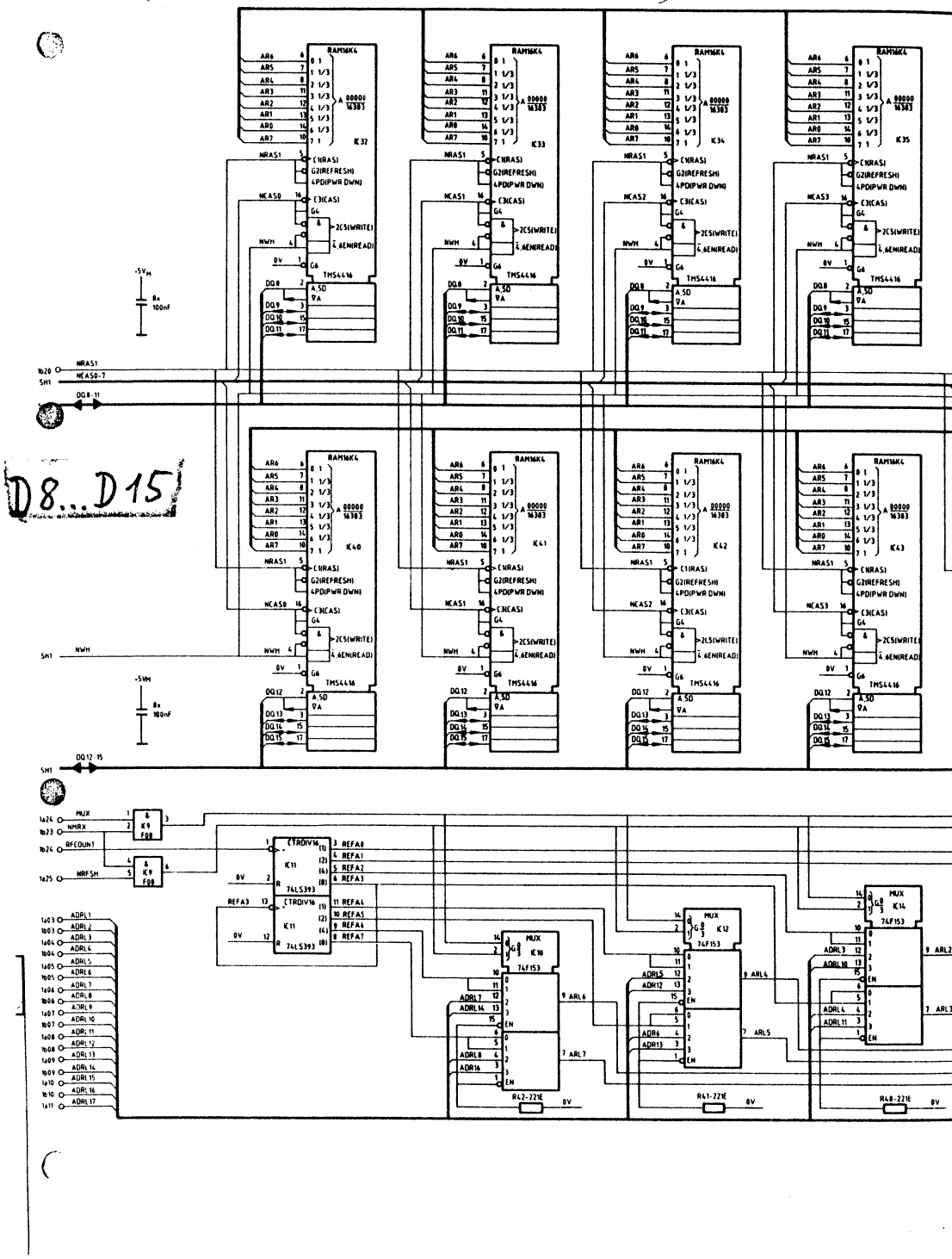
SHEET 3

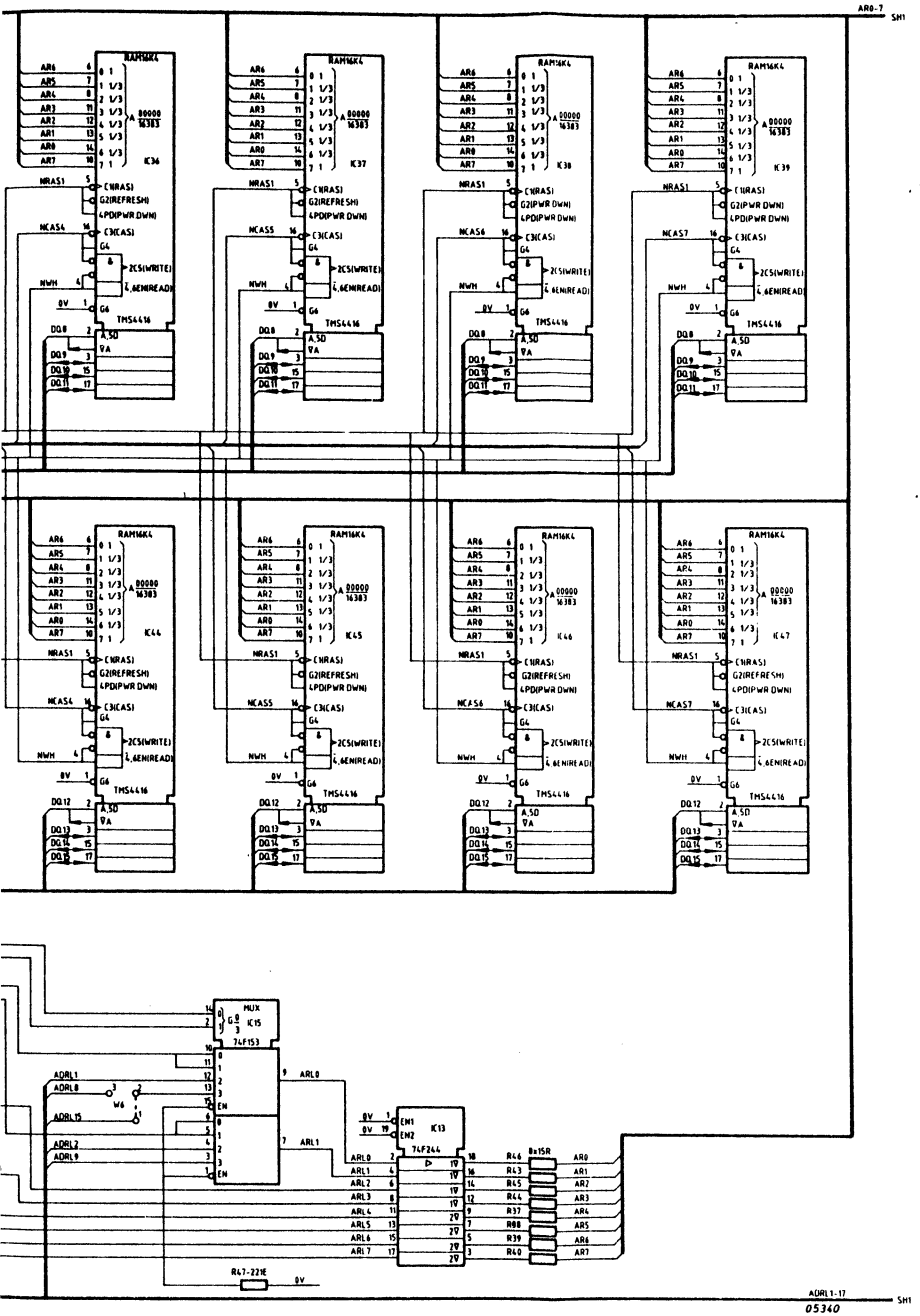


NOTE: CHIPS MARKED WITH * ARE CONNECTED TO +12V *

SHEET 4

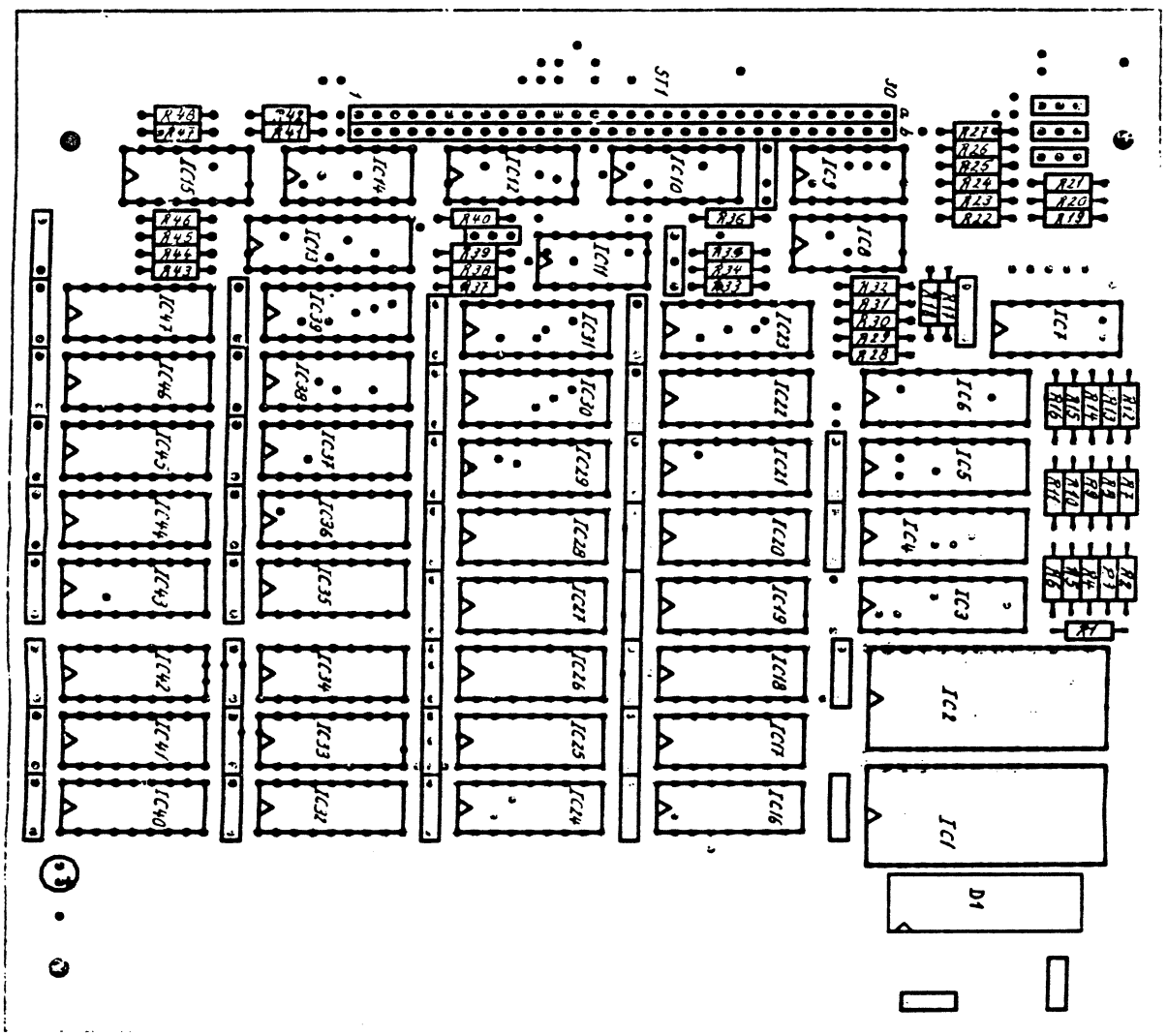

D0...D7
SHEET 1
05330


RAM16K4
IC32
IC33
IC34
IC35
IC40
IC41
IC42
IC43
TMS4416
NRAS1
NCAS0
NCAS2
NCAS3
NWM
DQ0-11
DQ12-15
SH1
MUX
NMRX
RFCOUNT
MRFSH
74LS393
74F153
ADRL1
ADRL2
ADRL3
ADRL4
ADRL5
ADRL6
ADRL7
ADRL8
ADRL9
ADRL10
ADRL11
ADRL12
ADRL13
ADRL14
ADRL15
ADRL16
ADRL17
ARL2
ARL3
ARL4
ARL5
ARL6
ARL7
R42-221E
R41-221E
R48-221E
D8...D15


AR0-7
SH1
RAM16K4
IC36
IC37
IC38
IC39
IC44
IC45
IC46
IC47
TMS4416
NRAS1
NCAS4
NCAS5
NCAS6
NCAS7
NWH
0V
DQ0
DQ1
DQ2
DQ3
(NRAS)
G2(REFRESH)
&PDI(PWR DWN)
C1(CAS)
C3(CAS)
G4
2CS(WRITE)
4,6EN(READ)
G6
A,5D
VA
MUX
IC15
74F153
ADRL1
ADRL8
ADRL15
ADRL2
ADRL9
W6
ARL0
ARL1
74F244
IC13
EN1
EN2
ARL0
ARL1
ARL2
ARL3
ARL4
ARL5
ARL6
ARL7
R46
R47-221E
8x15R
AR0
AR1
AR2
AR3
AR4
AR5
AR6
AR7
ADRL1-17
SH1
05340

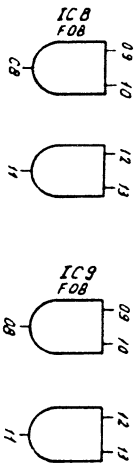
SHEET 2

PHILIP



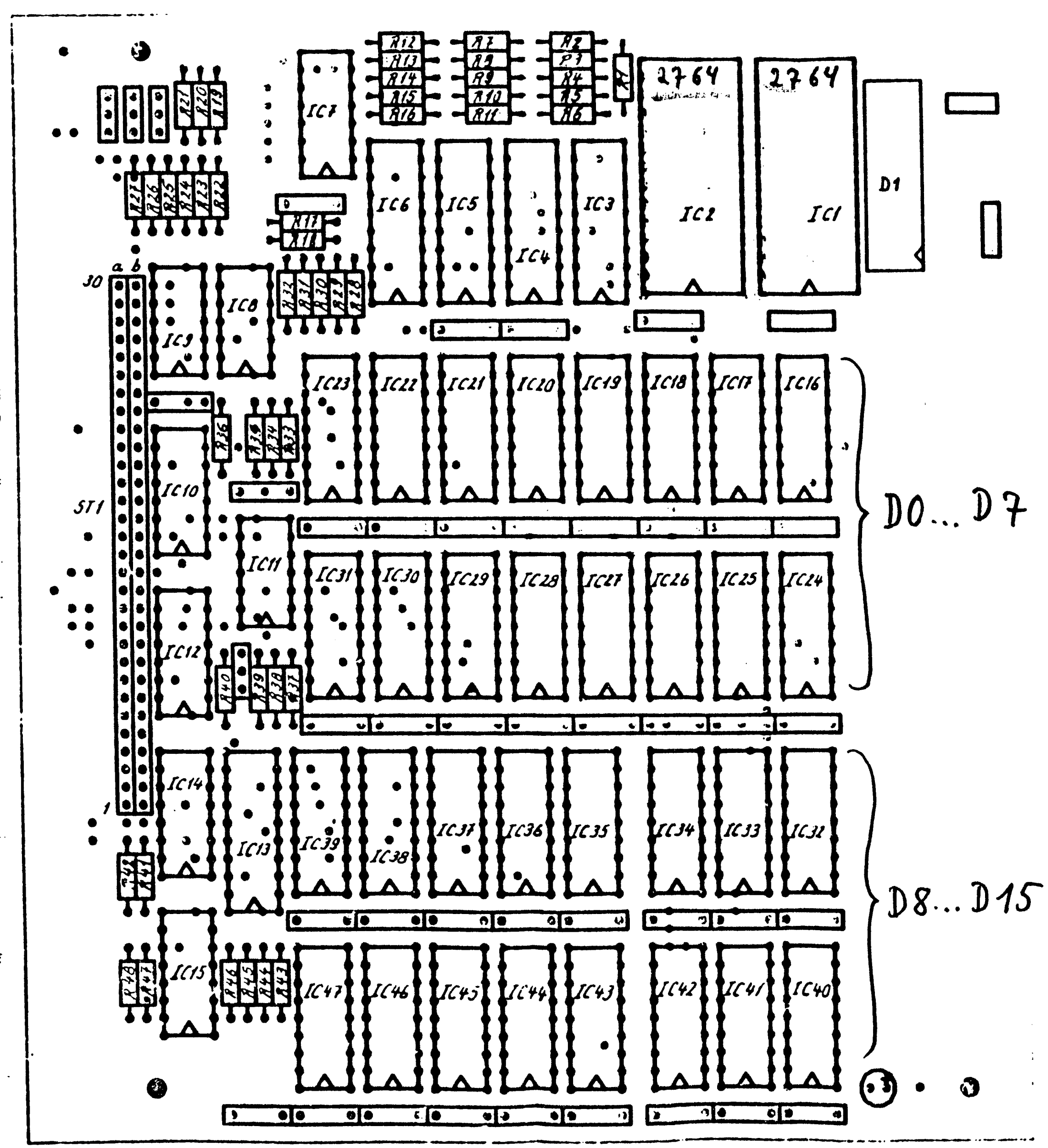
	a	b
30	0V	0V
29	+5V	+5V
28	E3	NE2
27	NE1	NW
26		
25	NRFSH	LC373
24	MUX	RFCOUNT
23	NMWCL	NMRX
22	NOELA	NOEEPR
21		
20	NRAS0	NRAS1
19	DATL15	NUCS
18	DATL13	DATL14
17	DATL11	DATL12
16	DATL9	DATL10
15	DATL7	DATL8
14	DATL5	DATL6
13	DATL3	DATL4
12	DATL1	DATL2
11	ADRL17	DATL0
10	ADRL15	ADRL16
9	ADRL13	ADRL14
8	ADRL11	ADRL12
7	ADRL9	ADRL10
6	ADRL7	ADRL8
5	ADRL5	ADRL6
4	ADRL3	ADRL4
3	ADRL1	ADRL2
2	+5VM	+5VM
1	0V	0V

Stecker / plug /

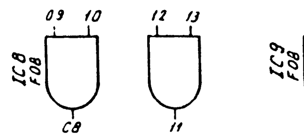


Freie Gatter / free gates

PRINT PMU186M-256K 5112 291 92620



Freie Gatter / free gates



Stecker / plug 1

Pin	a	b
30	0V	0V
29	+5V	+5V
28	E3	NE2
27	NE1	NH
26		
25	NRFSH	LC373
24	MUX	RFCOUNT
23	NMWCL	NMRX
22	NOELA	NOEEPR
21		
20	NRAS0	NRAS1
19	DATL15	NUCS
18	DATL13	DATL14
17	DATL11	DATL12
16	DATL9	DATL10
15	DATL7	DATL8
14	DATL5	DATL6
13	DATL3	DATL4
12	DATL1	DATL2
11	ADRL17	DATL0
10	ADRL15	ADRL16
9	ADRL13	ADRL14
8	ADRL11	ADRL12
7	ADRL9	ADRL10
6	ADRL7	ADRL8
5	ADRL5	ADRL6
4	ADRL3	ADRL4
3	ADRL1	ADRL2
2	+5VM	+5VM
1	0V	0V

Ind.	KM	Änderung	Dat	Name
1	5115	Brücken entfallen D1 hinzu	28.8.84	
	3868	Freigabe	13.1.84	

Rauheit DIN D 28 µm DIN ISO 1302

zul. Abweichung für Maße ohne Toleranzangabe

DIN 7184 UN D 603

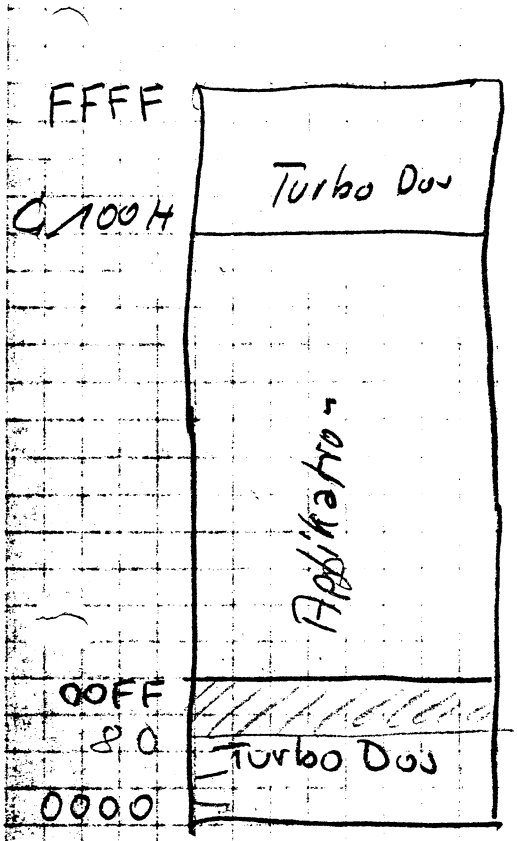
Allgemeine Rauheit | Einheit mm | Maßstab | Europ. Proj.

Modell-Nr | Auftrags-Nr

CLASS

PRINT PMU186M-256K 5112 291 92620

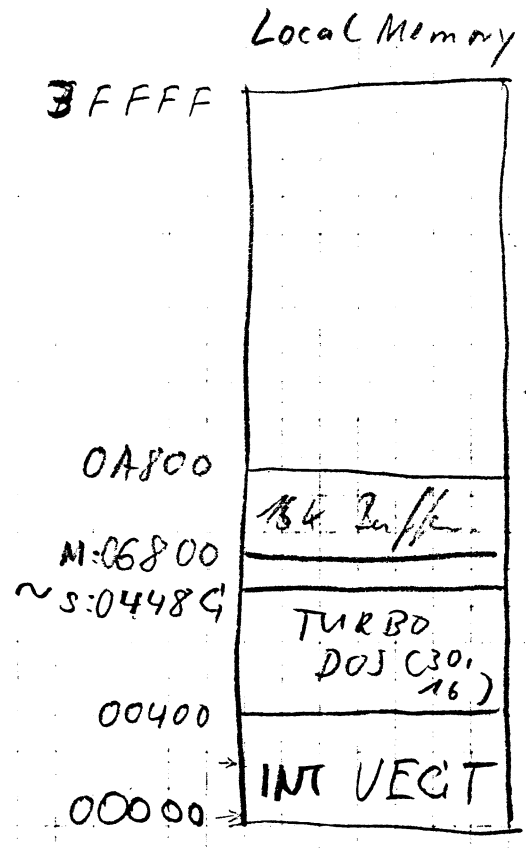
NAME G.H. 03.12.14



8 Bit

C laden

nach 5 sprung



je Vektor 4 Byte

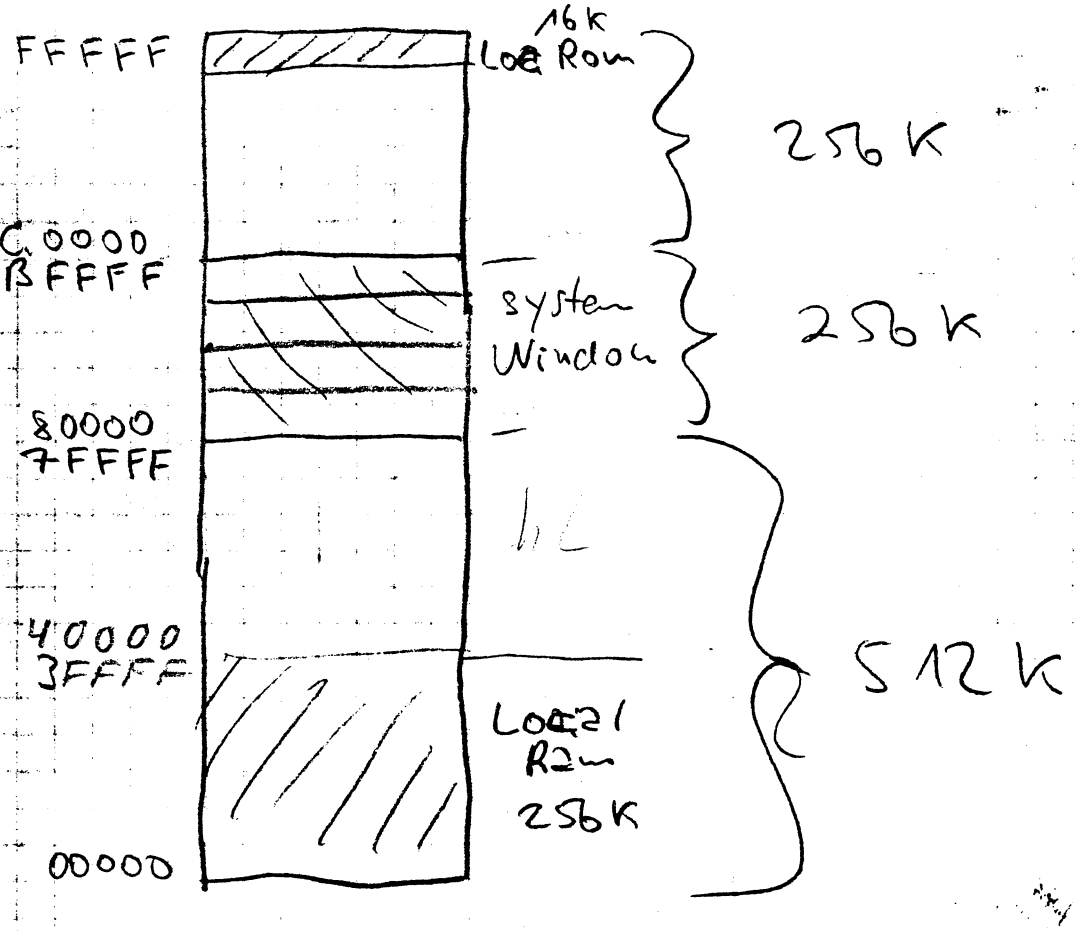
16 Bit

INT Typ

Adresse = Typ · 4

CD x

x = 0 ... FF



NLLS enablet Loc. Ram

NUCS - Loc. Rom

NMCS 0-3 256K Window

Beispiel: Error-LED auf PMU 186 ON

Aufrufen WS 186

TEST.A (NON DOC. FILE)

MODULE ␣ "TEST"

TAB LOC ␣ Code £
MOV AX, = 0X003F
MOV DX, = 0X0022
OUT DX, AX
RETF
END

TASM ␣ TEST

↓

TEST.O

↓

TLINK ␣ TEST

*

↓

TEST

↓

*

↓

Beispiel:

Einschreiben von einem in einen anderen Slave: (Slave 2 → Slave 1)

Kann auch 0 sein → 022,4F ← (muß immer F sein)

* 9000:0050 (2D) AA=55

In Adresse 0050 bei Slave 1 steht nun 55

If the first character of a signal name is "N", the signal is active low. All other signals are active high. The list is in alphanumeric order, the N in front off the signal name has no effect on the order of this list.

N22	I/O chip select address 22H (control ports 1, 2)
N28	I/O chip select address 28H (control port 3)
N2A	I/O chip select address 2AH (virtual port 4)
NA	memory access
A16-19	upper processor address lines
AD0-15	time-multiplexed address/data bus
NADR0-19	EMM-bus address lines
ADRL0-19	address-bus local
ALE	address latch enable (processor)
ALEL	address latch enable local
ALEV	address latch enable delayed
NALEV	
AR0-7	address/refresh bus on memory board
ARDY	asynchronous ready, processor input
NARDY	
ARL0-7	address/refresh local bus on memory board
NASYN	asynchronous (EMM) access to memory
BARE	battery back-up status
NBCLK	bus clock (EMM-bus)
BCLKI	bus clock internal (on this board, from EMM-bus)
NBCLKI	
NBHE	bus high enable (EMM-bus)
NBHEL	bus high enable local
NBHEP	bus high enable processor
NBPRI	bus priority in
NBPRO	bus priority out
BUSCON	EMM-bus controlled by this PMU
NBUSCON	
BUSCONV	EMM-bus controlled by this PMU (delayed)
NBUSY	EMM-bus busy
NCAS0-7	column address strobe lines (bank select)
NCBRQ	common bus request (on EMM-bus)
NCBRQX	common bus request external (on this PMU)
CBRQX	
NCEN	command enable
CEN	
CLKP	clock processor
NCLKP1,2	clock (inverted CLKP)
CLKV	clock delayed
NCMDENL	command enable local
NCMDENS	command enable system
COUNT1	indicates (with NRFSH) last clock cycle of a refresh cycle
CPSEL	I/O chip select for access by EMM-bus
CS186	memory chip select 80186
NCSFIFO	chip select FIFO for access by EMM-bus
CTRPSTB	control port strobe
NCTRPSTB	
NCTSA	V24 clear to send channel A
NCTSB	V24 clear to send channel B

CTSBL	clear to send channel B local
ND1	delay 1 (insert 1 wait state)
ND3	delay 3 (insert 3 wait states)
NDACK1	DMA acknowledge (always inactive)
DAT2	inverted EMM data line nr.2
DATC0-7	control data bus
NDCDB	data carrier detected channel B
DCK	memory mapping version (default: high, version B),
NDENP	data enable from processor
NDIR2	direction system data bus drivers
NDIRC	direction control data bus buffer
NDIRP	direction local data bus buffers
DQ0-15	data bus on memory board
NDRQ0,1	DMA request lines from SCC to DMA in 80186
NDSR	data set ready
NDSRA	data set ready channel A
NDSRV	data set ready (power on channel A, port 1)
DTR	data terminal ready (channel A)
NDTR	
NDTRB	data terminal ready channel B
DTRBL	data terminal ready local
NE1	enable bank select outputs (1)
NE2	enable bank select outputs (2)
E3	enable bank select outputs (3)
NEMMRQ	EMM request (access request from EMM-bus)
NEMMV	delayed X2, PMU accessed by EMM bus
NEN1	enable system data bus drivers
NEN2-4	enable system data bus drivers
ENDR	enable (?) data set ready
NFI	chip select FIFO for access by local processor
NGC	enable control data bus driver
NGDP	enable local data bus buffers
NHHPF	hand-held pannel (service processor) interrupt
INT0,1	interrupt request inputs integrated PIC
NINTA0	interrupt acknowledge integrated PIC, channel 0
NINTAB	interrupt acknowledge both (PIC and SCC)
NINTAFF	interrupt acknowledge from Flip-Flop
NINTAJK	interrupt acknowledge from JK flip-flop
NINTAPIC	interrupt acknowledge for PIC
NINTASCC	interrupt acknowledge for SCC
NIORC	I/O read command (EMM-bus)
NIORCL	I/O read command local
NIOWC	I/O write command (EMM-bus)
NIOWCL	I/O write command local
IPLRQ	initial program load request
IR0	interrupt 0 (power failure)
IR1	interrupt 1 (FIFO buffer not empty)
NIR1	
IR4-7	interrupts 4-7 (used by master only)
NIR4-7	interrupts 4-7
IRCMD	interrupt command (from networking control port)
NJ	set JK-flipflop to activate BUSCON
NK	reset JK-flipflop to deactivate BUSCON
LC373	clock data bus latches on memory board
NLCDR	latch clock (for access to) dynamic RAM
NLCP	latch clock (for access to) PROM
NLCS	lower memory chip select (from 80186)
NLE	enable local address latches

NLOCK	lock bus (EMM-bus)
NLOCKP	lock bus from processor
LOCL	local loop (testloop V24)
NLOCL	
NLS138	enable 74LS138 of local I/O decoder
NMCL	memory command local (read or write)
NMCS0-3	midrange memory chip select lines from 80186
NMMU16-19	local memory mapping bits
MMU18-19	system memory mapping bits from port 2
NMR	master reset, memory excluded
NMRC	memory read command (EMM-bus)
NMRCL	memory read command local
MRS	master reset, initiated by master
NMRS	
NMRX	master reset, memory included
MUX	select refresh or normal address
NMWC	memory write command (EMM-bus)
NMWCL	memory write command local
NOEEPR	output enable EPROM
NOELA	output enable memory data bus latches
NOLI	on-line indicator
NOLS	on-line switch
PCLKSCC	processor clock SCC
NPIC	chip select programmable int. controller
PSON	power supply on
PWFNP	power failure interrupt
NPWOFF	power off indication
Q2	2 wait states inserted
RAMRQ	external request to access RAM
RAS	row address strobe
NRAS0	row address strobe 0 (even byte addresses)
NRAS1	row address strobe 1 (odd byte addresses)
NRASBU	acivates row address strobe during reset (battery unit)
RASBU	
NRASPN	row address strobe enabled
NRCLK	refresh clock
RCLK	
NRDP	read (processor)
REFA0-7	refresh addresses
REML	remote loop (V24 test loop)
NREML	
RESETN	reset from service processor
NRFCK	refresh clock divided by 2
RFCK	
RFCKB	refresh clock, low during reset
RFCKS	refresh clock synchronized
RFCOUNT	refresh count
NRFCOUNT	
RFRQ	refresh request
NRFSH	refresh cycle executed
NRHHP	reset service processor interrupt
RPON	remote power on
NRPON	
RRPO	reset remote power on (not used)
RSLN	reset from EMM-bus during power on/off
RSLNI	reset during power on/off internal
NRT	receiver timing
NRTSA	ready to send channel A

NRTSB	ready to send channel B
RTSBL	ready to send channel B local
NRW	read/write command on EMM-bus
RXDA	received data channel A
RXDB	received data channel B
NS0L	status line 0 local
NS0P	status line 0 processor
NS1L	status line 1 local
NS1P	status line 1 processor
NS2L	status line 2 local
NS2P	status line 2 processor
NSBRQI	system bus request internal
SBRQX	system bus request external
NSBRQX	
NSCC	SCC chip select
SDTU	serial data from PMU to service processor
SDTUN	
SDUT	serial data from service processor to PMU
SDUTN	
SLL0-3	special logic lines, slot number (binary & inverted)
NSM18-19	upper system memory address lines (system mem. mapping)
SRDY	synchronous ready (processor input)
NSYNCB	synchronisation channel B
NT	timing (V24)
TBMAST	this board is master
TCLK	transfer clock
NTDBL	transmit data channel B local
NTIOUT	time out
NTIV	test indicator V24
NTRXCA	transfer clock channel A
NTT	transmitter timing (V24 channel A)
TXDA	transmitted data channel A
TXDB	transmitted data channel B
NUCS	upper memory chip select (80186)
NW	memory write enable
NWH	write signal to RAM, higher half of data bus
NWHB	write signal to memory, enable higher data bus buffer
NWL	write signal to RAM, lower half of data bus
NWLB	write signal to memory, enable lower data bus buffer
X0	low if local processor controls PMU
NX0V	delayed X0
X2	low if PMU is accessed by EMM-bus
NX2	
NXACK	transfer acknowledge on EMM-bus
XACK	transfer acknowledge (to EMM-bus from memory timing/FIFO)
NXACKAS	transfer acknowledge asynchronous
NXACKI	transfer acknowledge internal
NXACKLB	transfer acknowledge local bus (from EMM-bus)
X0V	delayed X0
XV	low if local processor controls PMU
Z	disable RAM access during refresh cycles

CONTENTS

AC Master ent ab Release 6

1 PROCESSOR

The processor on the PMU 186 is the Intel 80186, a 16-bit micro processor. It is capable of addressing 1Mb of memory. Four peripherals are integrated on the chip.

1.1 PROCESSOR CLOCK

The processor clock is generated internally, using an 16 MHz. crystal. This results in a 8 MHz. processor clock CLKP. This clock signal is inverted in two ports to create NCLKP1 and NCLKP2. NCLKP1 is inverted again to generate CLKV.

1.2 INTEGRATED PERIPHERALS.

The peripherals integrated in the 80186 are all used.
Pages 4-11 to 4-19 give further information on the addresses and the meaning of the register in the peripheral control block.

The Chip Select unit provides 6 memory chip-select signals :

- NUCS select upper memory (ROM)
- NMCS 3-0 select mid-range memory (system window)
- NLCS select lower memory (local RAM)

The integrated timer is used internally but not connected.

The Direct Memory Access Controller may receive a request from the SCC, controlling the V24 Interface. It is presently not used in the P3500/P3800.

The integrated Programmable Interrupt Controller is programmed to operate in Cascade mode, providing two interrupt inputs (INT0 and INT1) and two dedicated interrupt acknowledge outputs (NINTA0 and NINTAPIC).

SCC PIC

1.3 COMMAND GENERATOR

The command generator is used to decode the status-lines from the processor into four command signals (NMRCL, NMWCL, NIORCL, NIOWCL) and a signal ALEL to latch the address and status lines in the local bus latches.
The outputs of the command generator are enabled only when NLE is active, the command outputs may also be enabled by CEN.
(see also documentation)

1.4 READY / WAIT GENERATION

A bus cycle is ended when either SRDY or ARDY is activated.

SRDY is activated when NXACKI is activated (after synchronisation to the delayed processor clock). NXACKI is a signal from the memory timing and is generated in IC 24 (PAL 16R6) and is activated when:

X0=0 => PMU controls it's own board.
and NRASPN=0 => RAS lines are activated.
and CS186=1 => processor selects local RAM.
and NRFSH=1 => no refresh cycle running.
Conclusion : NARDY is the transfer acknowledge signal for an access to local RAM.

ARDY is activated when one of NTIOUT, NARDY or NXACKLB is activated.

NTIOUT is the output of an eight bit binary counter. This counter increments on every trailing edge of RFCKB as long as the counter is enabled. The counter will be enabled when NGDP, which is the enable signal for the local data bus drivers, is active. If the counter reaches the value 128, then NTIOUT is activated. This causes activation of ARDY and NMI. The activation of ARDY will end the current bus cycle and the NMI indicates that the bus cycle that was started has not been executed properly.

NARDY is synchronised to the processor clock and can only be activated when NALEV is inactive. If NALEV is active then NARDY is deactivated, this is done at the beginning of every bus cycle. Activation of NALEV depends on D1, the inverted signal ND1, that is generated in IC22 (PAL 16L8). ND1 is activated if during XV=0 either NUCS or Q2 is activated. This means that (because of the clocking of IC5) one wait state is inserted if the local ROM is accessed or if Q2 is activated. Q2 is activated two clock cycles after activation of ND3 and ND3 is activated if during XV=0 one of the following devices is selected :
- SCC or PIC, (either for a normal access or in an interrupt acknowledge cycle)
- all devices selected through IC4 (see Local I/O Decoder)
If one of these devices is accessed then 3 wait states will be inserted in the bus cycle.

Through W7 it is possible to eliminate the wait state that is inserted when the local ROM is accessed. If W7 is strapped then ARDY is activated immediatly, when both XV and NUCS are low.

NXACKLB is activated only when IC67 is enabled by BUSCON is active, indicating that this PMU has control over the EMM bus. NXACKLB is activated when NXACK is active. NXACK is a signal on the EMM-bus and may be activated either by this PMU or by a different PMU.
If this PMU accesses memory or the networking control port or the FIFO buffer on another PMU then NXACKLB is the acknowledge signal for this transfer.
NXACKLB may be activated in three ways :
1. In a memory access. If the RAM is accessed the signal XACK is activated and if at that moment X2 is low (indicating an access by the EMM-bus on this board) then NXACK is activated.
2. In an access to the networking control port. If a PMU accesses this port NXACK is immediatly activated, no wait states are inserted.
3. In an access to the FIFO buffer. The shift register will activate (5 bus clock cycles after the beginning of the access) the NXACKF signal and this will immediatly activate NXACK.

1.5 RESET LOGIC

The reset logic generates three signals, RSLNI, NMR and NMRX.
If NMR is active then the PMU is reset except for the memory refresh logic. NMR is activated if one of NMRX, RESETN or NMRS is activated.
NMRS is activated in the Master-Slave Control Port (Networking control port) by the master to give a selective reset of this PMU.
RESETN is a signal from the connector for the service processor, it allow's the service processor to reset the PMU.
NMRX is activated when RSLN (general system reset from EMM-bus during power-on/off) is active. RSLN is synchronised to NRASBU and NRCLK, both signals derived from the refresh timing. NMRX will reset the refresh logic and will also activate NMR. This means that activation of NMRX will reset the complete PMU, refresh logic included.
RSLNI has the same logic level as the RSLN line. It is used to reset the networking control port.
If RSLN is active, the power supply to the TTL/V24 drivers (+12V*), is switched off.

1.6 LOCAL BUS TIMING

The local bus timing generates two important signals:
X0 0 - local 80186 controls the PMU
X2 0 - PMU is accessed by EMM-bus

Other signals generated in this logic :
XV signal activ when X0 is activ, remains activ for one more clock-cycle.
NLOCKI - internal bus lock
NGDP - enable local address bus buffers
NLE - enable local address latches
- enable command generator
CEN - command enable for command generator

2 LOCAL BUFFERS

The local buffers are used to demultiplex the address and data lines from the processor.
Four bits of the buffers are used to latch the processor status signals and NBHEP (Bus high enable processor)

3 SYSTEM BUS DRIVERS

The system bus drivers allow access from the PMU onto the EMM-bus or from the EMM-bus to the PMU. The system bus drivers may be divided into three groups of bidirectional drivers for the address, data and control lines.
The drivers are controlled by signals from the system bus select logic, the system bus arbitration and the local bus timing.

3.1 SYSTEM ADDRESS-BUS DRIVERS

The system address bus drivers consists of two biderectional 8-bit buffers, that control the exchange of the 16 lower address lines, and two four bit buffers controlling the four upper address lines.
The 8-bit buffers are controlled by NEN1 and X2. NEN1 is the enable signal for the outputs of the buffers, X2 sets the direction of these buffers.
Because of the memory mapping mechanism, the upper four address lines are treated differently.
In an access of the PMU to the EMM bus ADRL 16 and 17 are placed on the EMM bus (NADR16/NADR17) and the lines NMM18/NMM19 are placed on the upper two address lines of the EMM-bus. This driver is enabled by NBUSCON.
If the access is from the EMM-bus to this PMU then the upper four address lines from the bus are replaced by the NMMU lines to create a physical address in memory that is accessable to the system. Activation of this buffer is controlled by the signal X2.

3.2 SYSTEM DATA-BUS DRIVERS

The data bus drivers are three 8-bit buffers that allow not only a direct connection of the data busses but also a connection of the lower half of the EMM data lines to/from the upper half of the local bus data lines. This allows communication between 16-bit and 8-bit PMU's.
The buffers are enbled by the signals NEN2, NEN3 and NEN4.
The direction off the buffers is set with the signal NDIR2.
The following scheme gives an overview of the data directions and the level off the controlling signals.

EMM data		local data	NDIR2	NEN2	NEN3	NEN4
0- 7	--->	0- 7	0	1	0	1
0- 7	<---	0- 7	1	1	0	1
8-15	--->	8-15	0	0	1	1
8-15	<---	8-15	1	0	1	1
0- 7	--->	8-15	0	1	1	0
0- 7	<---	8-15	1	1	1	0
0-15	--->	0-15	0	0	0	1
0-15	<---	0-15	1	0	0	1

3.3 SYSTEM CONTROL-BUS DRIVERS

The system control bus drivers are two 4-bit buffers. One buffer is used to allow command signals from the EMM-bus on the local command lines. This buffer is enabled when NCMDENS (command enable system) is activated. The other buffer is enabled if the PMU accesses a different PMU, the local command signals are then needed on the EMM-bus. This buffer is enabled if NCMDENL (command enable local) is active. The local memory write command is connected to this buffer via a strap (W26). If this strap is not installed it's not possible for this PMU to write data into the memory on other boards because this command line can not be activated.

3.4 SYSTEM BUS SELECT

The 80186 uses ADRL0 and BHE (bus high enable) to indicate the form of the data transfer.

transfer:	ADRL0:	NBHEL:
byte, even address	0	inactive
,, odd address	1	active
word, even address	0	active
,, odd address	two transfers:	-1st. byte at odd address
		-2nd. ,, at even address

These lines (ADRL0 and NBHEL) are, with other signals, used to generate the control signals for the system bus drivers. The generation of these signals is done in a PAL 16L8 (IC76). NEN1 is the enable signal for the system address-bus drivers and is activated when BUSCON=active or X2=low. BUSCON=active indicates that this PMU controls the EMM-bus, X2=low indicates that the PMU is accessed by the EMM-bus.

NEN2 is activated if ADRL0=0 and NBHEL is active but only when BUSCON=active or X2=low. This means that NEN2 is activated during a word transfer to or from the EMM-bus.

NEN3 is activated if ADRL0=0 and: BUSCON=active or X2=low. Conclusion: NEN3 is activated during the transfer off a byte or a word from an even address, either to or from the EMM-bus.

NEN4 is activated if ADRL0=1 and NBHEL=active but only when BUSCON=active or X2=low. NEN4 is activated during the transfer of a byte at an odd address, to or from the EMM-bus.
Bytes for an odd address are transferred via the upper half of the local data bus and via the lower half of the EMM data bus.

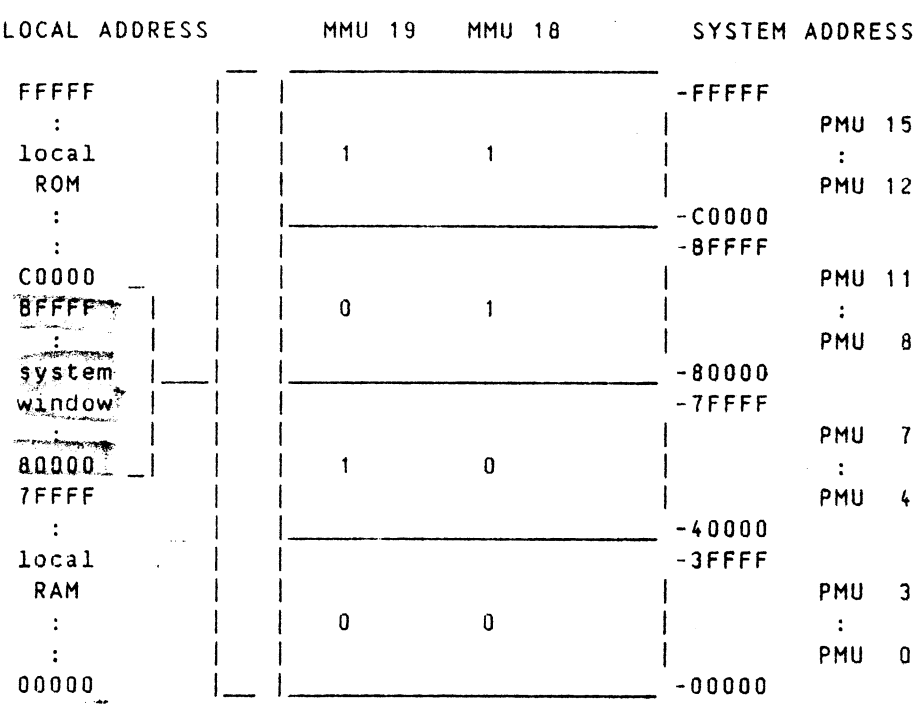
NDIR2 is activated during a memory or an I/O read command when BUSCON is active and NOFF8 is active. This signal is also activated when during a memory read command on the EMM-bus X2=low, indicating a bus cycle to read from the system memory.

NCMDENS is activated when X2=low, indicating an external access by the EMM-bus, or when NEMMV is active, which is a delayed X2 signal.

3.5 MEMORY MAPPING MECHANISM

3.5.1 MAPPING OF LOCAL ADDRESS SPACE TO SYSTEM MEMORY

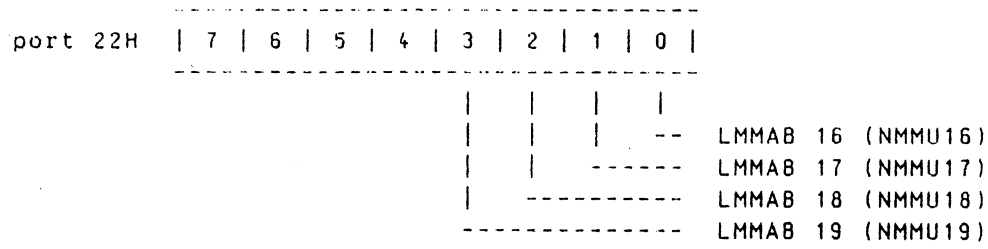
If the address on the local bus is within the system memory area (80000H-BFFFFH) the local address is translated into a system memory address. The upper two bits of the local address are replaced by two bits from the MMU/control port2. These two bits select a group of 4 addressable PMU's.
The replacement of the upper address lines is done in a PAL (IC63).



3.5.2 LOCAL MEMORY MAPPING

Each processor board has a page of 64 k8 in the system memory. The local address area of the PMU 186 is however 1 M8. By means of 4 bits of output port 22H the local processor can indicate on which part of the local memory the system memory page must be mapped.

Output



LMMA8 = LOCAL MEMORY MAP ADDRESS BIT

The four most significant bits of the system memory address, which hold the PMU number, are replaced on the accessed processor board by the lines LMMA8 19-16.
These lines are the most significant four local addresslines.

3.6 SYSTEM BUS ARBITRATION LOGIC

The PAL 16L8 (IC23) uses the following input signals.

MSCS - Activated if one of the mid-range memory chip-select signals is activated.

X0 - low if PMU controls it's own board.
high if PMU is accessed by a different PMU.

TBMAST - inactive (low) only if SLL0-3 are all high, indicating that the PMU nr. is 0 (MASTER).

DCK - depending on W5 selects memory mapping version, usually open and then DCK is high. Memory mapping version B is then selected.

NIOCL - activated if an I/O read or write command occurs

NULC - activated if upper or lower memory chip-select is activated.

BUSCONV - local processor has control over the EMM-bus (delayed)

ADRL5-8
ADRL15
NMWCL
NMRCL
NS2L

The PAL generates 3 output signals :

NSBRQI,
NCMDENL,
NOFFB.

NOFFB is activated only if X0=low when :
- The PMU accesses the system memory window,
- The PMU is master and tries to access I/O addresses 40H-FFH, which are the addresses of the system I/O area's part 1 and part 2.
- The PMU is not the master PMU and tries to access I/O addresses in 40H-5FH, which is the system I/O area part 1.
- The PMU accesses the reserved I/O space 100H-1FFH.
- Memory mapping version A is selected and the PMU does a memory access while the upper and lower memory chip select are both inactive.

Conclusion:
NOFFB is activated when the PMU accesses devices or memory on other boards.

NSBRQI is activated if NOFFB is active and X0 is low during active signals on NMWCL, on NMRCL or on NIOCL.

Conclusion:
NSBRQI is activated during activation of command lines if the PMU accesses other boards.

NCMDENL enables a buffer. If this signal is activated the local command signals of the PMU are admitted on the command lines of the EMM-bus.
NCMDENL is activated under the same conditions as NOFFB but without checking if the PMU is a master and only when BUSCONV is active (that is when the PMU is really connected to the EMM-bus).

If NSBRQI is activated then, if CBRQX is inactiv (PMU has not yet made a common bus request), a D-latch (IC41) is reset at the leading edge of the EMM-bus clock BCLKI. If the D-latch is reset then NSBRQX is activated and this will hold the D-latch in this state until it is set (when NALEV or NMR is active).
If SBRQX is activated when NCBRQ is inactive (no common bus request on the EMM-bus) then a JK-flipflop is set and CBRQX is activated As a result NCBRQ is activated, the PMU does a bus request. The JK-flipflop is reset when SBRQX is deactivated.

The BUSCON signal is generated using a JK flipflop which is controlled by the outputs NJ and NK of a PAL 12L6 (IC63). If NJ is activated then the flipflop is set and BUSCON is activated. NJ is activated when:

NBUSY=high, indicating that the bus is not being used by another PMU

and

NBPRI=low, indicating that no PMU with a higher priority is requesting control over the EMM-bus

If the PMU is the master-PMU then NJ is always activated when these conditions are met. If the PMU is not the master PMU then NJ is activated only if CBRQX (Common bus request to transfer) is activated.

If NK is activated then the flipflop is reset and then BUSCON is deactivated indicating that this PMU has no longer control over the bus. This happens when NCBRQ is activated, indicating a bus request, while CBRQX is inactive. This means that BUSCON is deactivated when a busrequest is pending that is not coming from this CPU.

NBPRO is activated either by a PMU with a higher priority then this PMU or by this PMU itself. If the signal NBPRI is high then the signal NBPRO will be high. If both CBRQX and SBRQX are active, indicating a bus request on this PMU, then NBPRO will be high, indicating PMU's with a lower priority that a higher priority PMU wants to control the EMM-bus.

3.6.1 EMM-BUS EXCHANGE CONTROL SIGNALS.

N8PRI - bus priority in
A low level indicates to the PMU that no PMU with a higher priority is requesting EMM-bus control. N8PRI is synchronised to the bus clock NBCLK.

N8PRO - bus priority out
Deactivated by a PMU when it requests the EMM-bus, indicating to a PMU with a lower priority that a higher priority bus request exists.

NCBRQ - common bus request.
Any PMU that wants control of the EMM-bus, but does not control it presently, can activate NCBRQ. If the signal is high it indicates to a PMU, acting as bus-master, that no other PMU is requesting the bus and therefor the present bus-master can retain the bus.

NBUSY - bus busy
This signal is activated by the PMU that is in control of the bus. It's monitored by other PMU's to determine the state of the bus.

NBUSY is activated (low) if BUSCON is high. BUSCON high indicates that the PMU is connected to the EMM-bus.
BUSCONV has the same function as BUSCON but it is delayed one 8CLKI-cycle

4 MASTER SLAVE CONTROL PORT

A PAL 16L8 (IC78) compares SLL0-3 (the slot-number of the PMU) to NADR1 4 to see if the I/O address on the EMM-bus is an I/O address that selects this board. The output signal CPSEL is activated during an I/O write command where SLL0-3 is equal to NADR1-4. (slot 0 - 40/41, slot 1 - 42/43, ...)
A second PAL 16L8 (IC22) activates the NCPS signal. NCPS is activated during an I/O write command from the EMM-bus to the Networking Control Port or to the FIFO buffer input.
It uses the CPSEL signal to see if the access-address is an address on this PMU. The EMM address lines NADR5-7 are checked to see if the address is in the range 40H-5FH, which are the I/O addresses for the Networking Control Port and the FIFO buffer.
CPSEL is not activated when NDACK1 is active. NDACK1 is an acknowledge signal from channel 1 of the DMA-controller on the SESCO and this channel is not used. Therefore NDACK1 is assumed to be always inactive (high). In a PAL 12L6 (IC63) the signals NCTRPSTB and NCSFIFO are generated.
NCTRPSTB is the select signal for the Networking Control Port and is activated when NCPS is active and NADR0 is high (even address).
NCSFIFO is a select signal for the FIFO buffer and is activated if NCPS is active and NADR0 is low (odd addresses).

4.1 SYSTEM ACCESS DECODER

The system access decoder compares SLL0-3 to the address on the EMM-bus (NADR16-19) and generates signal NEMMRQ. This signal is inverted and synchronised to the processor clock and this gives the signal EMMRQ.
NEMMRQ is activated when SLL0-3 are equal to NADRL16-19 but only during an active memory read or write command on the EMM-bus.
Conclusion:
EMMRQ is activated (high) during a memory access by the EMM-bus on this board.

4.2 NETWORKING CONTROL PORT

This port is selected by the signal NCTRPSTB. Only 3 bits of the 8-bit port are used. Bits 0 and 1 are latched in an 8-bit port, bit 2 is treated differently.

bit 0:
If this bit is set then MRS is activated. This immediatly activates NMRS and this signal will reset the 80186 on the board.

bit 1:
A 1 on this bit activates IPLRQ which is bit 0 of control port 1. This way the master PMU sends a IPL-request to the PMU186.

bit 2:
If this bit is 1 then an interrupt request is generated and send to the P.I.C. via the line IRCMD.

Bit 2 is latched in a JK-flipflop on the trailing edge of CTRPST8 (end of I/O write command from EMM-bus). The flipflop should be reset by the local 80186 at the beginning of the interrupt service routine for this interrupt request. This is done by writing to the virtual control port 4. This port doesn't use the data that's being written. The combination of the chip-select signal and the I/O write command line (N2A and NIOWCL) both active, will reset the flipflop.
The NMR signal is used to reset the port when the 80186 is being reset.
If NCTRPSTB is activated then NXACK is activated, which is the transfer acknowledge signal on the EMM-bus.

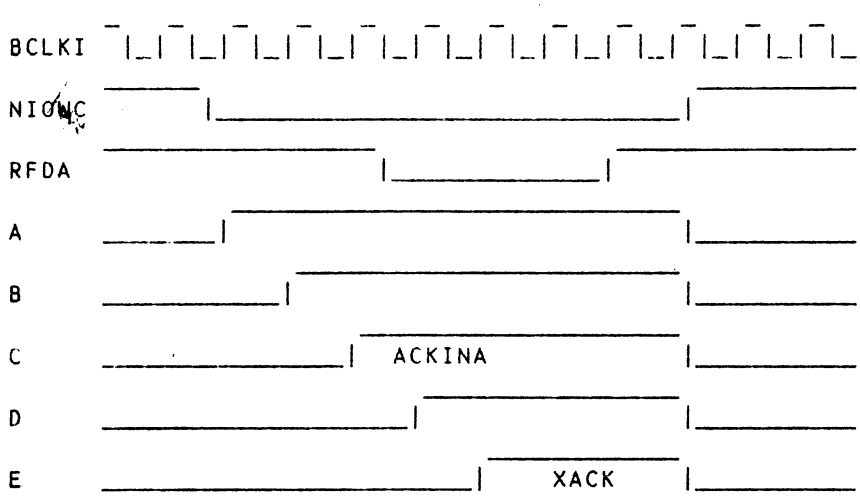
4.3 THE FIFO BUFFER

The signals used on the input of the FIFO-buffer are the input ACKINA and the output RFDA.

ACKIN = acknowledge input.
This line signals the FIFO that data on the input is valid if it is active (low).

RFDA = Ready For Data.
The signal is active high and signals that the FIFO is ready to receive new data.

A shift register is connected to the FIFO buffer. This buffer is reset until there is a write command to the FIFO buffer (both NCSFIFO and NIOWC are active).



If there is an I/O write command on the EMM-bus NIOWC is activated. If the FIFO is selected then the input of the shift register is activated and the first bit of the shift register will be 1.
After two EMM-bus clock cycles the 1 is shifted into bit 3. Then the ACKINA input of the FIFO is activated and the data on the data-bus is read by the FIFO. As a result the RFDA signal goes inactiv.
After another two bus-clock cycles the XACK is activated indicating the PMU that controls the EMM-bus that the transfer is finished (no more wait states) That PMU will then deactivate the NIOWC command and the shift register is cleared.

If the FIFO buffer receives a byte the signal EMPTY is deactivated which generates an interrupt request, via IR1,to the P.I.C.. The 80186 can then read the FIFO in the interrupt service routine.

5 LOCAL I/O DECODER

The local decoder consists of a PAL 12L6 (IC21) and a 1-of-8 decoder.
The PAL either directly selects one of the I/O devices or it enables the decoder.

Directly selected devices :
P.I.C. (addresses 08H-0BH) - through signal : NPIC
S.C.C. (addresses 00H-07H) - through signal : NSCC

The LS138 signal is activated in the I/O address range 20H-2FH. In this range the decoder may select one of the following addresses :

address 22 : Control port 1 (input)
address 22 : Control port 2 (output)
address 28 : Control port 3 (output)
address 2A : Control port 4 (virtual output)
address 2C : FIFO (input)

The PAL also provides two signals for the Control Data Bus Driver :

NGC - Gate clock for transceiver latches.
NDIR - Direction for transceiver.

NDIRC is activated during I/O read commands in the address ranges : 00H-0FH, 2CH-2FH.
NGC is activated during any access in these I/O areas.
Because these signal should also be activated during interrupt acknowledge cycles, the signal NINTAB is used to indicate an interrupt acknowledge to the SCC or PIC.

The PAL outputs are only active during NS2L is active (low), NS2L indicates that the current bus-cycle is :

Interrupt acknowledge
Read/Write I/O
Halt

6 CONTROL DATA BUS DRIVER

The control data bus driver is a biderectional buffer between the local data bus and the control data bus. The control data bus is used to access the FIFO-buffer, the SCC and the PIC. The control signals for the buffer are generated in the local I/O decoder.

7 PROGRAMMABLE INTERRUPT CONTROLLER

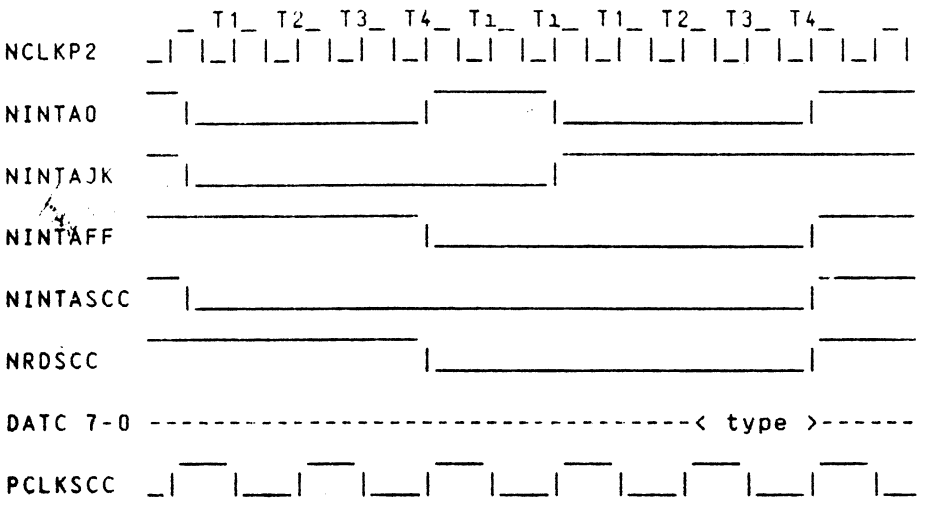
The P.I.C. is selected by NPIC. ADRL1 is used to select one of the internal registers in the controller. NIOWCL and NIORCL are used for the normal I/O operations. NINTAPIC is the interrupt acknowledge signal coming from the integrated int. controller on the 80186. The interrupt lines coming in on the P.I.C. are :

IR0	-	activated when PWFNP is activated. Indicates a power failure.
IR1	-	activated when the FIFO buffer is not empty.
IRCMD	-	interrupt command from master through control port 4.
IR3	-	activated by PSON or NPWOFF, depending on the setting of strap W10.
IR4-7	-	interrupt requests from EMM bus (NIR4-7).

8 SCC / V24 INTERFACE

Because the Zilog SCC interface to a processor is different from the Intel 80186 signals, some extra logic is needed.
To reset the SCC both the read and write signals for the SCC should be activated. The select logic will activate both NRDSCC and NWRSCC when NMR is activated.
The 80186 runs two interrupt acknowledge cycles but the SCC expects only one cycle. Also the 80186 doesn't activate the I/O-read command during the interrupt acknowledge cycles. These problems are also solved in the SCC select logic.

timing:



The V24 circuits may control the remote power on logic. Depending on the strap-setting the remote power on logic is controlled by channel A or channel B. Activation of the V24 lines will activate RPON and the power-supply is switched on. RPON is deactivated when NRPON is active, the PSU is then switched of. During reset (RSLN is active) the signal RPON may not be activated by activation of NRPON.
A circuit is provided to switch of the power to the V24 drivers during power on/off to prevent generation of unwanted characters.

9 CONTROL PORTS

An overview of the control ports is given in the HSI-manual, page 4-31.

10 MEMORY INTERFACE

10.1 MEMORY BUS SELECT

The memory bus select controls the data and address buffers on the memory board. It consists of a PAL 12L6 (IC62) that generates 5 signals.

NOELA is used to enable the outputs of the latches for data from the memory board. It is activated during a read cycle from the memory, initiated either by the local processor (ROM or RAM) or by the EMM-bus (RAM-access).

NLCP is activated when the local processor reads from ROM. If NLCP is active then LC373 is activated and this signal is used as a strobe for the data latches (data fromm memory to PMU).

NOEEPR is activated under the same conditions as NLCDR, it is used to enable the ouptuts of the EPROM chips.

NASYN is activated when X2=low (indicating an access by the EMM-bus) and ADRL18 and ADRL19 are low. This means that NASYN is activated during an EMM-bus access to the lower 256K of the local memory. The signal is used in the memory timing.

NA is used together with Z, a signal from the memory timing. The data buffers on the memory board, used for data from the PMU to the memory, are enabled when NMWCL or NW is activated. NW is active when both Z=high and NA=high. Z=high is an indication that no refresh cycle is running. NA is high when the local processor controls the PMU and is executing a write cycle (derived from status lines).

10.2 MEMORY TIMING

The memory timing provides the RAS and CAS signals for the dynamic RAM and the acknowledge signals to the processor and the EMM-bus. Two important lines in this logic are NRFSH and NRASPN. NRFSH is activated during a refresh cycle and NRASPN is a signal that allows activation of the RAS-lines to the memory board. The RAS-lines NRAS0 and NRAS1 are activated only when NRASPN is active, during a refresh both RAS lines will be activ to refresh both parts of the memory. During a normal memory access the activation of the RAS-lines depends on N8HEL and ADRL0, to select the right part of the memory (byte/word access, odd/even byte). NRASPN will also activate MUX, E3 and NE1. MUX is the inverted NRASPN signal and it is delayed for 100 nsec. E3 is the same signal but with a delay of 200 nsec. NE1 and E3 are used to enable the bank select (CAS-lines). NE2 is high during a reset and during refresh cycles and is used to disable the bank select in these situations.

Refresh cycles are started on a refresh request. This request is made via a D-latch that is clocked on the leading edge of RFCKS, a signal derived from the refresh clock. At the end of a refresh cycle COUNT1 will be low, indicating the end of the cycle. If both NRFSH and COUNT1 are low, the D-latch for the refresh request will then be reset.

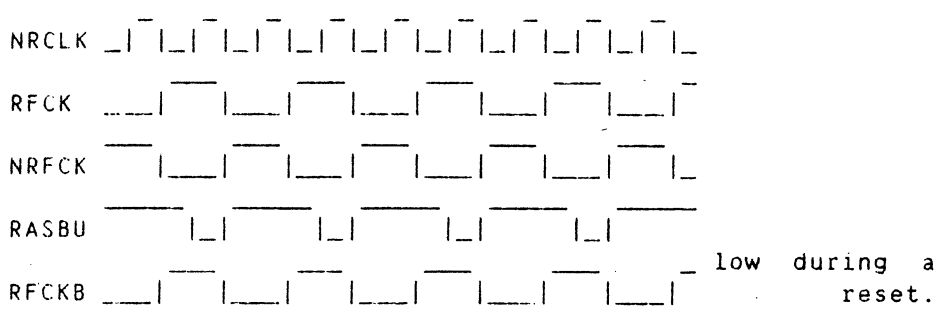
The signal NASYN, created in the memory bus select PAL is used to indicate the memory timing logic that the EMM-bus wants to access the memory. Activation of NASYN will set a D-latch, synchronised to the processor clock. This will activate RAMRQ and if NX2 is high, indicating an external access to this PMU, the input of the PAL is activated. The D-latch is reset when the read or write command is deactivated again.

The transfer acknowledge to the EMM-bus is derived from the signal NXACKAS, an output of the PAL. Activation of NXACKAS will set a D-latch (IC39) and this activates the signal XACK. If XACK is active and NX2 is high then the acknowledge to the EMM-bus is activated.

10.2.1 REFRESH CLOCK

The refresh clock generates :

NRCLK refresh clock
RFCK ,, ,, divided by 2
NRFCK



low during a reset.

RFCOUNT is the signal that increments the refresh counter. During reset, RFCOUNT is logically identical to the RASBU signal. During normal operation RFCOUNT has the same level as the RFRQ signal

RFCKB is derived from NRFCK, it's the inverted NRFCK signal during normal operation and always low during reset.

RFCKS is derived from RFCKB by synchronizing with the processor clock (NCLKP2) and then delaying it for one NCLKP2-cycle.

RFRQ is activated on the rising edge of RFCKS and is deactivated when :

the processor is being reset.
or: if NRFRSH=activated and COUNT1=low

This means that RFRQ is continuously being activated, and is reset if a refresh-cycle is started and count1=low.

11 LOCK-SIGNALS

NLOCP is the signal from the 80186 indicating that the instruction that the 80186 is executing may not be interrupted by an access from the EMM-bus.
The signal is latched to generate NLOCKI, which will remain activated throughout the execution of a whole buscycle.
If the PMU accesses the EMM-bus then NLOCK on the EMM-bus will be activated when NLOCKI is active.
If the PMU is accessed by the EMM-bus and NLOCK is activated by the PMU controlling the EMM-bus then NLOCKE will be activated. This causes X2 to remain low when it is accessed by the EMM-bus, indicating that the PMU is accessed by the EMM-bus. As a result the 80186 is not able to run a local bus-cycle.

12 INTERFACE TO POWER SUPPLY.

RPON is a line on the EMM bus that switches on the PSU if it is high. The PSU is switched off if RPON is low. RPON may be activated in two ways :

1. Via V24 channel A:
   depending on the setting of strap W23:
   - circuit 125 (ring indicator)
   - circuit 109 (data carrier detected)

2. Via V24 channel B:
   depending on the setting of strap W1:
   - circuit 108 (data terminal ready)
   - circuit 109

Suppose the PSU is switched off. If one of the V24 circuits is activated, the voltage on that line will be +12V and this will activate RPON. The PSU is then switched on and PSON will remain high because of the pull-up resistors on the EMM-bus.
If the device connected to the V24 interface is switched off, the signal NPWOFF is activated. This is done either via NCTSB (clear to send) or via NDCDB (data terminal ready) If NPWOFF is activated an interrupt is generated via the PIC and bit3 is reset in control port 1.

If the PMU is master it will look if all the PMU's are ready. If they are, then the master will switch off the PSU via control port 2. If bit7 of this port is set then NRPON will be high and via a port (IC17) RPON will be pulled to ground. This will switch off the PSU.

The port (IC17) is used to prevent deactivation of RPON during reset. RPON is always active when the reset signal RSLN is low.

13 SERVICE PROCESSOR FACILITIES

The service processor is an instrument to test the PMU186. A special connector on the board provides connections to 4 lines on the PMU :

- ground.
- SDUTN
- SDTUN
- RESETN

SDUTN allows serial data transfer from the PMU to the service processor. It is the inverted output of bit3 in control port 3.

SDTUN has two functions:
Activation of SDTUN will activate SDTU, which is bit 7 of control port 1. Also if NRHHP is inactive, activation of SDTUN will set a latch which causes a non-maskable interrupt in the 80186. NRHHP is bit 2 of control port 3. If this line is activated the latch will be reset and will remain reset, independent of SDTUN.

RESETN causes activation of NMR and this signal resets the PMU (except for memory refresh logic).

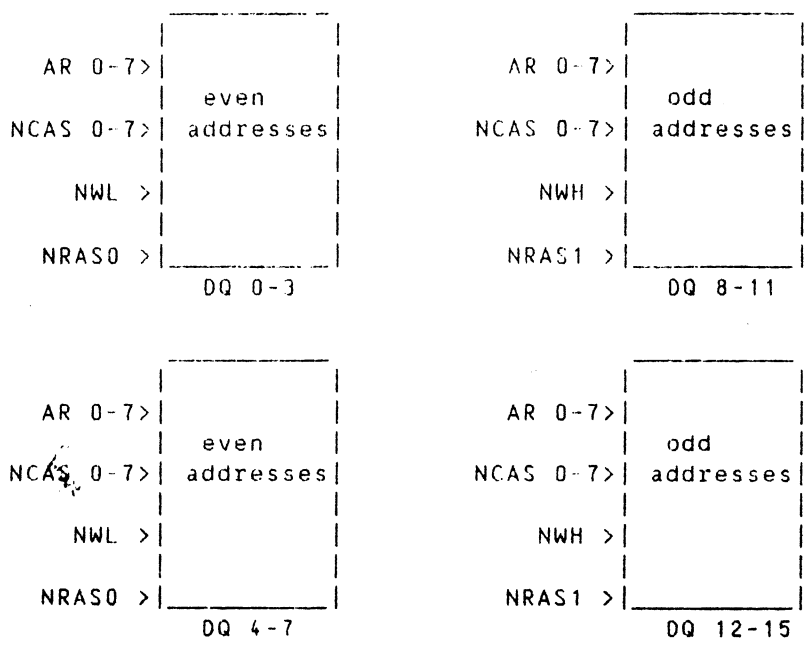
14 MEMORY BOARD

14.1 ROM

Two EPROM's are connected parallel, forming a word oriented ROM. The chips are selected when NUCS is activated. To enable the outputs of the EPROM's the signal NOEEPR should be activated.
Straps W1 and W2 are provided to allow installation of 16K8 EPROM's.

14.2 DYNAMIC RAM

The 256K8 dynamic RAM on the memory board is byte organised and can be word-accessed. The chips are divided into 4 banks



14.3 DATA BUFFERS

The data lines on the memory board (DQ15-0) are connected to a buffer and a latch.
In a read operation the data from memory is latched in two 8-bit latches when LC373 is activated. The outputs of these latches are enabled when NOELA is active.
In a write operation the data on the local data-bus is buffered to the lines DQ15-0. The outputs of the two 8-bit buffers are enabled when NW or NMWCL is active.

14.4 COLUMN ADRESS STROBE

The column address strobe signals NCAS7-0 are derived from the address lines ADRL 17-15. Straps W3,W4 and W5 are used to adapt the generation of the NCAS lines to the memory capacity that is installed at the memory board.
The outputs of this decoder are enabled when NE1,NE2 and E3 are all active.

14.5 REFRESH COUNTER

The refresh counter is incremented every time RFCOUNT is deactivated. The outputs of the 8-bit counter are used to select a row address during refresh cycles (REF7-0).

14.6 ADDRESS MULTIPLEXERS

The multiplexers on the M-board must select a refresh address.
If NMRX is low (active), the processor is reset. The multiplexers will then select a refresh address.
Further selection :

MUX	NRFSH	selected :
0	0	refresh address
1	0	refresh address
0	1	row address
1	1	column address

NRFSH selects between refresh or row/column address,
MUX " " row or column address

During normal operation NRFSH should be active (low) to select the refresh address.