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TITLE: Processing Memory Unit 80 (PMU 80)

Maintenance: M. Ginsberg

Department: System Development

Date: 82-07-13

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FM VOL: 1012 Processing Memory Unit 80 (PMU 80) CHAPTER: 11 RELEASE AND CHANGE DOCUMENT SECTION: SUBSECT:		Document number SOF. SF **L** Distribution Confidential
Change Order	Originator: A. van Hoevelaken Date: 82.12.20	Registration number: 82.167

TITLE: Change Order for FM VOL 1012

DESCRIPTION: see Configuration Index SOF. SF 24460 to 24464

REASON: Correction of two page numbers :

10.3.1/39.1 to 10.3.2/1 and
10.3.1/39.2 to 10.3.2/1.1

COMMENTS:

Andere
S. 10.3.1/27
10.3.1/8
10.3.1/30
133
139

Cf. van Hoevelaken

Prep. by:			FMV 1012
Supersedes doc. no. SOF. SF	L		Date 821220 Page

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FM VOL: 1012 Processing Memory Unit 80 (PMU 80) CHAPTER: 11 RELEASE AND CHANGE DOCUMENT SECTION: SUBSECT:		Document number: SOF. SF L Distribution: Confidential
Change Order	Originator: A. van Hoevelaken Date: 82-12-09	Registration number: 82.159

TITLE: Change order for FMV 1012

DESCRIPTION: see Configuration Index SOF.SF 24187 to 24213

REASON: Acceptance of Change Proposal 82.137 by the 4th SyCB/P3000 Meeting

COMMENTS:

A. van Hoevelaken

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Eck, R. van	P&P
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1. Scope

This document specifies the hardware of the 8 bit Processor Memory Unit (PMU-80) to be used e.g. within P3500 system.

The design shall be based on a Z80-A microprocessor.

The PMU-80 shall be able fo fulfill all functions required by the operating system "TurboDOS" *), e.g. it shall be able to act as "master" as well as "slave" and shall provide the following facilities:

- o an 8 bit wide local bus usable for autonomous internal operations
- o an 8 bit wide EMM-bus compatible interface,
- o an 64KB dual port RAM
- o an 4KB (8KB) (P)ROM
- o one serial interface to provide the connection of a V.24 Data Terminal Equipment (DTE) (R/6/)
- o one serial interface to provide the connection of a V.24 Data Circuit-Terminating Equipment (DCE) (R/6/)

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2. Applicable Documents

R/0/ System Specification P3500

R/1/ HPF Vol. 2108
EMM-System Bus Specification, ch. 10 EPS

R/2/ DSS Vol. 8, Standard 4
Short Distance Interface, ch. 10 EPS

R/3/ HPF Vol. 2138
PSU-WS 120, ch. 10 EPS

R/4/ HPF Vol. 2125
Flexible Disk Controller 5"/8" (FLEXCO) ch. 10 EPS

R/5/ ZILOG 1981 Data Book

R/6/ CCITT Yellow Book, Vol. VIII Fascicle VIII.1

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3. Requirements

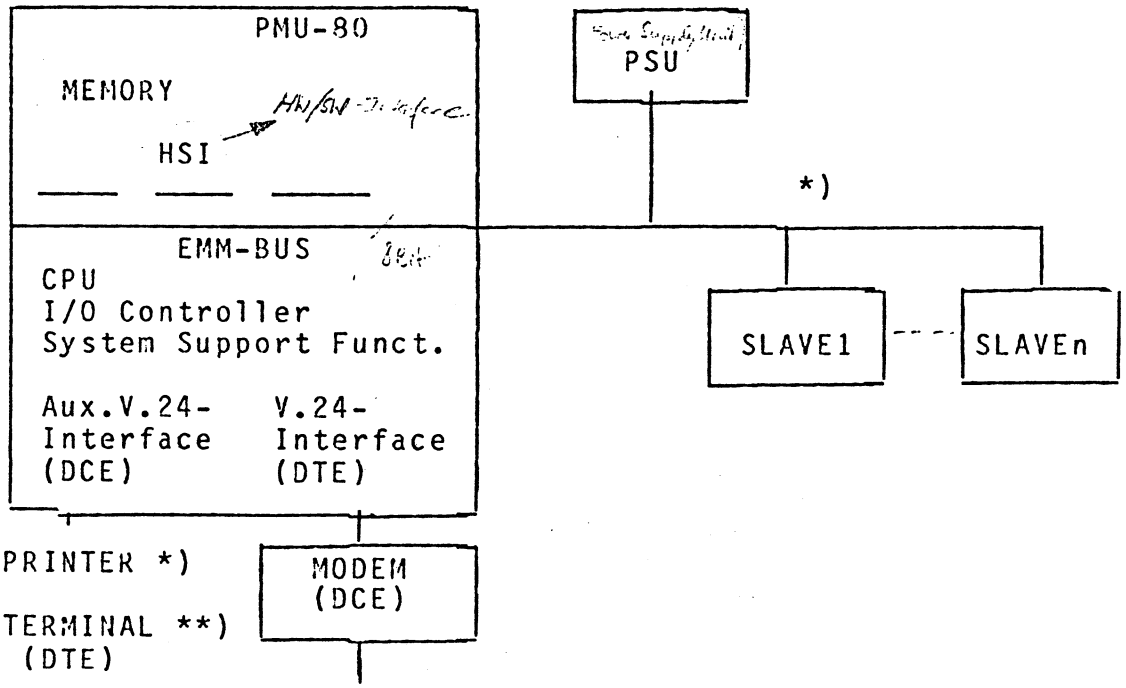
3.1 External Interfaces

3.1.1 General

Figure 3.1-1 shows the external interfaces of PMU-80.

Figure 3.1-1

External Interfaces



*) only if PMU-80 acts as MASTER

**) only if PMU-80 acts as SLAVE

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3.1.2 Interface Hardware - Software

3.1.2.1 General

Figure 3.1.2-1 illustrates all functional modules represented at the Hardware-Software Interface.

- Main Processor Unit
  - Z80-A CPU plus typical support components
  - Memory Mapping Unit
- Local Memory
  - 4KB (8K8) (P)ROM
  - 64KB dyn. RAM
- System Support Functions
  - Interrupt Control
  - Baud Rate Generation, Real Time Clock
  - Input/Output Control Ports
- Serial Interface Control
- Master-Slave Control Port

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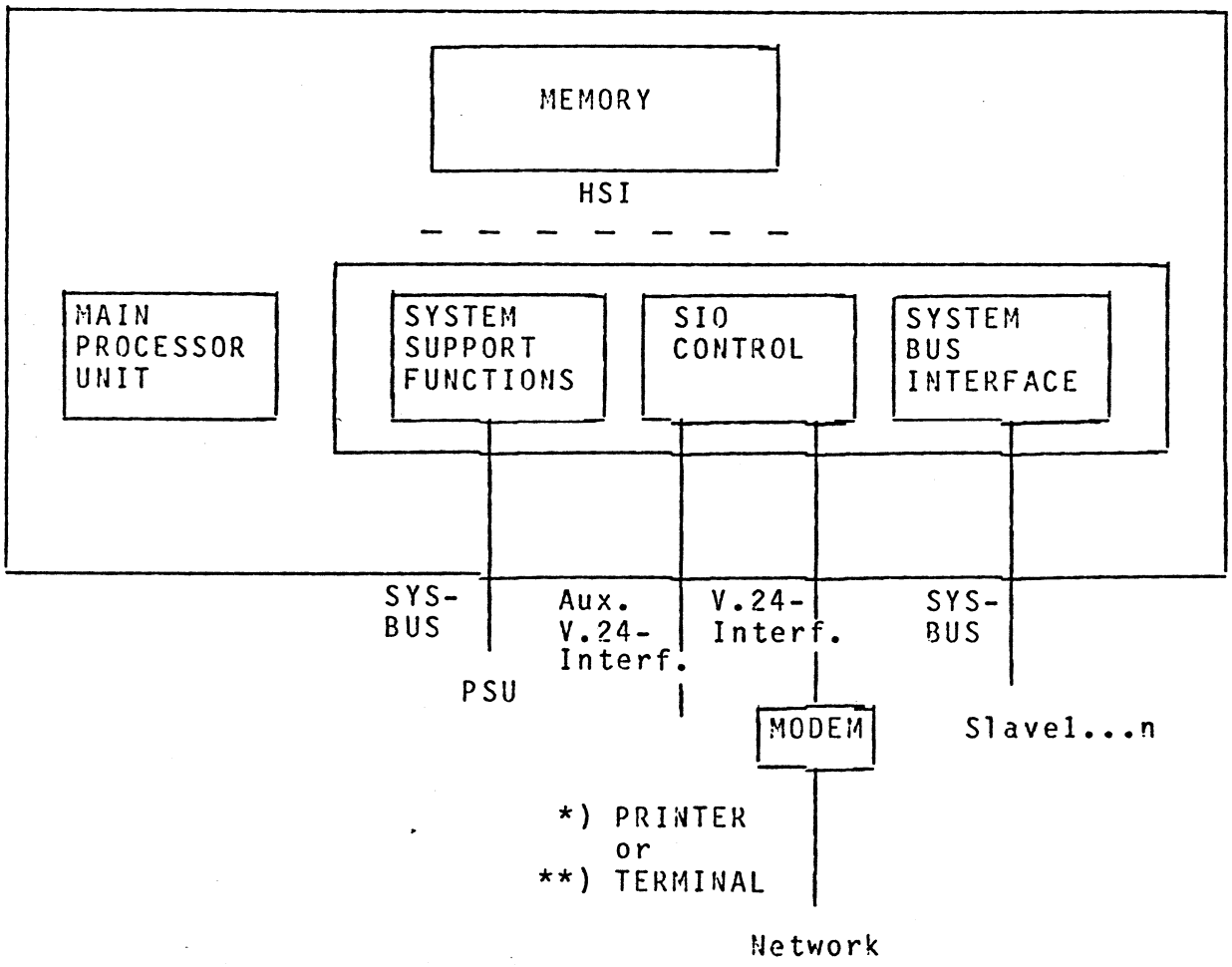
Figure 3.1.2.1-1

Main modules represented at the Hardware-Software Interface



*) if PMU-80 acts as MASTER

**) if PMU-80 acts as SLAVE

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3.1.2.2 Main Processing Unit

The Main Processing Unit, based on a Z80-A CPU will be responsible for the execution of arithmetic, logical and I/O instructions as specified by the program, stored in the local memory, as well as

- generating the required control signals to the memory or peripheral controllers situated on board or on separate cards via the system bus for memory - or I/O-access.
- servicing the interrupt request coming from interrupt system
- granting system bus control respectively local bus control to any DMA device, wishing to use the system bus respectively the local bus.
- extending of the 64KB address space of the Z80-A CPU to 1MB using a memory mapping mechanism (see ch. 3.1.2).
- resolving of System hang up if bus time out occurs.

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3.1.2.2.1 Processor Instruction Set

The processor instruction set is defined by the Z80-A CPU.

For description of the instruction set as well as all other relevant informations see /R5/.

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3.1.2.2.2 Main Processing Unit Addressing Capabilty

The Z80-A CPU is able to address

- up to 64KB memory (logical address space)
- up to 256 B~~/c~~input/output registers

The memory addressing capability will be extendable up to 1MB by use of a memory mapping unit (see ch. 3.1.2.2.3).

It should be noticed that the whole I/O address space is split up into parts which are reserved for certain purposes and are protected against unauthorized accesses:

- local I/O area

  cnly accessable by local CPU

- system I/O area

  only accessable by a PMU-80 which acts as master. It contains the I/O areas of the "common resources".

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Figure 3.1.2.2.2-1

PMU-80 I/O address space

address	assignment		accessable by
00H - 03H	Z80-A SIO (Serial Input/Output-Controller)	local I/O area	local CPU (master or slave)
04H - 07H	Z80-A CTC (Counter/Timer-Circuit)		
08H - 1FH	reserved		
20H - 23H	loc.I/O cont.ports		
24H	mem.mapp.port		
28H	master-slave interrupt reset		
30H-3FH	reserved		
40H-41H	master control port **)	syst. I/O area	master PMU
42H - 5FH	master- slave control ports		
60H - 6FH	DMA contr.reg. *)		
70H - 7FH	reserved		
80H - 82H	SASI-port *)		
88H - 8AH	operator panel *)		
90H - 9FH	reserved		
AOH - AEH	flex.disk contr.*)		
BOH - FFH	reserved		

*) accessed via EMM-Bus
**) allows a master to access its own control port

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3.1.2.2.3 Memory Mapping Unit

Initial-Program-Load

The Z80-A offers an addressing capability of 64KB. But the PMU-80, if it accesses to its own IPL-ROM or if it acts as master module, needs more than 64KB address space.

So, its own logical address space is split up into 16 pages of 4KB and one of these (either page 0 (after master reset) or page 1 according to the table below) can be mapped into a 1MB physical address space.

Dependent on two control port bits EXMAC = external memory access and MAPEN = memory mapping enable the address extension can be restricted to local memory or can be related to system memory according to the table below.

EXMAC	MAPEN	access to	via log address space
0	0	local memory, IPL ROM	0-0FFFH (page 0)
0	1	local memory extension	1000H-1FFFH (page 1)
1	0	local memory (phys. = log. address)	
1	1	system memory*)	1000H-1FFFH (page 1)

*) It should be mentioned that there is no possibility to access own local memory via this state.

The initial state of EXMAC and MAPEN after reset is zero.

For physical memory map see ch. 3.1.2.2.3.3

*) After master reset automatically the highest 4KB page of local physical address space will be accessed.

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3.1.2.2.3.1 Memory Mapping Port

The Memory Mapping Port, which contains the most significant address bits of the physical address is located on address 24H and is loadable only.
It's bit assignment is shown below.

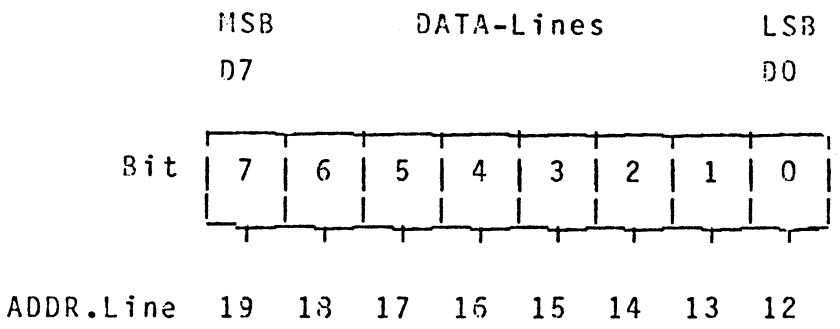

Figure 3.1.2.2.3.-1
Bit Assignment of the memory mapping port

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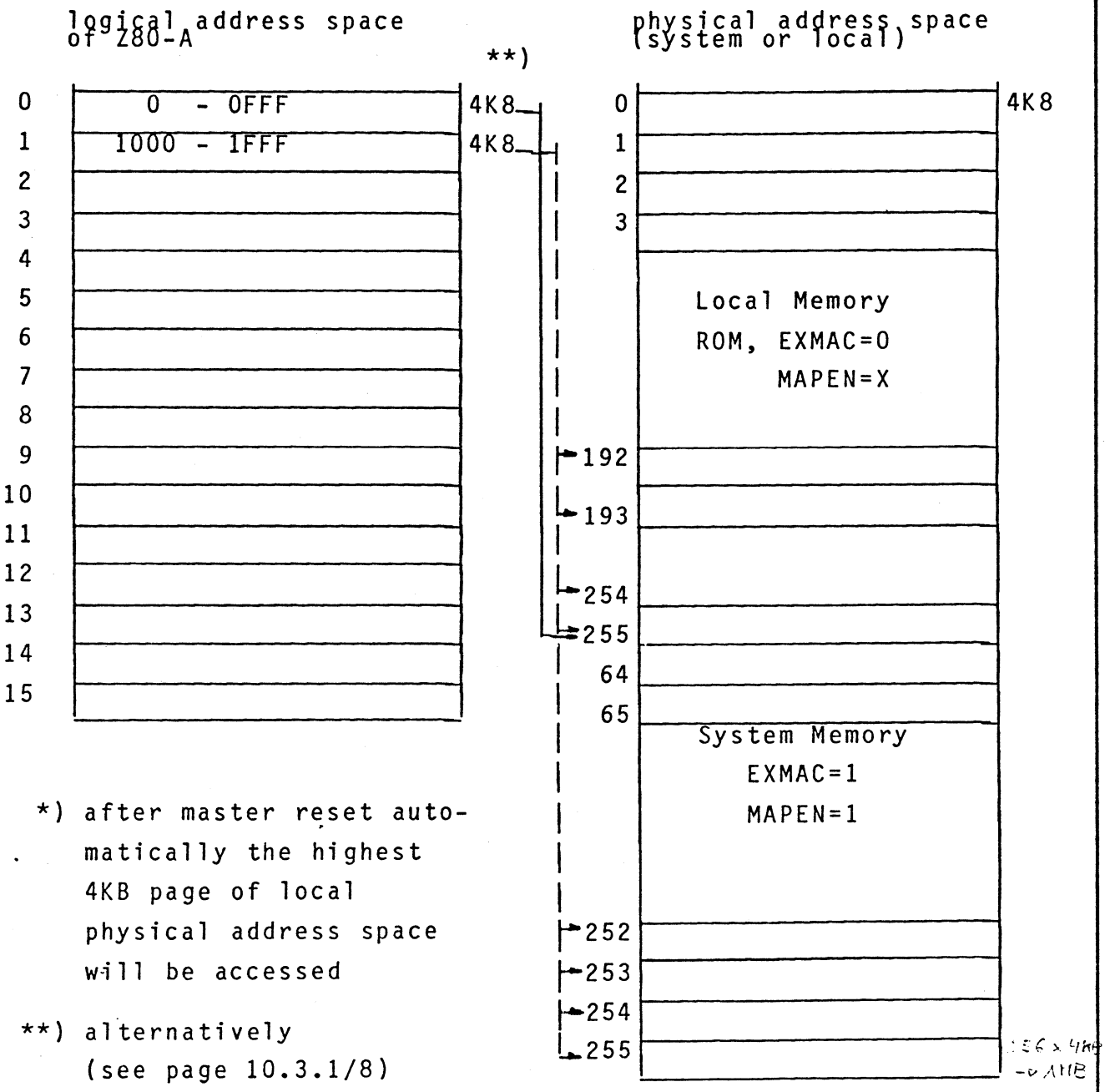
3.1.2.2.4 Memory Mapping Example



*) after master reset automatically the highest 4KB page of local physical address space will be accessed

**) alternatively (see page 10.3.1/8)

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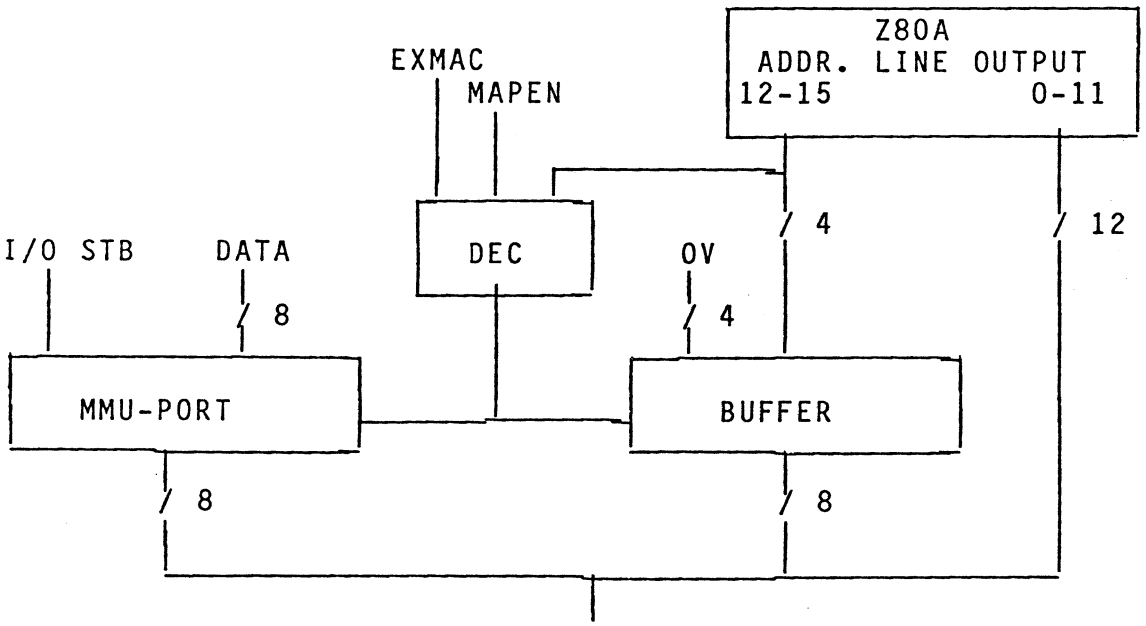
3.1.2.2.3.2 Memory Mapping Unit Blockdiagram



The MMU Port is an 8 bit wide output control port. The decoder circuit DEC detects a memory access to logical address space either 0-0FFFH (Mapen = 0, EXMAC = 0) or 1000H-1FFFH (Mapen = 1, EXMAC = X) and disables/enables the buffer respectively the MMU-Port dependent of the status of MAPEN and EXMAC.

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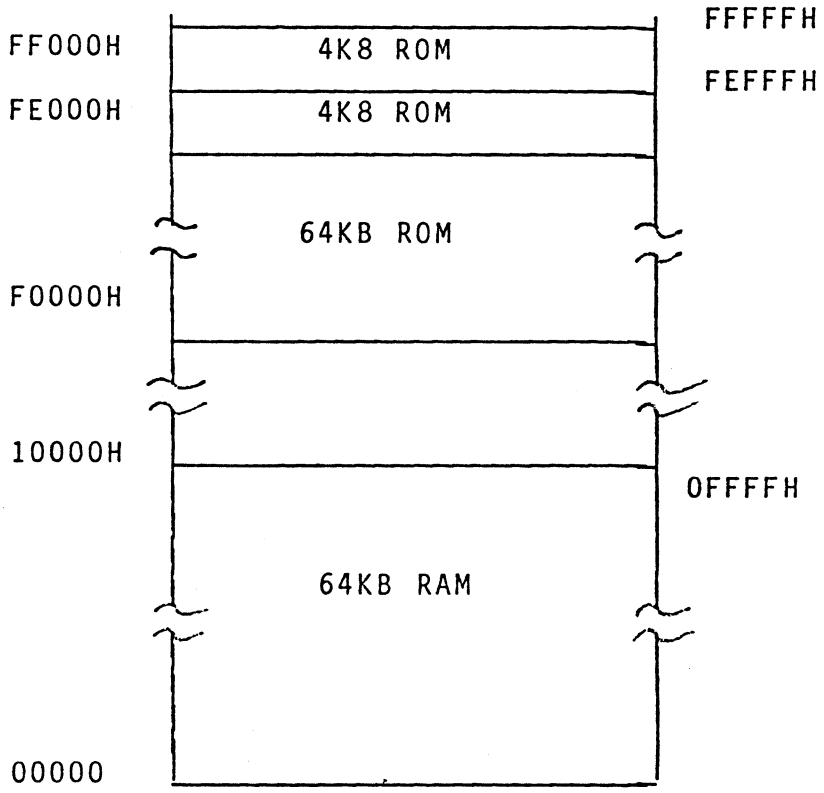
3.1.2.2.3.3 Physical Memory Map

a) local memory



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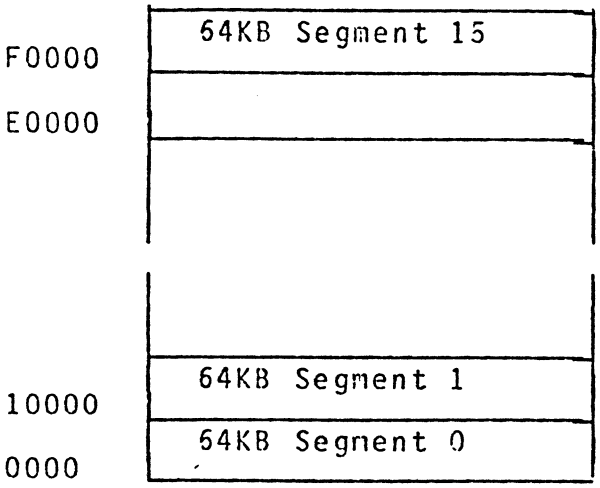
3.1.2.2.3.3 Physical Memory Map (cont'ed)

b) system memory



The system memory address space of 1MB will be devided into 16 segments, with a size of 64 KB each.

The local 64KB RAM area of every module is assigned to a certain segment of the system memory address space according to the schematic above.

The module number will be determined via the backpanel plug.

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3.1.2.3 Local Memory

The local memory consists of

8 KB (P)ROM and
64 KB dynamical RAM.

The ROM-part is assigned to memory address FE000H till FFFFFH.

Read accesses to even page numbers deliver the contents of FE000-FEFFFH, read accesses to odd page numbers deliver the contents of FF000H-FFFFFH.
A write into memory address space F0000H-FFFFFH has no meaning.

Start address of bootstrap program is FF000H.

The RAM-part is located from address 0 till 0FFFFH.

The RAM will be powered up when the system has been switched off and a battery back up unit and a battery or the mains are available.

The input control port signal "Automatic Restart Enable" (BARE) indicates whether the memory has been powered up or not during the last system off state.

See also 3.1.2.2.3.3 a) local memory map.

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3.1.2.4 System Support Functions

System support functions in this meaning are

- o Interrupt System
- o Baud Rate Generator and Real Time Clock
- o Input Output Control Ports.

3.1.2.4.1 Interrupt System

The PMU-80 shall be able to handle a number of maskable, asynchronous interrupts, created by I/O modules or peripheral controllers external.

The non maskable interrupt input of the Z80-A CPU will not be used.

Every interrupt is assigned by type code that identifies it to the CPU. The type code is used by the CPU to point to a location in a memory based interrupt vector table containing the address of the interrupt routine.

The interrupt system shall be able to use all the interrupt control functions offered by the ZILOG-type peripheral controllers as Z80-A CTC, Z80-A SIO and shall have an interrupt control module to provide handling of 8 additional single ended interrupt lines.

For detailed description of the interrupt facilities of Z80-A CTC, Z80-A SIO see app. A1, A2, A3 and ch. 3.1.2.5.

The interrupt control module shall have a priority encoder to encode the 8 single ended interrupt lines NIR 0-7 and shall be able to deliver the interrupt type code on the local bus, when the Z80-A performs an interrupt acknowledge cycle.

The interrupt lines have to be of level triggered nature.

Interrupt line NIR 3 can be disabled by control port 2 bit 4 "Terminal off Line Interrupt disable".

Only a master type of PMU-80 is able to react on interrupt lines NIR 4 - NIR 7. But both, master- as well as slave-types of PMU-80 are able to react on interrupt lines NIR 0 - NIR 3.

NIR 4 - NIR 7 are identical with EMM-Bus lines NIR 4 - NIR 7.

NIR 0 - NIR 3 are reserved for local interrupt sources.

NIR 3 is assigned to Terminal off line

NIR 2 is assigned to Command interrupt from master.

NIR0 is assigned to Power Failure Interrupt and can be disabled by control port 2, bit 0 "Power Failure Interrupt Inhibit".

The interrupt priority scheme is shown in table 3.1.2.4.1-1.

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Table 3.1.2.4.1-1

PMU-80 Interrupt Lines

Interrupt	Vector.Nr.	Source	Priority
Real Time Clock	*)	Channel 3, Z80-A CTC	highest
SIO-Interrupts acc. to initializ. of Z80-A SIO/2	*)	Z80-A SIO/2	
NIR 0	10	Power Failure Line	
1	12	reserved	
2	14	Master/Slave Control Port	
3	16	Power off	
4	18	SASI-Port	
5	1A	reserved	
6	1C	reserved	
NIR 7	1E	Flexible Disk Control	lowest

*) depends on initializing of CTC respectively SIO.

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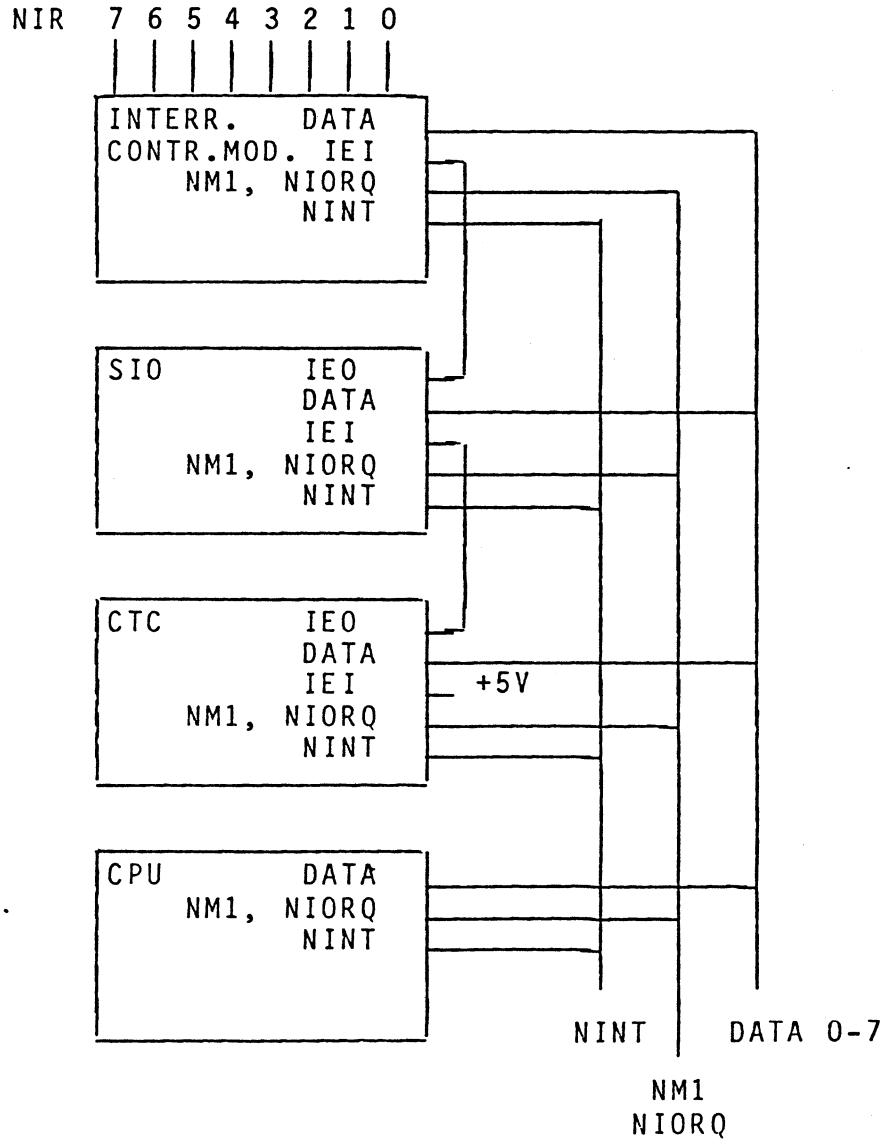
Fig. 3.1.2.4.1-1

PMU-80 Interrupt System



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3.1.2.4.2 Baud Rate Clock Generation and Real Time Clock

Baud Rate Clock Generation and Real Time Clock shall be performed by a Z80-A CTC.

Its internal registers are assigned to the following addresses:

Channel 0:	04H
1:	05H
2:	06H
3:	07H

Channel 0 functions as Baud Rate Clock Generator of the V.24 interface (if internal baud rate clock is required),

Channel 1 functions as Baud Rate Clock Generator of the Auxiliary V.24 interface,

Channel 2 is reserved, and

Channel 3 functions as Real Time clock Generator.

At the Clock/Trigger Inputs of all channels a frequency of 921,6 KHz will be applied.

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After master reset the following initialization should be done:

Channel 0 address 04H

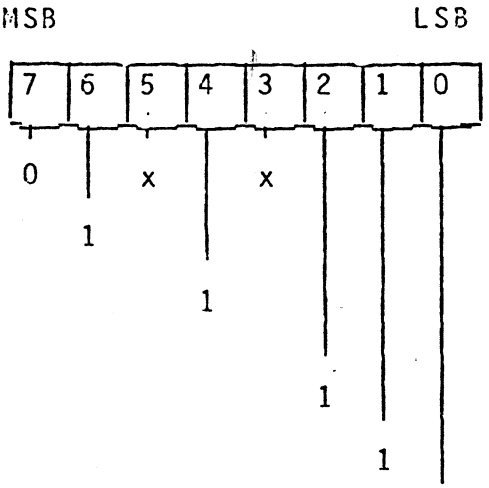
Normally not used (see chapter 3.1.4.3.2).
But if used, it should be noticed, that its output frequency will be devided by two, to produce a signal element timing with a 50% duty cylce.

Channel 1 address 05H

1. Channel Control Word:

commands:

- o Interrupt disable
- o counter mode selected
- o trigger on rising edge of CLK/TRG
- o time constant follows
- o software reset
- o control word identification



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2. Time Constant Word: address 05H

19,200 KB:	03H
9,600 KB:	06H
4,800 KB:	0CH
2,400 KB:	18H
1,200 KB:	30H

To calculate the frequency of the Baud Rate Clock the following formula must be applied:

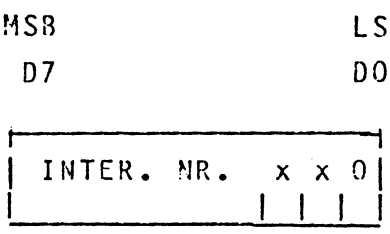
$$f_{BRC} = 921.6\ \text{KHz}: \text{time constant word}$$

Channel 2 address 06H

not used

Channel 3

1. Interrupt Vector Word: address 04H



The interrupt vector word contains the interrupt number on its bits D3-D7. D0 has to be zero D1, D2 are don't care.

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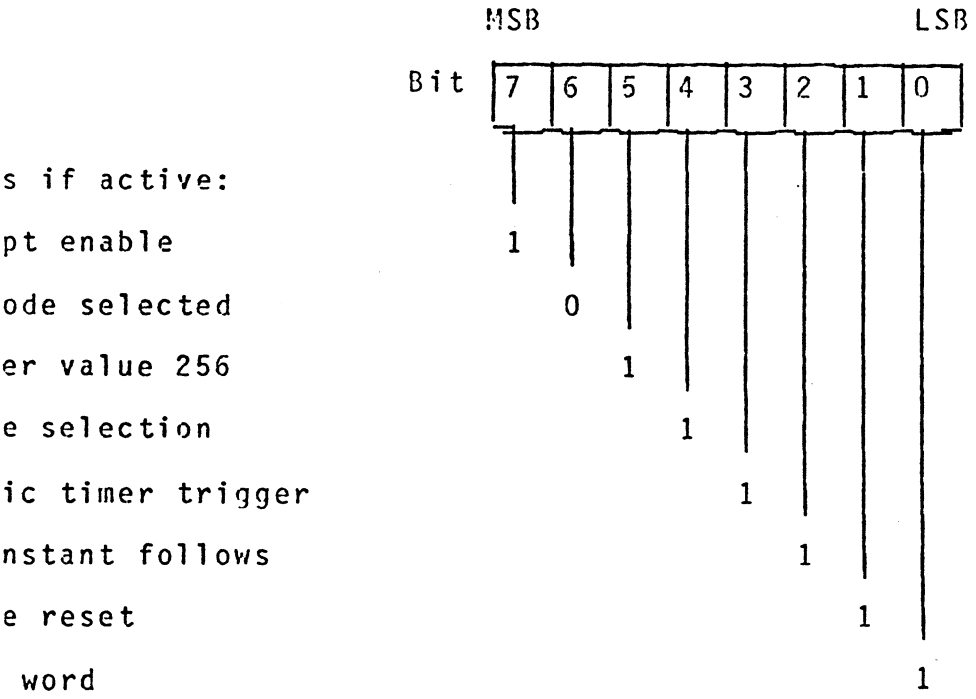
Channel 3 cont'ed

2. Channel Control Word: address 07H



3. Time Constant Word: address 07H

To calculate the frequency of RTC the following formula must be applied:

$$f_{RTC} = \frac{3.6864\ \text{MHz} : \text{presc. fact}}{\text{time const. word}}$$

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3.1.2.4.3 Input/Output Control Ports

Control port 1

Address: 20H, Input Port

Bit	7	6	5	4	3	2	1	0
states if active								
a) Data Set Ready (107) (V.24 Interf.)	1							
a) Test Indicator (V.24 Interf.)		1						
1) "Remote Power On" (108.2)(aux.V24 Interf.) Data terminal Ready (108.2)(aux.V24 interf.)			1					
2) Master Identification				1				
3) "Remote Power On" (109 or 125)(V.24 Interface)					1			
4) Memory not maintained						1		
5) No IPL requested							1	
6) Power Failure Not								1

a) This bits reflect status lines of the V.24 interface
1) Indicates the "Remote Power On" condition of aux. V.24 Interf.
2) Indicates that the PMU-80 acts as master.
3) Indicates the "Remote Power On" condition of V.24 Interface.
4) Memory was not powered up during the last system off time.
5) Master/Slave Control Port Bit
6) Reflects the state of Power Failure Line (for test purpose only).

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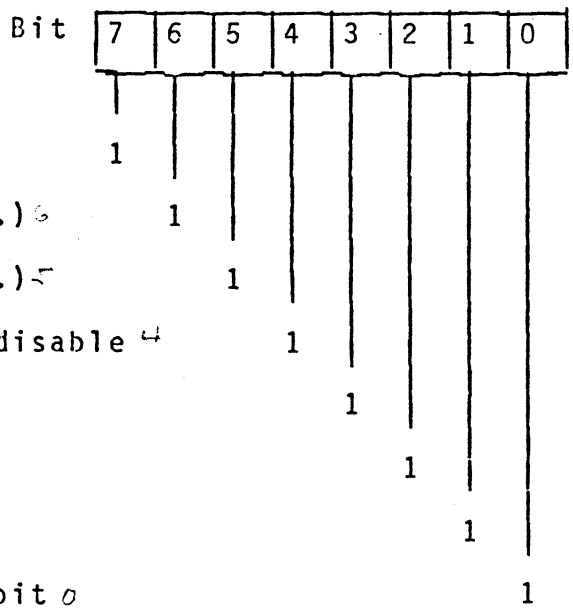
Control Port 2

Address: 20H, Output Port, loadable only,
cleared after master reset (zero)

Commands if active:



Test LED off 7

1) Remote loop on (V.24 Interf.) 6

1) Local loop on (V.24 Interf.) 5

Terminal off line interrupt disable 4

2) System Memory access enable 3

2) Memory mapping unit enable 2

3) Power off 1

Power failure interrupt inhibit 0

1) Control bits of the V.24 Interface

2) Combination of the two bits determines the several modes of memory access:

Bit 3	Bit 2	access to
0	0	local memory, IPL ROM
0	1	local memory, extension
1	0	local memory, (phys. = log. address)
1	1	system memory

3) Should only be used by master modules.

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Control Port 3

Address: 28H virtual output port,
accessable by an output command only,
contents: don't care

Control port 3 must be used to clear a master/slave command interrupt.

It is a virtual port, i.e. an output command into address 28H causes a reset signal on the master/slave command interrupt flip flop.

Accessing of this port should be done typically within a master/slave command interrupt service routine.

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3.1.2.5 Serial Interface Control

The PMU-80 shall provide two external interfaces from type of V.24/V.28 according to R/6/. These two interfaces will be controlled by the Dual USART Z80A-SIO/2.

Channel A shall support the V.24-interface (DTE) and channel B shall support auxiliary V.24-interface (DCE).

Interface A shall be able to act as "DTE" and to handle the following V.24 circuits.

V.24 circuit		corresponding bit of SIO's control/status register
101		-
102		-
103		-
104		-
105		RTS
106		CTS
107	(see note 1)	DSR (bit of control port 2)
108.2	(see note 2)	DTR
109	(see 3.1.4.2.1, RPON)	DCD
111		-
113		-
114		-
115		-
125	(see 3.1.4.2.1, RPON)	SYNC/HUNT
140		-
141	)	bits of control
142	)	port 1 (2)

Notes:
1) On-condition is indicated via a LED on the operator panel of the STOMO.
2) Circuit can be set to off-condition by the operator via a switch (see 3.1.3.2).

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Interface B shall act as "DCE" and shall be able to handle the following subset of V.24 circuits

V.24 circuit	corresponds to SIO's control/status register
101	-
102	-
103	-
104	-
105 (see note)	-
108.2 (see 3.1.4.2.1, RPON)	CTS
106	DTR
107	-

Note: Circuit 107 will be the looped circuit 108.2.
Circuit 105 will not be interpreted.
This selection of circuits was made in order to implement a simple aux. V.24-interface and to have the possibility to control the SDI as given with (R/2/).
In both cases the same 1:1 connection cable may be used.

Data Exchange shall be interrupt driven using the interrupt facilities of Z80-A SIO/2.

The internal registers shall be represented at the HSI as a set as listed below:

Address	Register
00H	data register ch. A
01H	data register ch. B
02H	command reg. ch. A
03H	command reg. ch. B

The handling of the internal register set is described in A3.

After system reset both channels have to be initialized (see A3).

Standard Initialization values are as follows

- Auxiliary V.24-Interface (DCE) t.b.s.
- V.24-Interface (DTE) t.b.s.

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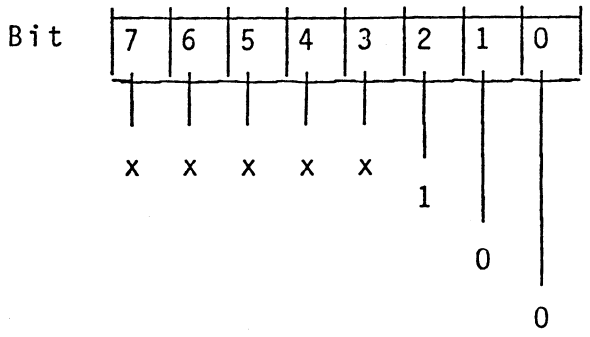
3.1.2.6 Master-Slave Control Port

The PMU-80 shall be equipped with a master-slave control port, which allows a master type of PMU to set up special control lines to a certain slave.

It is directly connected to the system bus. So, there is no need for the master to get control of the slave's local bus, if it wants to load a certain master-slave control port.

The ports are located from
40 - master
42 - slave 1
44 - slave 2
till
5E - slave 15
The bit assignment is as follows:



c.f.e.

1) handshaking interrupt
2) IPL requested
3) Selective master reset

After power on the port is cleared to zero, but it won't be influenced by is own selective reset signal.

Notes:

1) This bit must be set and immediately reset by the master module, to indicate, that the slaves command register or message buffer has been loaded. It causes an interrupt to the slave module.
(see also ch. 3.1.2.4.3, control port 3)

2) This bit is available on control port 1 and causes the slave to request an IPL.

3) This bit resets all the logic of the PMU, excluded the master slave control port and must be active for a time of at least 30 micro seconds.

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3.1.3 Interface Hardware - User

3.1.3.1 Inside Test Indication

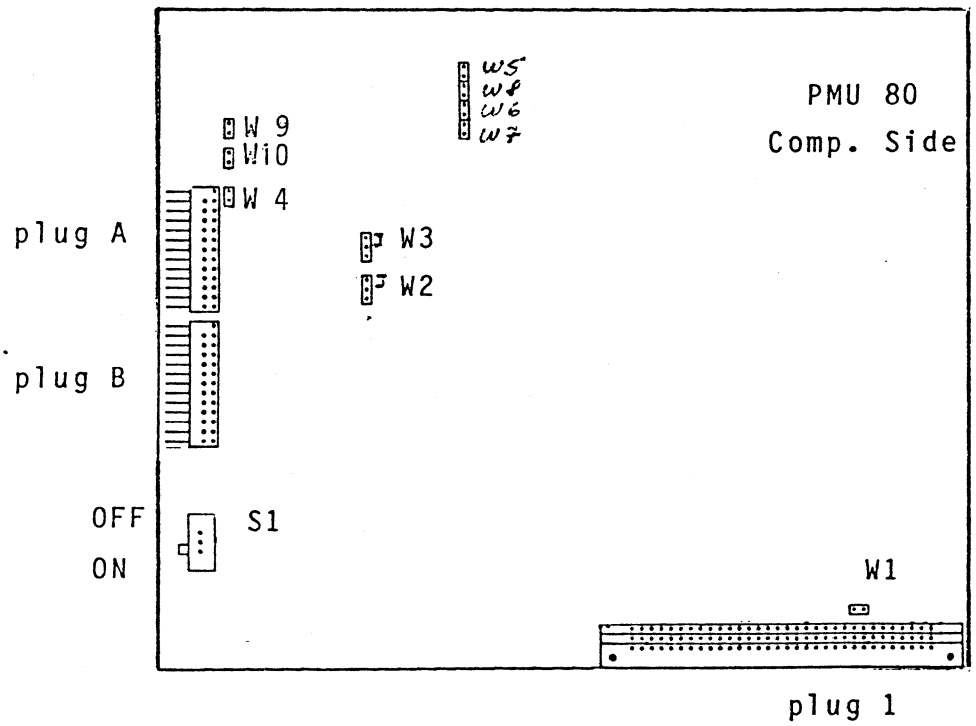
To indicate the state of the inside test, there is a Test LED available (see ch. 3.1.2.4.3, 3.3.8).

3.1.3.2 Hardware Straps

The hardware straps are located on the PCB according to figure 3.1.3-1.

Fig. 3.1.3-1

PMU 80 Hardware Straps



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3.1.3.2 Hardware Straps Cont'd

The assignment is as follows:

W1: Selection of Bus Clock Source
default: not mounted

W2,W3: Tx, Rx - clock selection of V.24 interface
default: internal clock selected according to fig. 3.1.3- 1

W4: Remote Power On via 108.2 of aux. V.24 interface
default: mounted on slaves, not mounted on masters

W5,W6,W7,W8: Offer interruption possiblity of the following lines: NM1, NRFSH, NBACK, NHALT.
This feature will be used for service test purposes.
default: mounted

W9: Remote Power On via circuit 125 of V.24 interface
default: not mounted

W10: Remote Power On via circuit 109 of V.24 interface
default: not mounted

S1: Will be used to switch off circuit 108.2 of V.24 interface
default: On.

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3.1.3.3 Special Logic Lines

The bus connector should contain four special logic lines SLL0-SLL3 to define a certain device number to every PMU. This provides determination of device number dependent on the backpanel slot the PCB has been mounted.

For P3500 the following assignment exist:

SLL0	SLL1	SLL2	SLL3	
H	H	H	H	master
L	H	H	H	slave 1
H	L	H	H	slave 2
L	L	H	H	slave 3
		.		
		.		
		.		
L	L	L	L	slave 15

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3.1.4.2 Interface to Power Supply and Battery Back Up Unit

The logical interface to PSU/BBU shall provide the following functions:

- o master reset for all logic circuits
- o power failure indication to support power break down handling
- o software controlled power off (planned power off)
- o remote power on
- o surveillance of BBU status during power off

These functions will be realized by the following signals:

- o RSLN reset line not
- o PWFN power failure not
- o RPON remote power on (planned power off)
- o BARE battery was off/automatic restart enable.

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3.1.4.2.1 Signal Definitions

RSLN services as reset signal for all logic circuits to avoid misoperating during switch on and switch off.

PWFN indicates a power failure, i.e. the main voltage has come below its minimum value and causes the system to start special save routines.

RPON is used to switch on the system remotely via

a) serial interface A circuit 125 (ring indicator) in case of a switched line.
b) serial interface A circuit 109 (data carrier detect) in case of a fixed line.
c) serial interface B circuit 108.2 (data terminal ready) if the directly connected terminal is not a printer only.

The wanted function is strapped via jumpers (see 3.1.3.2).

A high level RPON switches on the PSU. A low level RPON, caused by an output port control bit, switches off the system.

BARE reflects the status of the battery back up unit during system off state. Its status will be updated only when RSLN changes from active to inactive state and is available as input signal on the input control port.

Figure 3.1.4.-1 gives a rough information about the timing requirements.

For all detailed informations see R/4/.

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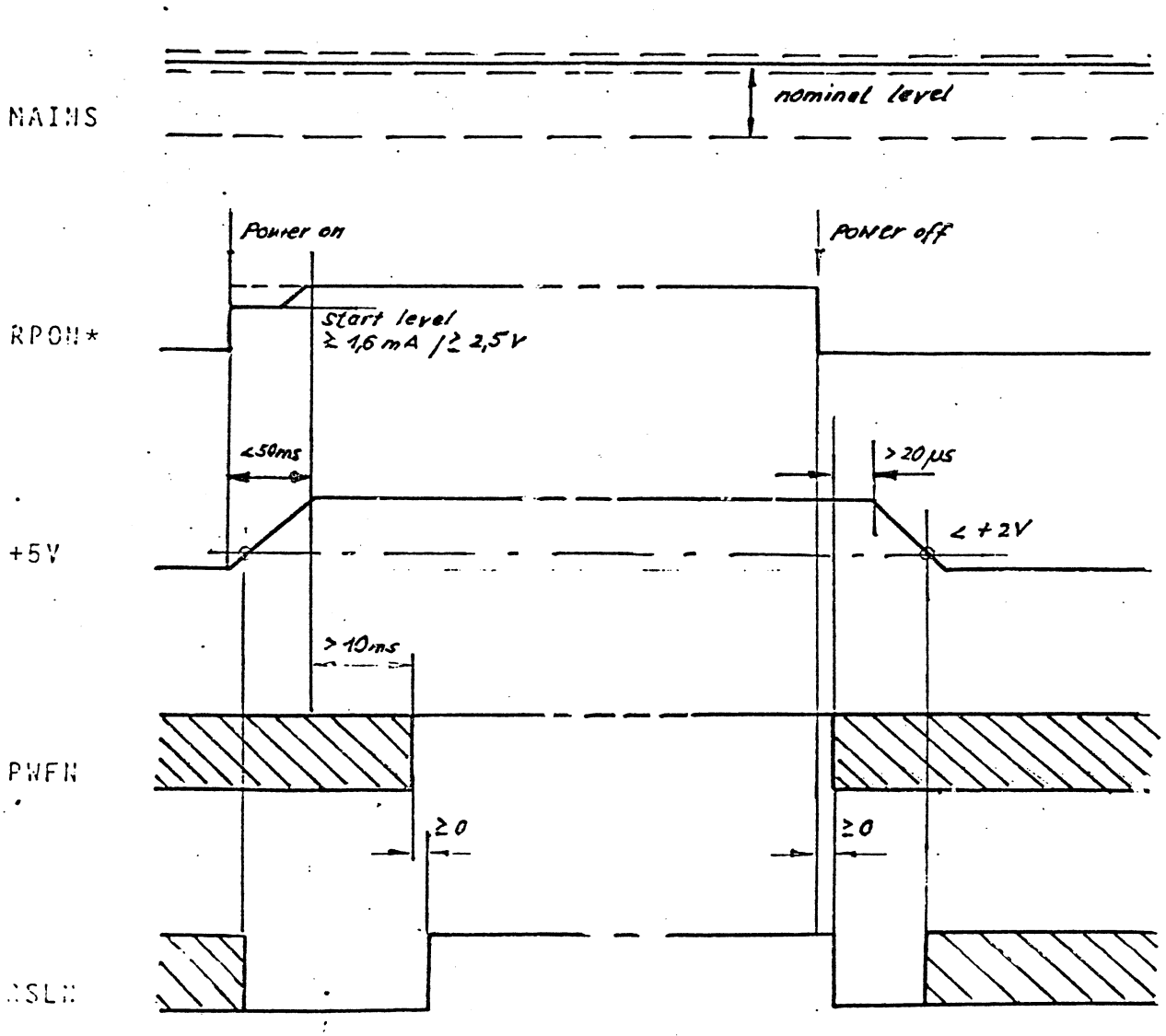
Figure 3.1.4.2-1

Power on/off Sequencing (planned on/off)



* min hold time as long as +4,75V level is not reached.

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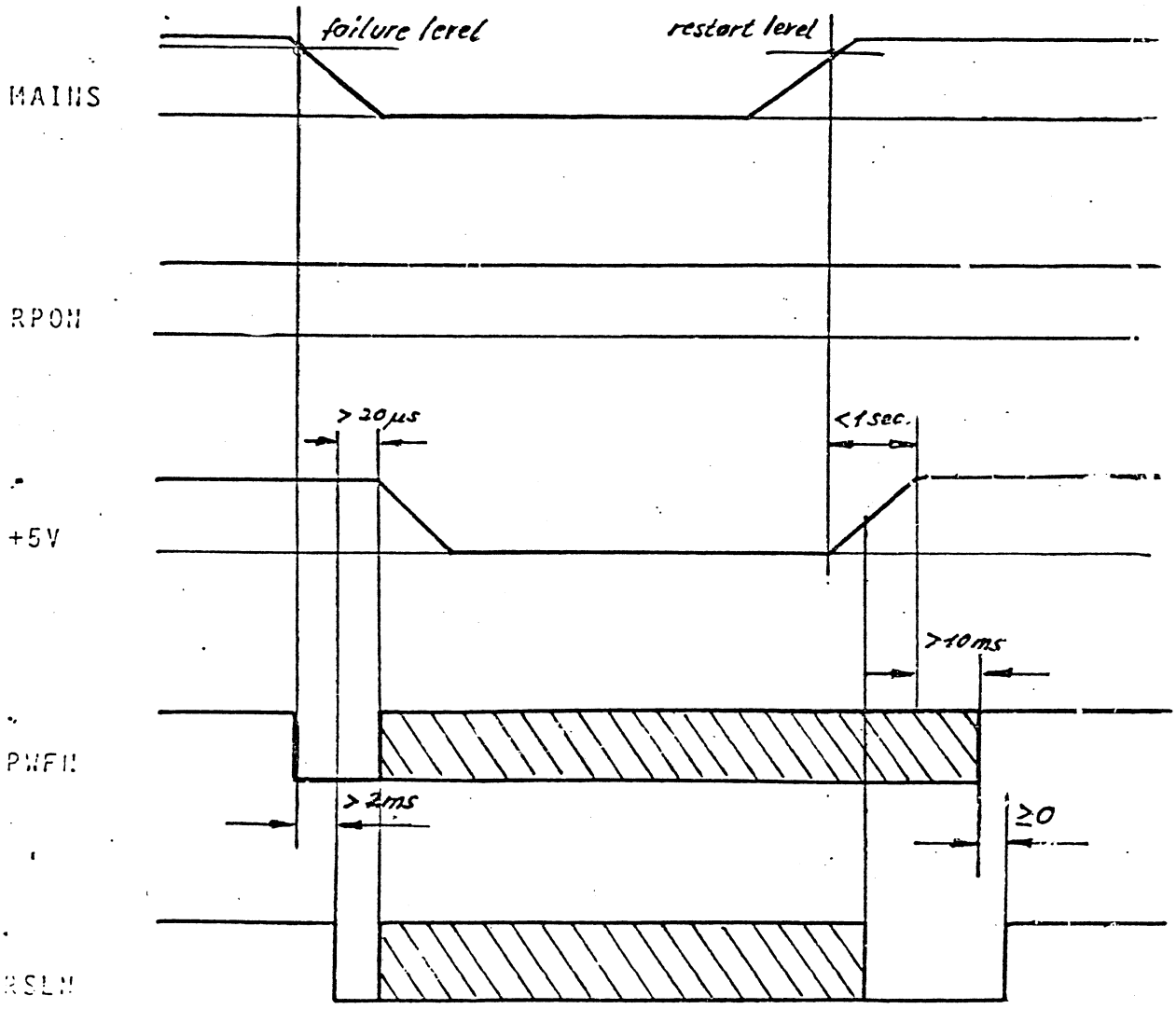
Figure 3.1.4.2-2

Power Break Down / Restart



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3.1.4.3 Serial Interfaces

3.1.4.3.1 Auxiliary V.24-Interface (DCE)

The following circuits are provided at plug B.

101	*)	108.2
102		106
103		107
104		

3.1.4.3.2 V.24-Interface (DTE)

The following circuits are provided at plug A:

101	*)	111
102		113
103		114
104		115
105		125
106		140
107		141
108.2		142
109		

*) directly connected to shield and housing by using of puc-system

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3.1.5 Electrical Interfaces

3.1.5.1 EMM Bus Interface

The PMU 80 is connected to the following bus lines:

Bus Signal	Type	Fan in	Fan out
NADR0-NADR19	Transceiver	H: 0,045 mA	15 mA
	Tristate	L: - 0, 65 mA	- 24 mA
NDAT0-NDAT7	Transceiver	H: 0, 02 mA	15 mA
	Tristate	L: - 0, 4 mA	- 24 mA
NIOWC, NIORC	Transceiver	H: 0,045 mA	15 mA
NMWC, NMRC	Tristate	L: - 0, 65 mA	- 24 mA
NXACK	Transmitter	- 0, 25 mA max	- 24 mA
	Open collector	H: 0, 02 mA	
NBPRI	Receiver	L: - 0, 4 mA	
	Transmitter		H: 0,4 mA
NBPRO	Totem-Pole		L: 8 mA
	Transmitter		
NBUSY	Open collector	- 0, 25 mA	- 24 mA
	Transmitter	- 0, 02 mA	
NBCLK	Totem-Pole	- 0, 6 mA	- 20 mA
	Transceiver		
NCBRQ	Open collector	- 0, 25 mA	- 24 mA
NIR4, NIR5	Receiver	H: 0, 02 mA	
NIR6, NIR7		L: - 0, 4 ma	
		H: 0, 02 mA	
PWFN, RSLN	Receiver	L: - 0, 04 mA	
		H: 0, 02 mA	
BARE	Receiver	L: - 0, 02 mA	
	Transmitter		
RPON	Open collector	- 0, 25 mA	- 24 mA
SLL0, SLL3	Receiver	H: - 0, 02 mA	
SLL1	Receiver	L: - 0, 4 mA	
		H: - 0, 4 mA	
SLL2	Receiver	L: - 3,0 mA	

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3.1.5.1 EMM Bus Interface Cont'd

Power Supply Lines

+ 5V
0 V
+ 12V
- 12V
+ 5VM

3.1.5.2 Auxiliary V.24 Interface

All circuits shall be according to V.28 (R/6/).

3.1.5.3 V.24 Interface

All circuits shall be according to V.28 (R/6/).

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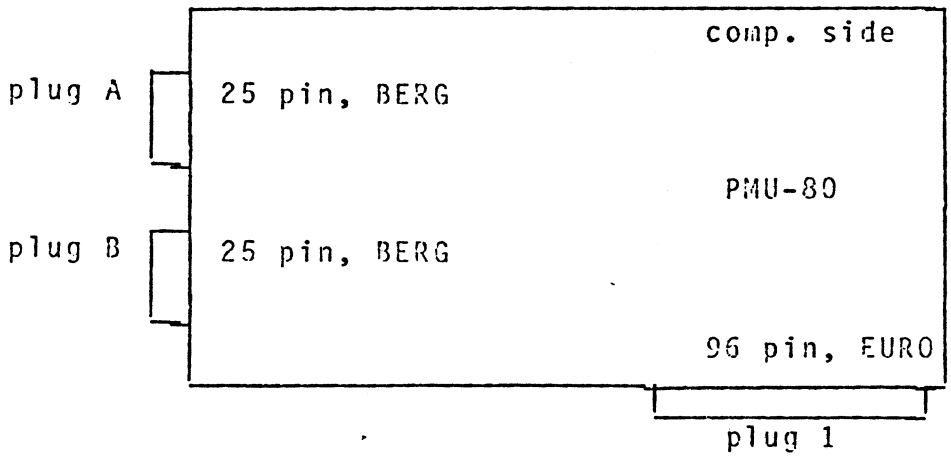
3.1.6 Mechanical Interfaces

3.1.6.1 PCB Dimensions

The logic shall be situated on a standard Double Euro PCB.

3.1.6.2 Connectors

The PMU-80-PCB contains three connectors which are situated on the PCB according to the scheme below:



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3.1.6.2.1 Pin Assignments

	b	a
1		
2	A103	A114
3	A104	
4	A105	A115
5	A106	A141
6	A107	
7	A102	A108.2
8	A109	A140
9		A125
10		A111
11		A113
12		A142
13	Dummy	

Plug A

(V.24-interface)

	b	a
1		
2	B103 ←	TD
3	B104 ←	RD
4	B105*)	RTS
5	B106 ←	CTS
6	B107	
7	B102 GND	B108.2 DTR
8		
9		
10		
11		
12		
13	Dummy	

Plug B

(Aux. V.24-interface)

* See Chapter 3.12.5.

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Pin Assignment (cont'ed)

Plug 1 (System Bus)

	a	b	c
1	+5V	+5V	+5V
2	0V	+5V	SLL3
3	0V	0V	0V
4	SLL0	SLL1	SLL2
5	NBUSY	NBLCK	NCBRQ
6			NDACK1
7			
8			
9	NIR4	BARE	NIR5
10	NIR6	RSLN	NIR7
11	0V	0V	0V
12	NDAT0	NDAT1	NDAT2
13	NDAT3	NDAT4	NDAT5
14	NDAT6	NDAT7	
15			
16			
17	PWFN	RPON	
18	0V	0V	0V
19	NADR0	NADR1	NADR2
20	NADR3	NADR4	NADR5
21	NADR6	NADR7	NADR8
22	NADR9	NADR10	NADR11
23	NADR12	NADR13	NADR14
24	NADR15	NADR16	NADR17
25	NADR18	NADR19	
26			
27	NIOWC		
28	NIORC		NMWC
29	NXACK		NMRC
30	NBPRI		NBPRO
31	+12V	+5VM	+5VM
32	-12V	-5V	

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3.1.7 Thermal Interfaces

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3.2 Performance

3.2.1 General

The PMU-80 shall perform all the instructions according to the instruction set of the Z80 as mentioned above. It shall be able to act as master as well as slave which will be determined by special logic lines SLL0-SLL3. (see chapter 3.1.3.3).

Working as slave, only local bus operations are required. As master, PMU-80 shall be able to achieve system bus control and to access system I/O area as specified in chapter 3.1.2.2.2. As master, it shall also be able to communicate with slaves by accessing their local bus via a memory mapping mechanism as described in chapter 3.1.2.2.
Furthermore the PMU-80 shall provide, that a DMA control module connected on its system bus interface can access its local memory.
The wait state generator/time out logic shall resolve bus hang up situations.
All memory or I/O read/write transfers shall be performed according to the EMM-Bus specification (R/1/).

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3.2.2 Performance Characteristics

Processor frequency	:	3.6864 MHZ
Local memory access (RAM or ROM)		
. op code fetch	:	4 clock cycles (1 wait state)
. read/	:	3 clock cycles (no wait state)
write	:	4 clock cylces (1 wait state)
I/O access	:	4 clock cycles (1 wait state)
Interrupt acknowledge cycle	:	5 clock cycles (2 wait states)

System memory accesses will be delayed for additional clock cycles due to bus arbitration sequences on the system bus and the slave's local bus.

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3.2.3 Operability

3.2.3.1 Realiability

The PMU-80 shall have a failure rate better than 0.025 10-3 h -1 or a MTBF of 40.000 hours, respectively.

3.2.3.2 Maintainability

The mean time ro repair (MTTR) in the workshop with their tools should not exceed 30 minutes.

3.2.3.2.1 Maintenance and Repair Cycles

not applicable

3.2.3.2.2 Service and Access

On line Diagnostics

By means of the execution of a diagnostic program on the system it should be possible to test the functions of the PMU-80.

The PMU-80 tests its own functions with the aid of a self-test program (inside Test) which is started with power-on or programmed selective master reset.

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Test and Diagnostics of PCBs

To accomplish final production tests to check the correct functioning of PMU-80 and to diagnose errors on component level it should be possible to apply testers like GenRad1976 or P488.

For repair in the service workshop it must be possible to use the system.

For that the design of the PMU-80 has to be done in such a way that it fits in a pinbed-adaption-facility of the used testers as well as in the system by using an extension adapter.

3.2.3.3 Useful Life

The useful life time shall exceed 15.000 power on hours or seven years which ever occurs first.

3.2.3.4 Human Performance

Not applicable

3.2.3.5 Safety

Not applicable

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3.3 Design Constraints

t.b.s.

3.3.1 General

t.b.s.

3.3.2 Software Design Constraints

t.b.s.

3.3.3 Logical Design Constraints

t.b.s.

3.3.4 Electrical Design Constraints

DSS VOL 2 must be applied.

3.3.5 Mechanical Design Constraints

DSS VOL 3 must be applied.

3.3.6 Technological Design Constraints

The design shall be based on the Z80A Central Processing Unit.

3.3.7 Thermal Design Constraints

DSS VOL 2 must be applied.

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3.3.8 Test and Diagnostic Tools and Provisions

In order to start each application session from a defined situation the PMU-80 will be provided for an Inside Test facility which will be started by:

- power on
- programmed selective master reset

At the beginning of the Inside Test Procedure a LED will be switched on.
In case of power-on or programmed selective master reset it will be switched on by hardware.

In case of use the PMU-80 as master the peripheral Control Units without any intelligence will be tested by the PMU-80, too.
After performing the test the status of all slaves will be sampled and will be made available for a diagnostic program.

In case of an error an indication will be given to the operator panel and the corresponding LEDs on the PCB(s) will not be switched off..

If the PMU-80 acts as slave the test status will be stored into its local memory and will be available for the master PMU-80.

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4. Quality Assurance

t.b.s.

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