INDEX PMU80-3

LIST OF ILLUSTRATIONS

1. PROCESSOR

The processor used in the PMU 80-3 is the high speed Zilog Z80. All information concerning this chip can be found in the data sheets. However, for the purpose of these descriptions, two important points should be noted:

(i) The processor is operating in interrupt mode two.
(ii) The Non-Maskable interrupt is not used owing to limitations in the software.

The signals NMRQ (Memory Request), NIORQ (Input/Output Request). NRD (Read) and NWR (Write), are gated (at D5F6) to create the four standard control lines of the EMM Bus, these are:

NMRCL - Memory Read Command Local
NMWCL - Memory Write Command Local
NIORCL - Input/Output Read Command Local
NIOWCL - Input/Output Write Command Local

These signals and the signals BACKL (Bus Acknowledge Local), NIORQL, and NMRQL are only valid when the disabling signal COMDIS (Command Disable), for the drivers D5E4 and H0F3 is inactive (low).

2. SYSTEM TIMING

The timing for the system is based on a crystal (G4F9) of frequency 12 MHz. The crystal is connected to a Voltage Controlled Oscillator located at G2F5. The facilities for controlling the range and frequency of the oscillator are not used. Therefore, both controlling inputs (pins 2 and 3) are connected to 2.5V.

The waveform on the output of the VCO (OSC - Oscillator), has the same frequency as the crystal. It is supplied to a divider (G2E6) which outputs two signals which are connected to pin 1 and 3 of the strap W1 (G3F4).

Strap between:

1 and 2	PRCLK (Processor Clock)	= 6 MHz	(Normal operation)
3 and 2	PRCLK	= 3 MHz	(for Test Purpose)

PRCLK is fed to T5 (testpoint 5), and is inverted at F6D4, to create the signal NBCLK (Bus Clock). The signal NBCLK can be supplied to the EMM Bus, using the strap W3 (F1D1).
The circuit around the gate, at F6D4 is used to correct the edges of PRCLK.

3. SERIAL INTERFACE

The SCC (Serial Communications Controller) controls the channel A and B interfaces.
Channel A: V24-interface
Channel B: short distance interface
Channel B can be strapped as either a DCE interface or as a DTE interface.

Before these interfaces can operate, the chip must be programmed by the processor. Programming is achieved by the processor writing a string of command bytes to the command registers of each channel. The command registers are assigned to the following IO addresses:

Channel A - 02
Channel B - 03

A command byte, present on the data bus DATL7-0, is written into the command register when NCSSCC (Chip Select SCC) is activated. The command byte is written into the command register specified by the level of the address line ADRL0, i.e.

ADRL0 = 0 selects Channel A
ADRL0 = 1 selects Channel B

The level of ADRL1 specifies whether the contents of DATL7-0, is a command or data byte, i.e.

ADRL1 = 0 data
ADRL1 = 1 command

Once programmed, the SCC is ready to transmit or receive data.

After a data byte is received or send, the line NINT is activated. The interrupt acknowledge circuit replies with an interrupt acknowledge (NINTACK). An interrupt vector is released by the SCC, and the Interrupt Service Routine (ISR) will cause the data to be read or write from the appropriate register. The data registers are assigned to the following addresses:

Channel A - 00
Channel B - 01

Data is received at a rate determined by the SCC clock inputs.
For Channel B, TCLK (Transmit Clock) is connected to RTxCB (Receive Transmit Clock). TCLK is an output from a divider located at G2E6.
TCLK can strapped for:

strap between	
1 and 2	TCLK = 3,072 MHz (normal operation)
2 and 3	TCLK = 1,536 MHz (test purposes)

The Voltage Controlled Oscillator at G2E5 supplies the clock at a frequency of 6,114 MHz to the divider.

For Channel B, there are two possibilities:

(i) The signal TCLK is connected to RTxCB when strap W23 2 and 3 is in place.
(ii) If the strap is placed on 1 and 2, the clock from the interface will be

used.

The output of gate B8D4 (circuit 109 ored with 125) can be strapped (W20 1 and 2) to form the DCDA (Data Carrier Detect) for channel A.

The signal NDSRA (Data Set Ready), circuit 107, is fed to the buffer at B8F3 where it forms the signal NOLI (On Line In). NOLI is fed to connector 5. With a switch on connector 5, NOLI is connected to NOLS (On Line Switch). With the signal NDSRA active low, NOLS is activated. The signal DTR (Data Terminal Ready) output of gate B8D4 is disabled. With removing the switch, or switch off, DTR is enabled.

The signals TxDA and TxDB are disabled at gate E7D4 and B4A3 with the signals NRTSA (Request to send) and NRTSB inactive.

4. REMOTE POWER CONTROL

The purpose of this circuit is to provide a remote device with the ability to switch the system power supply on or off.

The line RPON (Remote Power On) is output to the power supply via the EMM Bus. A high level on this line switches the power supply on, while a low level switches it off. This line can be driven high in four ways, by:

(i) A high level on the line A125 (Ring Indicator), with strap W21 1 and 2 in place. (A8F0)

(ii) A high level on the line A109 (Data Carrier Detect), with strap W21 3 and 2 in place.

(iii) A high level on the line B109 (Data Carrier Detect), with strap W14 1 and 2 in place. (DTE mode)

(iv) A high level on the line B108 (Data Terminal Ready), with strap W14 2 and 3 in place. (A9D6) (DCE mode)

The lines A125 and A109 originate from the V.24 interface, but the lines B108 and B109 originate from the auxilliary V.24 interface.

The line NPWOFF (Power Off) is strapped at C3G1 (W16) for:

strap between	
1 and 2	interrupt power off via CT 108 (DCE)
2 and 3	interrupt power off via CT 109 (DTE)

This line is normally high when the terminal is switched on.

5. LINE TRANSMITTERS AND RECEIVERS

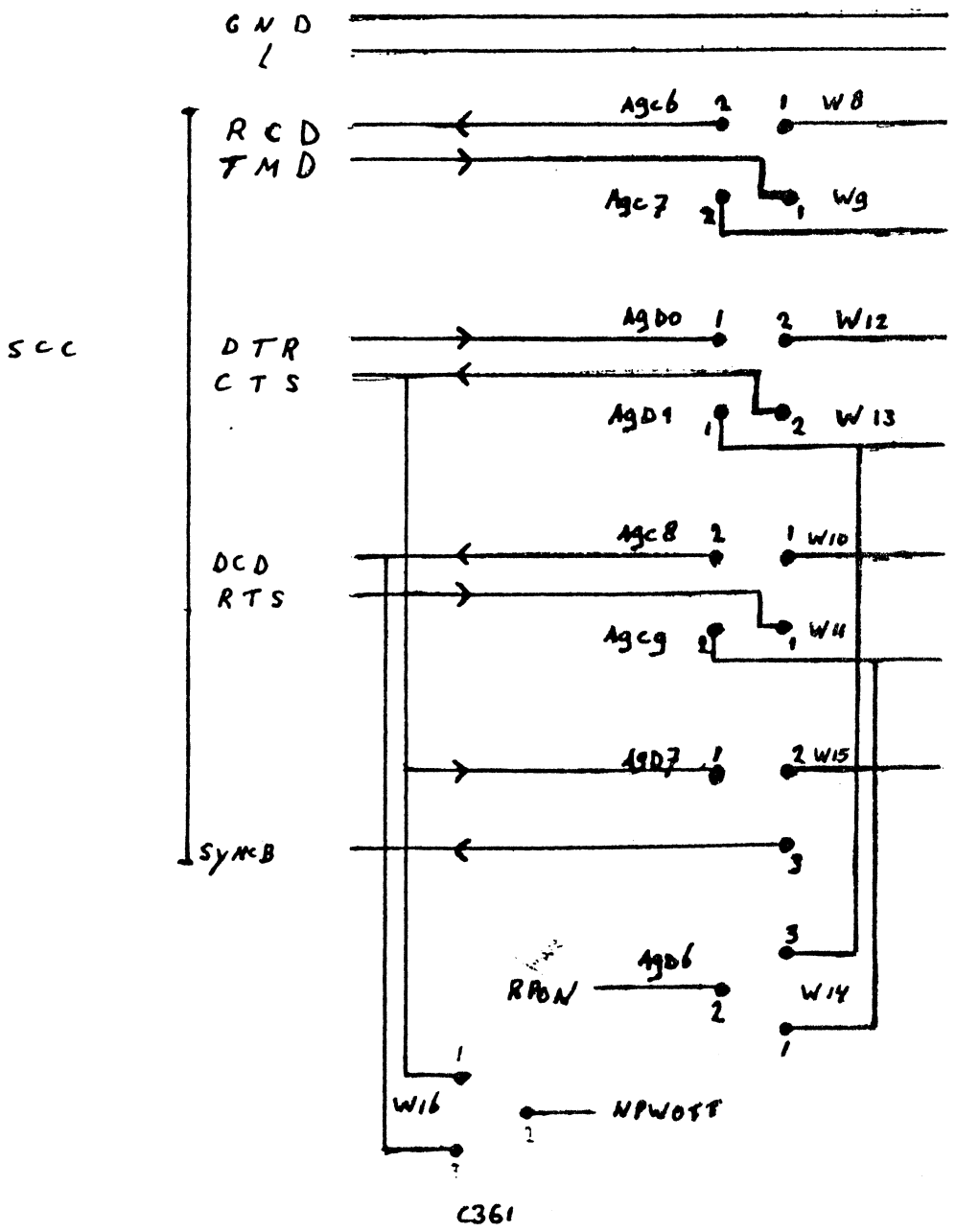
The control line of the V.24 and auxiliary V.24 interfaces are input to, or output from, the PMU80-3 via the Line Receiver and Transmitters respectively.

The circuit consist of two different types of gates (75189 and 75188) which function as follows:

- 75189, changes (and inverts) the V24 level (12V) to TTL level (5V).
- 75188, changes (and inverts) the TLL level to V24 level.

CH B
alle Straps offen

PMU 80-3V

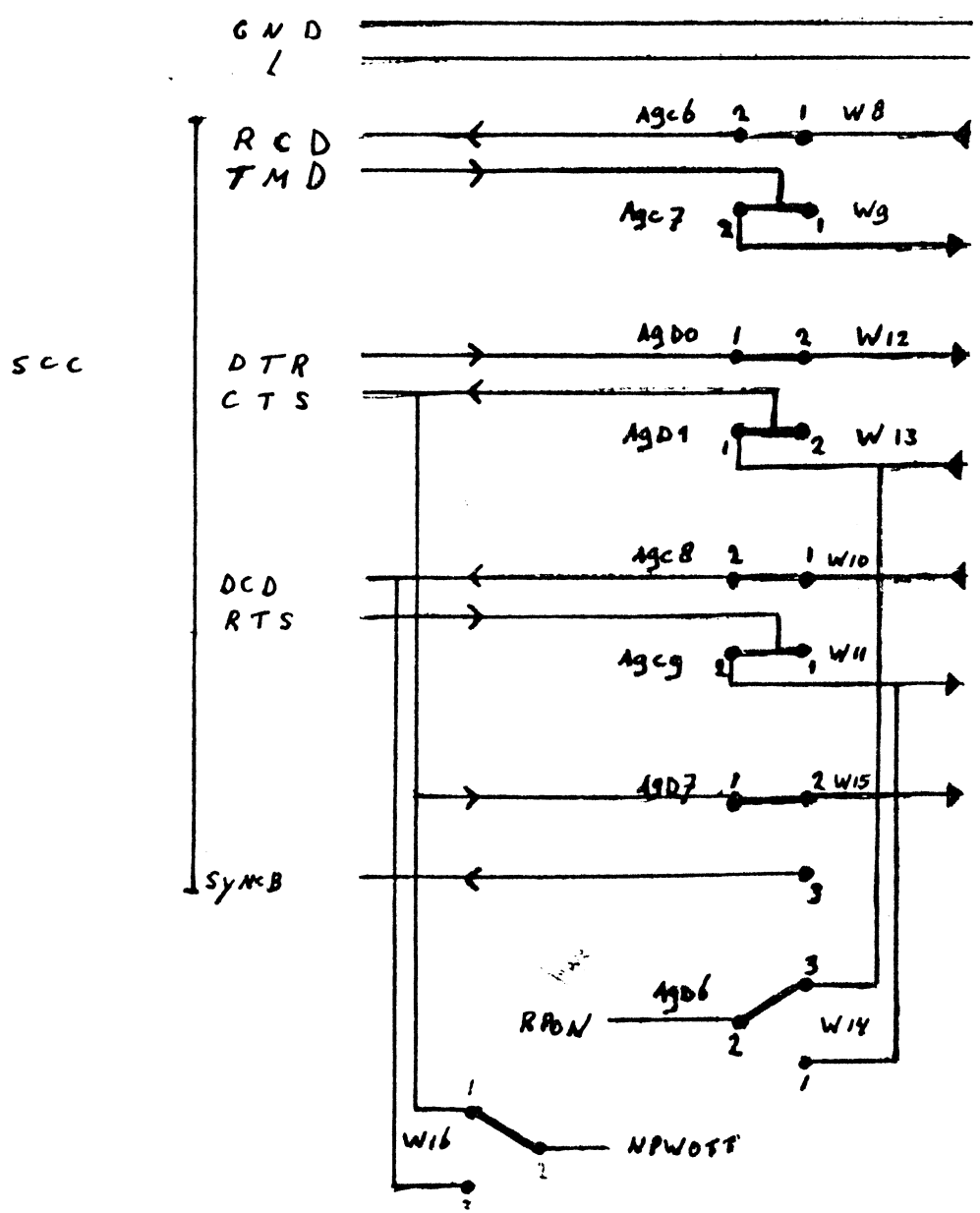


CC ITT	NAME	PIN
101	GND	b 1
102	L	b 7
103	TMD	b 2
104	RCD	b 3
106	CTS	b 5
108	DTR	b 7
105	RTS	b 4
109	DCD	b 8
107	DSR	b 6

CH. B

DCE 1:1
Cnormal()

PMU 80-3V

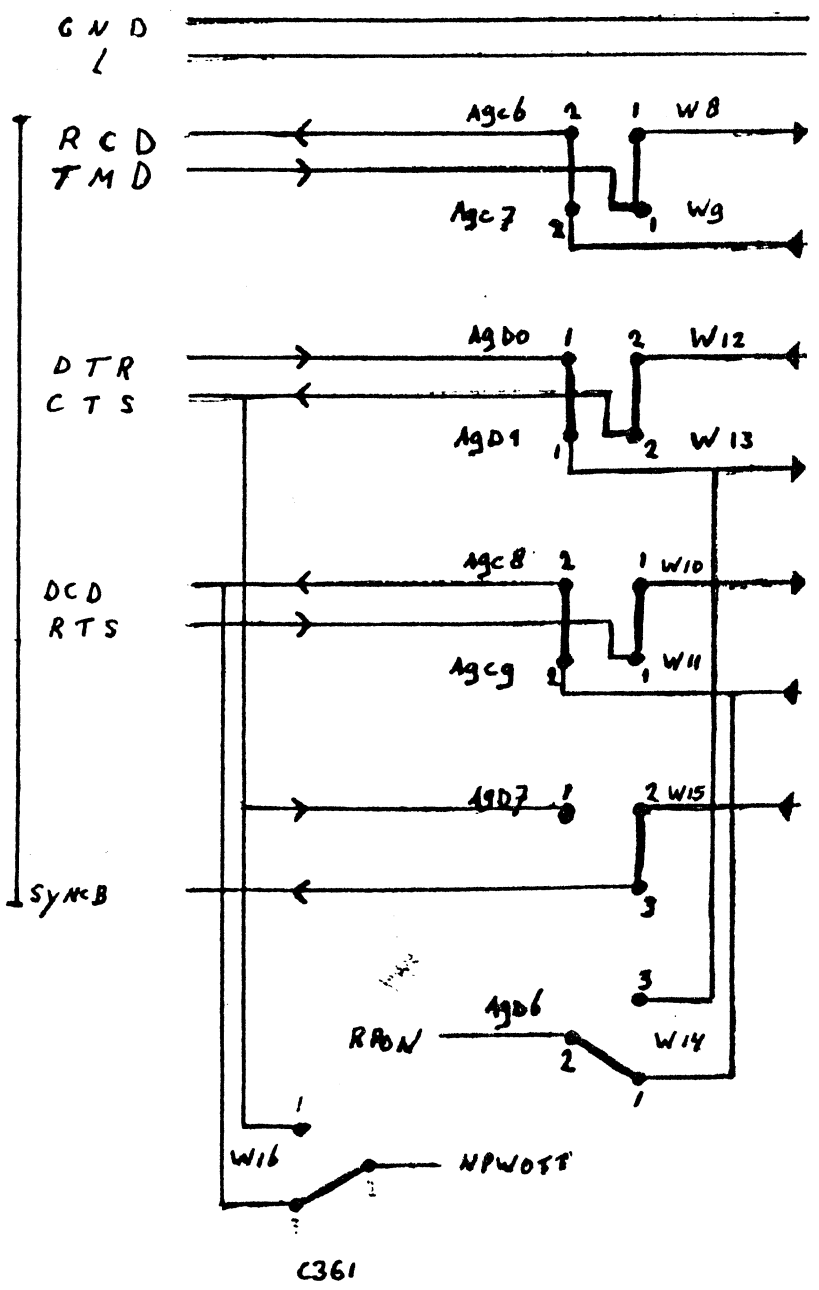


CC ITT	NAME	PIN
101	GND	b1
102	L	b7
103	TMD	b2
104	RCD	b3
106	CTS	b5
108	DTR	b7
105	RTS	b4
109	DCD	b8
107	DSR	b6

CH B

PMU 80-3V

DTE



CCITT	NAME	PIN
101	GND	b1
102	L	b7
103	TMD	b2
104	RCD	b3
106	CTS	b5
108	DTR	b7
105	RTS	b4
109	DCD	b8
107	DSR	b6

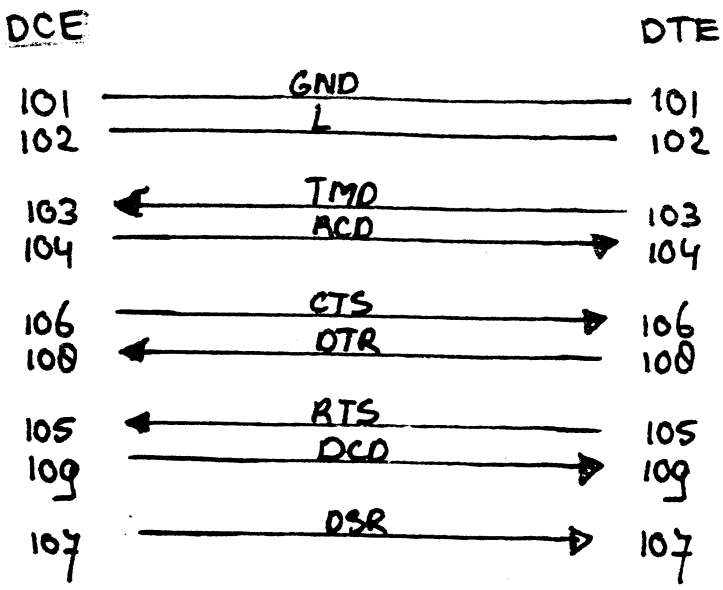


figure 1

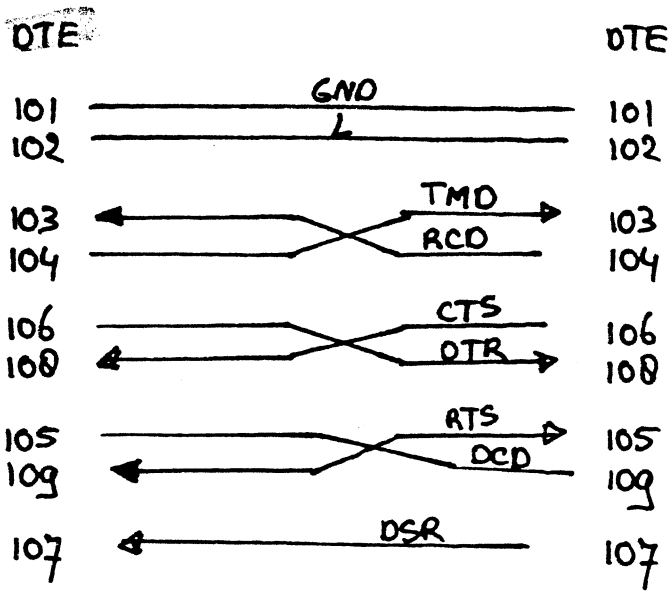


figure.2

TMD TRANSMITTED DATA
RCD RECEIVED DATA
CTS CLEAR TO SEND
DTR DATA TERMINAL READY
RTS REQUEST TO SEND
DCD DATA CARRIER DETECTED
DSR DATA SET READY

PMU 8013
Channel B

Strap	DCE (1:1) CSLAVE)	DTE	Master	
W 8	1-2	offen	1-2	103
W 9	1-2	offen	1-2	109
W 10	1-2	offen	1-2	105
W 11	1-2	offen	1-2	109
W 12	1-2	offen	1-2	106
W 13	1-2	offen	1-2	108
W 14	2-3 RPON über 108	1-2 RPON über 109	offen	108, RPON
W 15	1-2	2-3	1-2	107
W 16	1-2 NPWOFF über 108	2-3 NPWOFF über 105	1-2	108, NPWOFF

6. DATA BUS CONTROL

The function of this circuit is to control the times at which the processor's data lines, DATP0-7 are connected to the Local data bus DATL0-7. Connection is achieved via the tranceiver at H0E2.

The transceiver is enabled if the signal ADRD (Address disable) is inactive (low). The direction of data flow is controlled by the signal NDATPD (Data Processor Direction). When NDATPD is low data flow from the data bus to the processor, and when NDATPD is high data flow is from the processor to the data bus.

The decoding of the signal NDATPD is performed by the PLA circuit (G4C0) as follows:

NDATPD is low (active) when:

```
- BACKL    = 0
- NIORCL   = 0              IO Read
or
- BACKL    = 0
- NINTACK  = 0              Interrupt Acknowledge
or
- BACKL    = 0
- NMRCL    = 0              Memory Read (Except the Rom)
- NROME    = 1
```

7. INTERRUPT CONTROL

The Interrupt Control Logic contains:

a. Z8536-CIO (H7E3) (Counter/timer and Parrallel I/O Unit) which is capable of handling eight different interrupts lines, and the Real Time Clock.
b. Interrupt acknowledge circuit (B0B7,I6D5).

The Z8536-CIO contains three I/O ports and three counter/timers

	ADDRESS
I/O Port A: Input port for eight different interrupt lines.	23
I/O Port B: Input port (Discussed by Local I/O Port)	20
I/O Port C: Reserved	21
C/T 1 : Reserved	
C/T 2 : Real Time Clock Generation	
C/T 3 : Reserved	

For a detailed description of the operation of this chip reference should be made to the data sheets. However several aspects of the chip are now explained.

Port A is capable of handling upto eight different interrupts, but at the moment only six are used. The various lines are allocated as follows:

NIR0 - Power Failure (PWFNI) Highest Priority
NIR1 - Interrupt Fifo (INTFIFO)
NIR2 - Master Slave Interrupt (NIRCMD)
NIR3 - Power Off (NPWOFF)
NIR4 - SASI Port
NIR5 - Reserved
NIR6 - Reserved
NIR7 - Flexible Disk Controller Lowest Priority

The line PWFNP (Power Failure Supply) is an output from the power supply. If a power failure occurs this line goes low.

The lines INTFIFO and NIRCMD (Interrupt Command) are outputs from the MASTER SLAVE COMMUNICATION. They will be activated when the master processor (on the master PMU80-3), wants to interrupt the slave.

NPWOFF (Power Off) is an output from the V24 interface connector. If the terminal is switched off, this line is activated.

Note: The lines NIR4-7 are buffered at (H0F3). Reserved for master.

All the lines at the input of Port A will be programmed as level triggered, active zero inputs.
If an interrupt occurs on any of the input lines, then the line NINT (Interrupt) is activated.
Bit 7 has the highest priority, bit 0 the lowest. The interrupt vector is allowed to include status information (indicates the highest priority bit, which causes the interrupt).
So, an unique interrupt vector is released when the interrupt acknowledge signal is activated.

The remaining lines of the CIO have the following functions:

NCSCIO (Chip Select CIO)
When active this signal permits the CIO to be read or written.

IEOS (Interrupt Enable Out SCC)
The Z8536-CIO and Z8530-SCC are connected in a daisy chain, which gives the Z8530-SCC the highest interrupt priority. When IEOS is high, it indicates that no other device with a higher priority is requesting an interrupt.

ADRL1, NADRL0
These lines are used to select the I/O Ports and the internal Control register.

The signal M1 is gated (at H7D2) with NCOMDIS to create the enabling signal for the interrupt acknowledge control (at B0B7,I6D5).

Interrupt Acknowledge sequence. (fig. 1.)

After the line NINT is activated, the processor will response with.

a. A special NM1 cycle
b. NMRQ will stay inactive high.
c. INTACK (output 5 of flip flop B0B5) is activated on the rising edge of NPRCLK
d. T2 (output 8 of flip flop B0B7) is activated
e. With T2 active high, NINTACK is activated.
f. At the fourth clockpulse of TCLK, NIORPE (output of gate H7D2 pin 11) is activated, as well as NCIORD. At this moment the CIO puts his interrupt vector on the data bus.
g. At the fifth clockpulse of TCLK NXACKL becomes active low. As a result of this, on the rising edge of NPRCLK the processor deactivates NM1.

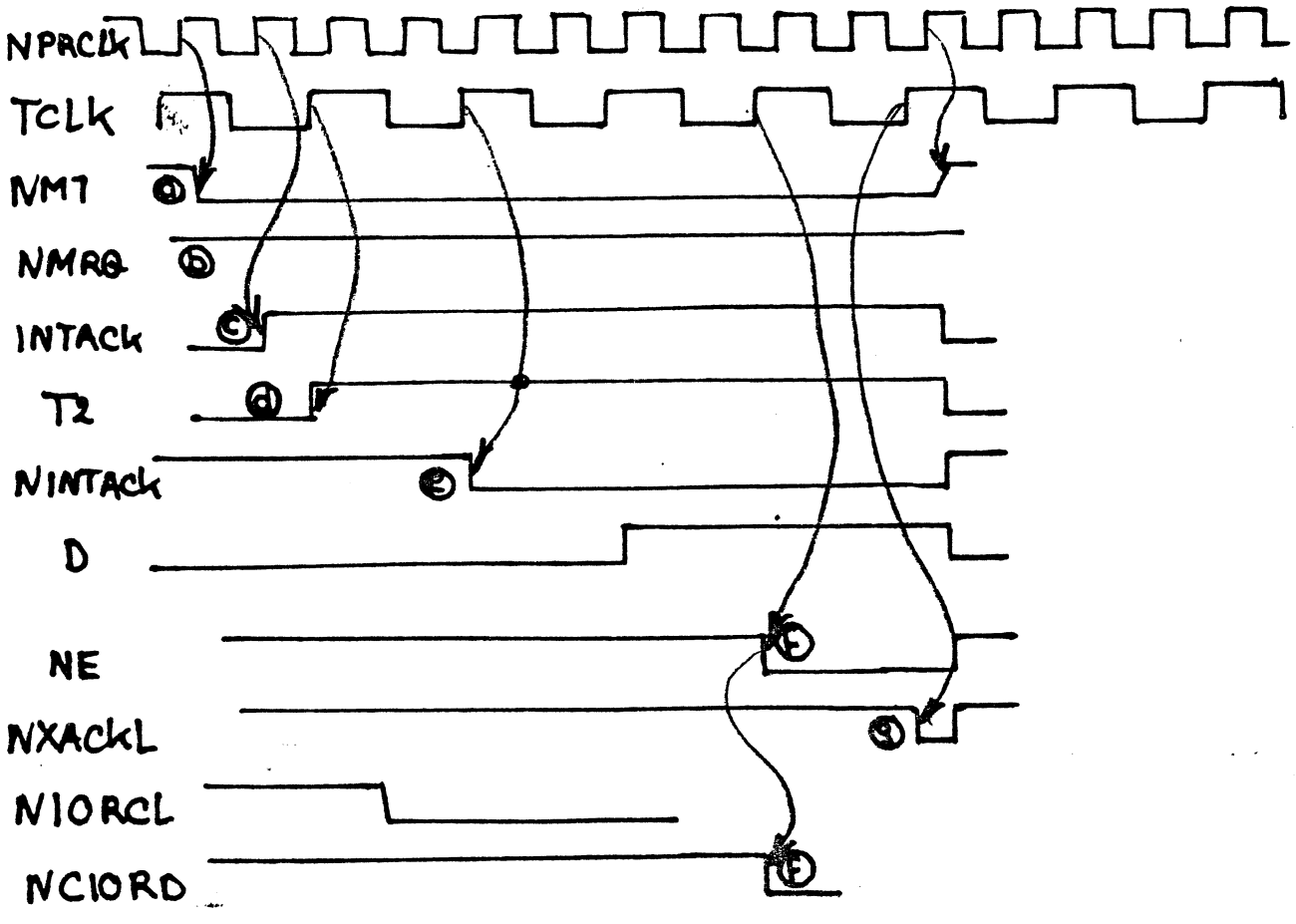


figure 1.

Remark:The CIO is reset by activating NCIOWR and NCIORD at the same time.

Real Time Clock Generation shall be performed by Counter/Timer 2.
It consits of a presettable 16 bit down counter, a 16 bit time constant register, an 8 bit current counter register, an 8 bit mode specification register and an 8 bit command status register.

All this registers are accessable by the CPU performing I/O commands to the

appropriate I/O addresses.

8. LOCAL IO DECODER

The decoding is performed by the PROM on Location E6C5. The Prom is enabled when the signal NIOL (Input/Output Local), from the PLA circuit F2C0, goes low. This signal is activated under the following conditions:

ADRL6 = 0
ADRL7 = 0
BACKL = 0

This results in a local IO address range of 00 - 3F.

After it has been selected, the PROM decodes the address lines ADRL2-6, to the following addresses:

LINE		ADDRESS
NCSSCC	(Chip Select SCC)	00 - 03
NCSIOP	(Chip Select IO Port)	20
NCSCIO	(Chip Select CIO)	20 - 23
NCSMMU	(Chip Select Memory Map Unit)	24
NMSCP	(Master Slave Communication Port)	28
NCSFIFOL	(Chip Select Fifo Local)	2C

All of these chip select lines are active when low.

9. MEMORY MAPPING

The memory mapping circuit is used to extend the number of processor addres line from sixteen to twenty, so that instead of being able to address only 64K of memory, the processor is able to address upto 1M.

Memory accesses can take four basic forms (see below). To fully explain the operation of this circuit, each type of memory access is explained. However, before proceeding with the explanation, the following important points should be noted:

a. The signals EXMAC (External Memory Access), and MAPEN (Map Enable), are set or reset by the "on board" processor, via OUTPUT PORT 20
b Throughout the following description reference is made to the ZSEG Buffer, and the MMU Port. These are the components located at G6E2 and G2D2, respectively.
c. The logical address, refers to address output of the processor.
d The physical address, refers to address of the memory location in the physical memory map.
e. The signal NMMUEN, when active, enables the MMU Port.

NMMUEN is active (Low) when:

- ADRP13-15 = 0 (System Memory or IPL Rom Access)
- BACKL = 0 (Logical addres 1000-1FFF)
- ADRL12 = 1
- MAPEN = 1

Note: BACKL = Bus Acknowledge Local

The circuit operates as follows:

(i) Access to TEST ROM.(Figure 2)

With EXMAC and MAPEN both 0 (after power on) and the logical address between 000 and FFF, the ZSEG Buffer and MMU Port are disabled. When the ZSEG Buffer is disabled the address lines ADRL19-12 are all high. Therefore, a logical address in the range 000-FFF is translated into a physical address in the range FF000-FFFFF. A hardware test program is located between these addresses.

Note: The ZSEG Buffer is disabled when the signal NZSEGDIS or the signal NADRD (Address Disable) is active (low), i.e. when:

- ADRP12-15 = 0 Test Rom access
- EXMAC = 0 (logical address 000-FFF)
- MAPEN = 0
- BACKL = 0

(ii) Access to IPL ROM. (Figure 3)

The test program is executed upto logical address 0FFF. During this program, the processor writes an "address adjuster" byte with the value FE into the MMU Port. At the end of the inside test an instruction which sets MAPEN to 1 is executed.
The next logical address output by the processor is 1000. With EXMAC=0, MAPEN=1 and a logical address in the range 1000-1FFF, the MMU Port is enabled and translated into a physical address of FE000. A logical address in the range 1000-1FFF is translated into a physical address in the range FE000-FEFFF. The IPL routine is located between these addresses.

Note: The ZSEG Buffer is disabled when NZSEGDIS is active (low), i.e. when:

- ADRP13-15 = 0 (IPL ROM access)
- EXMAC = 0 (logical address 1000-1FFF)
- BACKL = 0
- ADRP12 = 1
- MAPEN = 1

(iii) Access to Local Ram. (Figure 4)

With the lines EXMAC=1 and MAPEN=0, the ZSEG Buffer is enabled and the MMU Port is disabled. The upper four address lines (ADRL19-16) are set to 0, while ADRL0-15 take up the value of the lines ADRP0-15. A logical address in the range 0000-FFFF will be translated into a physical address of 00000-0FFFF. This represents the RAM area of the PMU80-3.

(iv) Access to System Ram (DC node PMU80-3 or master PMU80-3 only). (Figure 5)

With EXMAC=1 and MAPEN=1, and a logical address in the range 1000-1FFF, the ZSEG Buffer is disabled and the MMU Port is enabled. The "address adjuster" byte written into the MMU Port by the processor (and hence present on ADRL19-12) has two functions.

a. ADRL19-16 carries the number (0-15) of the slave PMU80-3, the processor is accessing.
b. ADRL15-12 carried the page number (0-15) of the slaves memory.

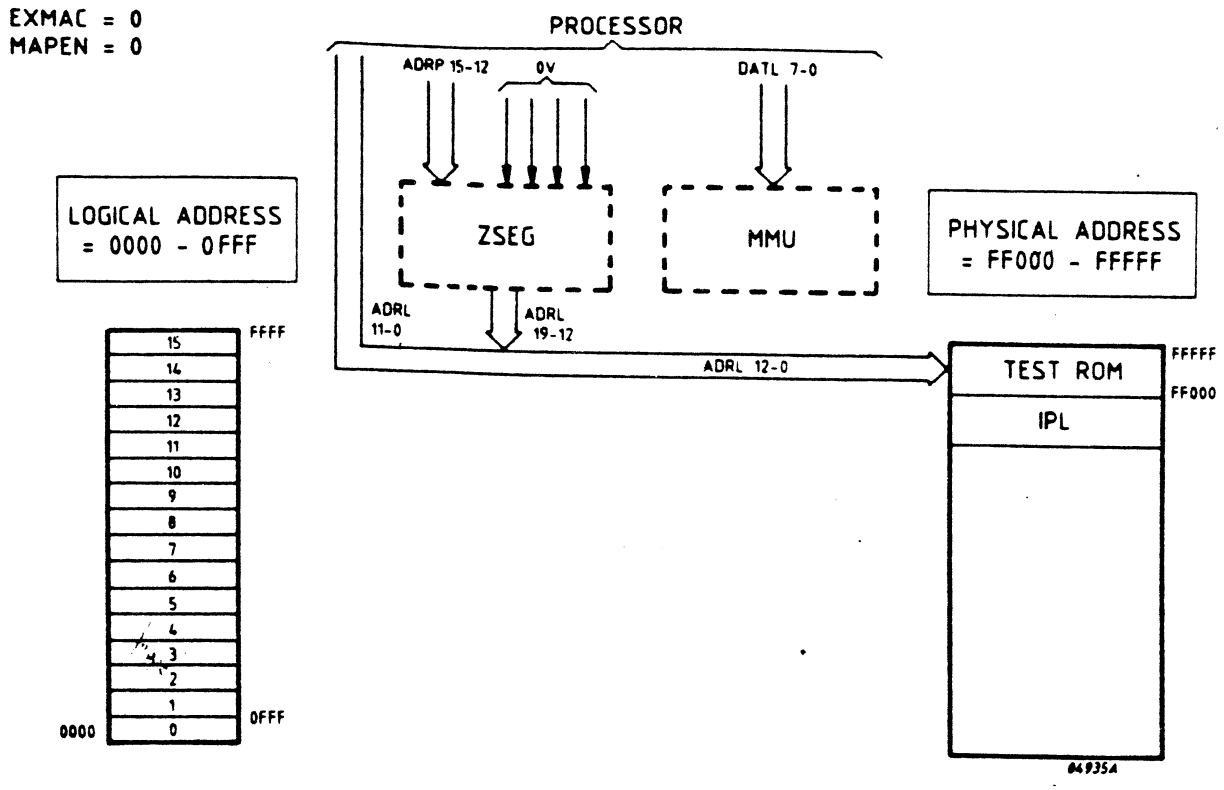


Figure 2. TEST ROM ACCESS

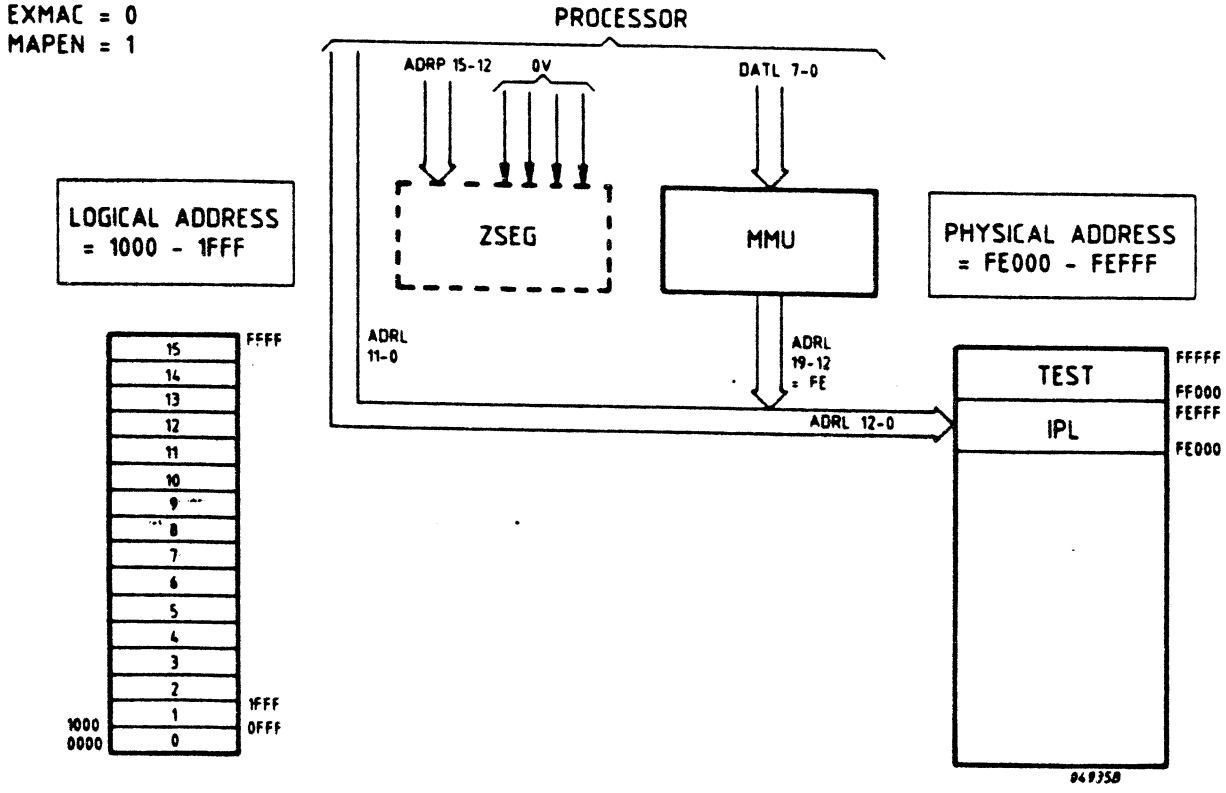


Figure 3. IPL ROM ACCESS

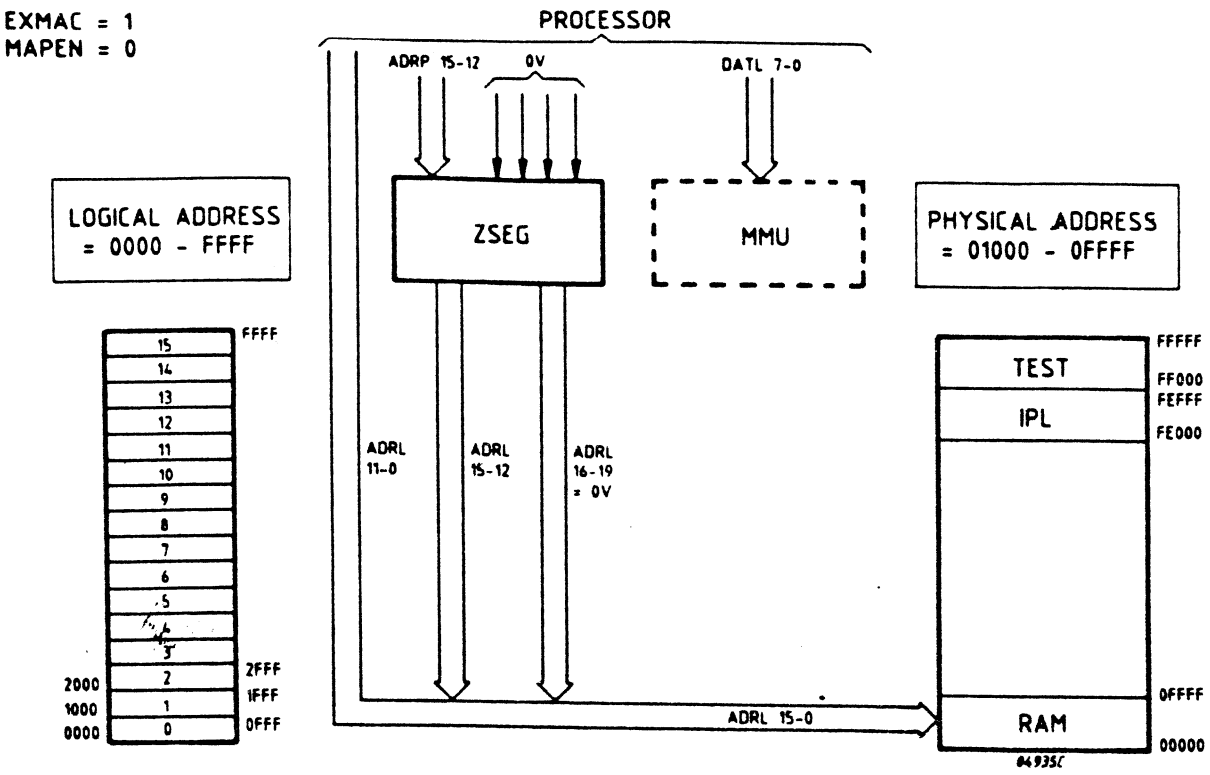


Figure 4. Local RAM Access

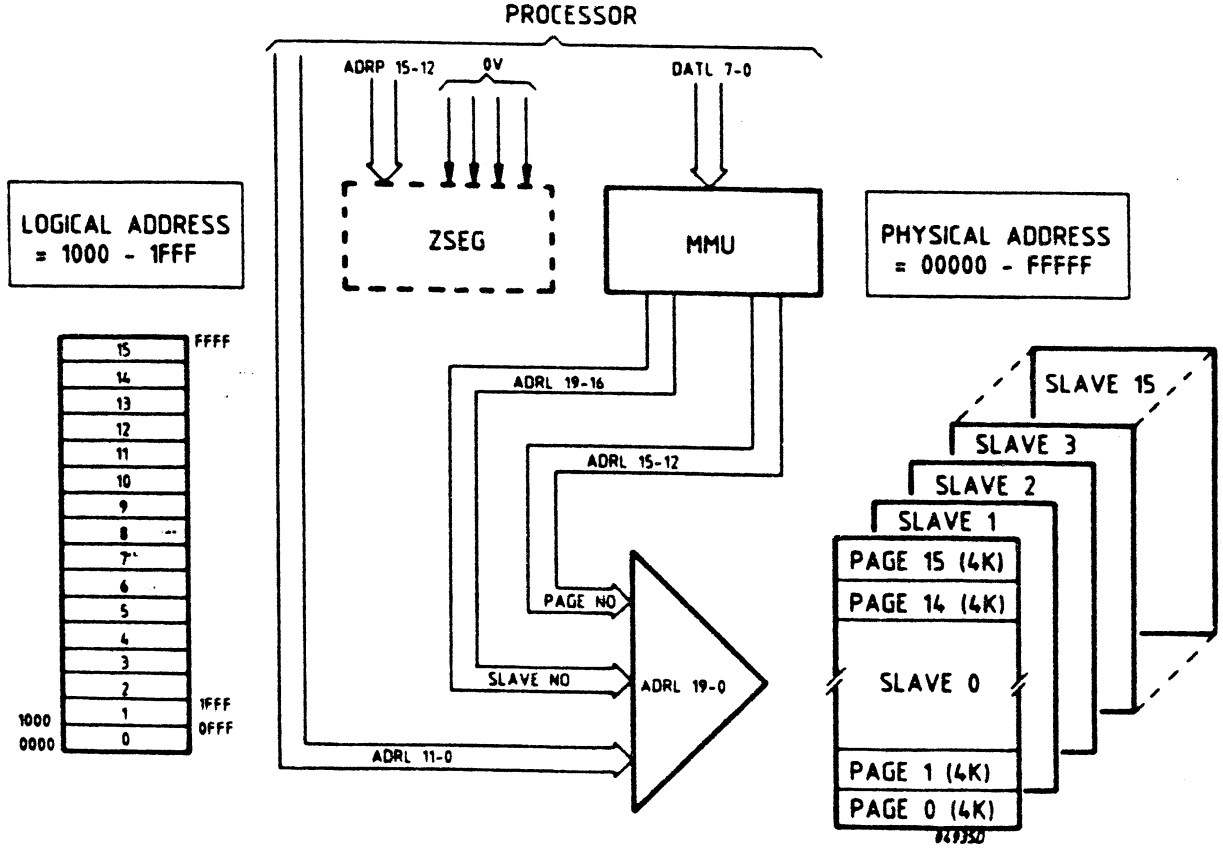


Figure 5. SYSTEM MEMORY ACCESS

Note: The 64K of Ram on each slave is divided into 16, 4K pages, numbered 0-15. The ZSEG Buffer is disabled when NZSEGDIS is active (low), i.e. when:

- ADRP13-15 = 0 (System Memory Access)
- BACKL = 0 (logical address between 1000-1FFF)
- ADRP12 = 1
- EXMAC = 1
- MAPEN = 1

The address lines ADRL11-0, carry the address of the memory location within the 4K page (with 12 address lines it is possible to access 4K).

10. ADDRESS BUS CONTROL

With the bustranceivers E7E4 and D5E4 the addresslines ADRP11-0 are connected to the addresslines ADRL11-0. This is only in the case of ADRD (Address Disable) inactive (low).

11. MASTER SLAVE COMMUNICATION

Each PMU80-3 has some facilities to support the interprocessor communication. These are: Master Slave Control Port
Networking FIFO
Both can be used alternatively. FIFO processing is only used if all PMU boards are able to perform FIFO processing.

To select a certain PMU board, the following comparison must be made. The inputs to the comparator (H6C0) are formed by the signals (SLL0-3) (Special Logic Lines), and NADR1-4 (Address Lines 1-4), both of which are lines from the EMM Bus. The levels of the lines SLL0-3 depend on the slot position of the various PMU cards within the system cabinet. The address lines (ADR1-4) are activated by the master when it wishes to acces a slave. The lines are compared in the comparator in the following manner:

NADR1 - SLL0
NADR2 - SLL1
NADR3 - SLL2
NADR4 - SLL3

If the comparison between all of these lines is successful, the the line CS is activated (high).

(i) Master Slave Control Port

The Master Slave Control Port is an input for a slave.
Data is clocked into the register on the rising edge of NCTRPSTB.
NCTRPSTB is active low, when:

NADR0	= 1	Master IO Write to an address in the range 40-5F
NADR5	= 1	
NADR7	= 1	41 - file master
NDACK1	= 1	43 - slave 1
CS	= 1	45 - slave 2
NADR6	= 0	till
NIOWC	= 0	5F - slave 15

Note: NDACK1 = DMA Acknowledge 1. (Not used) The address lines are inverted at the EMM bus.

The inputs of the register are connected to the EMM data lines (NDAT0-7). At the moment, only three lines have a function:

NDAT0 - Master Reset (active high)
NDAT1 - IPL Request Reset (active high)
NDAT2 - Master-Slave Interrupt (active low)

The Master-Slave Interrupt line (NDAT2), is in fact unimportant on the output of the register. It is sent, in parallel, to a D flip flop (I6F4), where it is clocked in on the rising edge of the signal NCTRPSTB.
If NDAT2 is low (active), the interrupt line (NIRCMD), to the INTERRUPT CONTROL circuit, is activated. (active low)

During the Master-Slave Interrupt Service Routine, the Slave can reset the NIRCMD line by generating an IO Write Command (NIOWCL) to the Master Slave Control Port.(28H) The active address of the control port causes the signal NMSCP(Master Slave Control Port) to be activated by the LOCAL I/O DECODER. NIOWCL and NMSCP (D0D5), active together, reset the D flip flop, and hence NIRCMD. A Master reset (NMR) also resets the flip flop.
When the data on the lines NDAT0-7 is clocked into the register I2C8, the transfer acknowledge signal NXACK is generated and sent back to th acessing device.

(ii) Networking FIFO

The Z8060 First-In First-Out (FIFO) is an input for the master. The FIFO (K0C0) on master can only be written by a slave. On the Local Bus the FIFO is only readable. Data transfers in the FIFO are only from port A (NDAT7-0) to port B (DATL7-0).

Before data can be written in the FIFO, the signal NFIFOSCS (FIFO)) must be activated. With NFIFOSCS is low, the shiftregister at K0F2 is enabled. NFIFOSCS is active low, when:

NADR5	= 1	I/O write to an address in the range 40H-5FH.
NADR7	= 1	
NDACK1	= 1	40 - file master
CS	= 1	41
NADR0	= 0	43 - slave 2
NADR6	= 0	44
NIOWC	= 0	

With the signals RFD (Ready For Data), output of the FIFO, active high and NDACK1 inactive (high) ,the shiftregister clocks in a "1" at the rising edge of NBCLKI. On the next clockpulses always a "1" is clocked in.
At the third clockpulse NACKA (Acknowledge Port A) is activated (low), which means for the FIFO that the input data (NDAT7-0) is valid.
The interrupt line INTFIFO ,to the INTERRUPT CONTROLLER, is now activated.

After the fifth clockpulse the transfer acknowledge NXACK is generated and sent back to the accessing device.
The shiftregister is reset when NFIFOSCS is deactivated.

With the signal NCSFIFOL (Chip Select FIFO) is active low, the contents of the FIFO (Byte by byte) can be read when NIORCL is activated. The interrupt line INTFIFO is activated as long as the FIFO is not empty.

NXACK is also generated after a write or read of the master in the slave memory. NMACK (Memory Acknowledge) (K0E4) is activated by the MEMORY TIMING during a read or write cycle.

12. WAIT STATE GENERATOR

This circuit is used to force the processor into "wait mode" if the speed of the processor is too fast with regard to the accessed device. Device accesses can take two forms, either a memeory access (system or local), or an I/O acces (system or local). At the start of a memory access, the signal NMRQL goes low, and at the start of an I/O access the signal NIORQL.

With no device access ocurring (NMRQL and NIORQL both high) the REQ line is low. This causes the counter I2F5 continually loaded with the value 13H on the inputs. Therefore he never counts out. At the same moment the counter I2E7 stays in the reset mode. The transfer acknowledge local signal (NXACKL), at this time will be inactive (high).
NXACKL is input to the PLA circuit at G4C0 and affects the condition of the NRDY (Ready) line, as follows:
NRDY is active (low) when:

- NXACKL = 0 Local Access
- BACKL = 0

or

- NXACK = 0 System Access
- BACKL = 0
- BUSCON = 1

With NWAIT low, the processor is in "wait mode", and will remain so until

- NRDY = 0

or

- NMACK = 0
- ADRD = 0

1. Memory Access (see figure 6)

a. NMRQL is activated.
b. NMRQL active, puts REQ active.
- When REQ is low, the counter (I2F3) is continuously loaded with the value on his pre-set inputs (inputs 3-6), and the counter I2E7 is in reset state. When REQ goes high, the counters start their counting action.
c. RIOTOUT goes high on the second rising edge of PRCLK.
d. At the third count of PRCLK, and then after each sixteenth count of PRCLK the counter I2E7 is incremented by one until it reaches the value 128.
e. TOUT becomes active after 1028 clock cycles of PRCLK.
- TOUT activates both NXACKL and NRDY.

2. Input/Output Access (see figure 7) (Not by a INTACK sequence)

f. NIORQL (and hence IOLREQ), is activated.
g. NIORQL active, puts REQ active.
h. RIOTOUT goes high on the second rising edge of PRCLK.

3. ROM Access (see figure 8)

j. NMRQL is activated
k. NMRQL active, puts REQ active.
l. RIOTOUT goes high on the second rising edge of PRCLK.
m. RIOTOUT and ROME (both high) both active, activate NXACKL and NRDY.

Another kind of device access that can put the processor into "wait mode", is when a processor, acting as a master, accesses a slaves control port, FIFO, or memory.
During this type of action the NRDY line can be activated when the accessed PCB activates the NXACK line.

The MEMORY TIMING generates the signal NMACK.

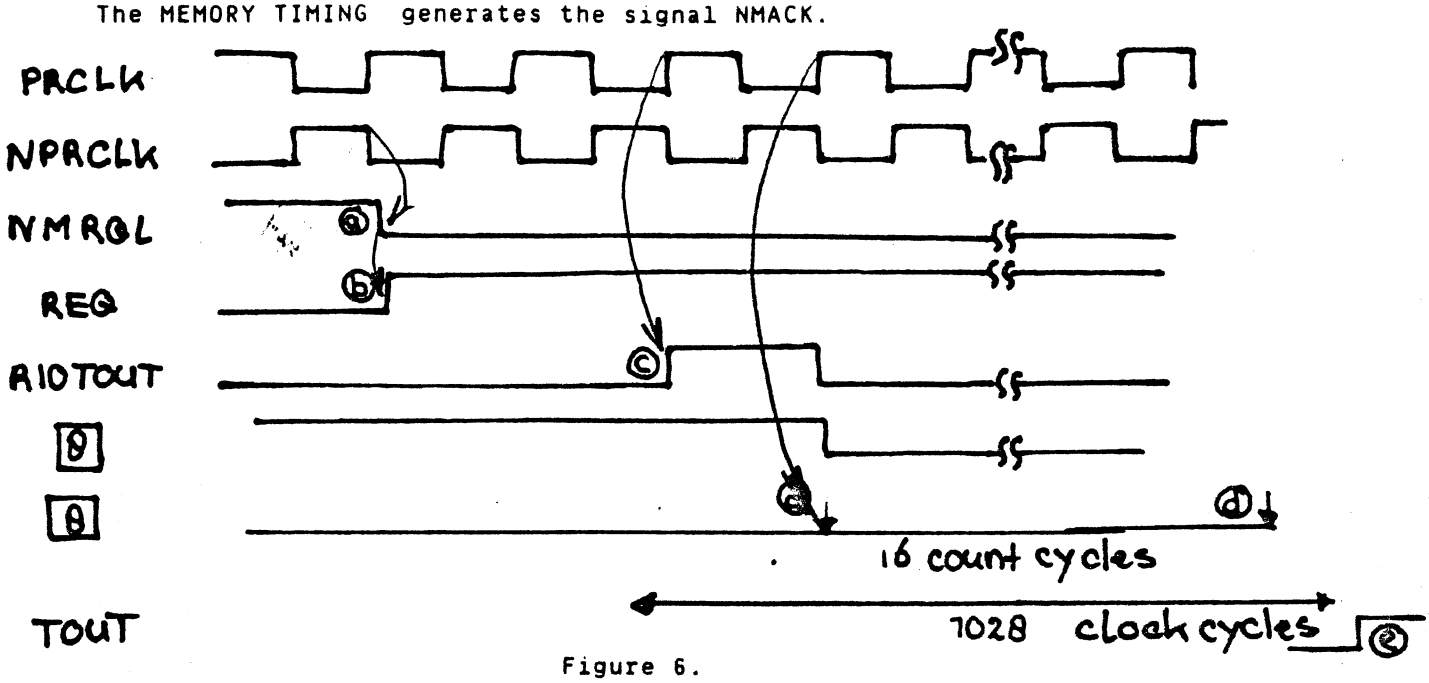


Figure 6.

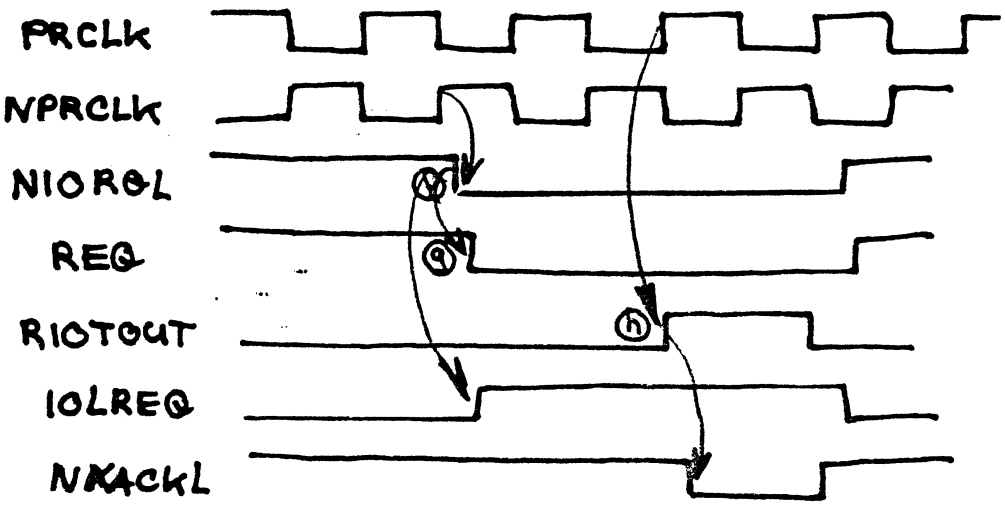


Figure 7.

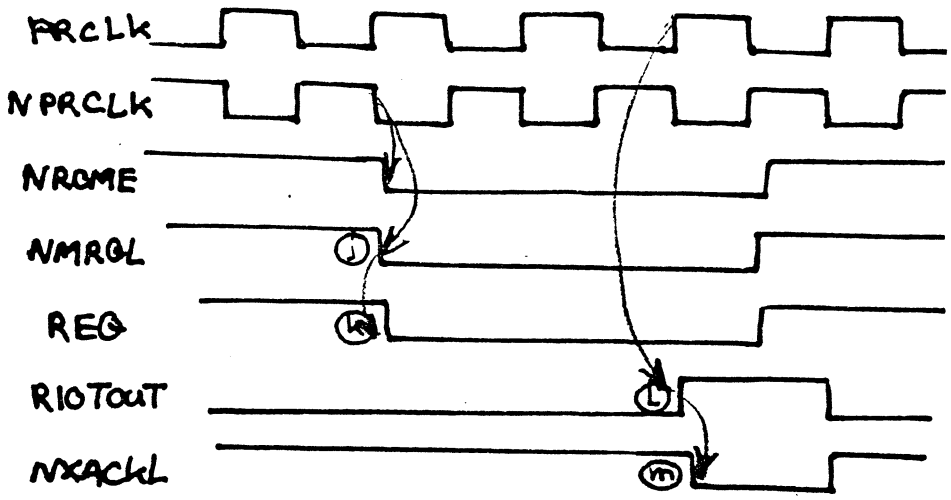


Figure 8.

13. RESET REFRESH LOGIC

The Reset Refresh Logic is used to perform the reset of the system at power-off or power down, and the RAM refresh cycles during normal processing and power down periods.
During normal processing the signals RSLN (Reset Line, from the power supply) and NMRS (Master Reset) are both inactive (high). NRES (Reset) therefore, is also high. As a result of this, both flip flops (B8B7) have a high level on their inputs. This is clocked in on the rising edge of RCLK (Refresh Clock), or the rising edge of NPRREF (Processor Refresh).
NMRI and STBMUX (Strobe Multiplexer) become high. (With STBMUX high, the RAS signals to the memory are supplied by the memory timing.)
At the same time the level of the reset line (NMR) (B4B7) is inactive (high).
The signal RCLK is fed to a gate at B4A3 (pin 2), where it is blocked while NMRI is high. STBREF therefore, stays low all the time.

NPRREF (Processor Refresh) is active when the signal NRADRE (Refresh Address Enable is inactive high.

NPRREF is gated (B4A3 pin 8) with MR to produce the signal PRREF.
This signal directly generates the signal COUNT (B4B7 pin 12) which is fed to the REFRESH COUNTER in the ADDRESS MULTIPLEXER circuit as the synchronised RAM refresh clock.
With NRADRE (Refresh Address Enable) is active low, NREFSHA (pin 9 of flip flop D8C6) is activated at the rising edge of NPRCLK. The signal MUXRM (C2C6) fed to the ADDRESSMULTIPLEXER is low, which means that there is a new refresh address available.
NPRREF (pin 6 of flip flop D8C6) is activated. NPRREF causes in the MEMORY TIMING a RAS signal.
When NPRREF returns to his inactive state, the REFRESH COUNTER is incremented.

The signal NRADRE is active low, when:

```
   NPACC  = 0          Refresh internal access
   NM1    = 0
   NCONT1 = 0
   NRASD  = 1
   NRADRE = 1
or
   NPACC  = 0          Rom or external access
   NM1    = 0
   NRASD  = 0
   BACKL  = 0
   NCONT1 = 1
```

If one or both, of the lines RSLN , NMRS go low, then NRES goes low as well. As a result of this, the flip flop output line NMRI also goes low.
NPRREF therefore is blocked by the high condition of the line MR.
The signal COUNT is output to the REFRESH COUNTER at the frequency of RCLK via gate B4A3.
When PONRES (genereated by the circuit around B0A9) is active low, then RCLK is fed to the refresh counter as well.
During "power on", the circuit tests the supply
voltage and keeps the output PONRES active low, as long as the supply voltage has not reached his nominal value.
Also when the supply voltage drops under the nominal value PONRES is active.

14. MEMORY TIMING

The purpose of this circuit is to control the times at which the PMU80-3 memory is accessed. Memory accesses can take the following forms:

(i) Local RAM access: where the processor is accessing its on-board RAM.
(ii) System Ram access: where a master processor is accessing a slave memory
(iii) Local RAM access: for refresh purposes.
(iv) ROM access: where the processor is accessing its on-board ROM.

Memory access timing for the PMU80-3 is performed by a PAL circuit, F1A8. The output signals from the PAL, NCONT1, NCONT2, and NEXACC (Externally Access) are the main signals to achieve correct address timing.
The signals NRASD (Row Address Strobe Disable) and NRADRE (Refresh Address Enable) are important for the refresh cycle.

Note: The signal NCONT1 is an internal feed back.

The first signal that must be generated is the signal RAS (Row Address Strobe), output of gate D4C6 pin 8.
RAS is disabled when the signal NRASD (Row Address Disable) is active.

NRASD is active during:

ADRP12 = 0		Test ROM Access
ADRP13 = 0		
ADRP14 = 0		
ADRP15 = 0		
BACKL = 0		
EXMAC = 0		
MAPEN = 0		
or		
ADRP12 = 1		IPL ROM Access
ADRP13 = 0		
ADRP14 = 0		
ADRP15 = 0		
BACKL = 0		
EXMAC = 0		
MAPEN = 1		
or		
ADRP12 = 1		System Memory Access
ADRP13 = 0		
ADRP14 = 0		
ADRP15 = 0		
BACKL = 0		
EXMAC = 1		
MAPEN = 1		
or		
NCONT2 = 0		
or		
BACKL = 1		Memory accessed External

RAS is active:

(i) During a local R/W. NMRQL input of gate E7C4 activates NMRW (Memory Read Write) which activates RAS.

(ii) During a system R/W. The signal NEXACC (External Access) activates RAS. NEXACC is active (low) when:

NEXACC is active when:

```
BACKL  = 1          Memory accessed externally
NCONT2 = 1
RDWR   = 1
```

(iii) During a local Opcode fetch. The signal NPRREF (Processor Refresh) is activated during the refresh part of the NM1 cycle.
During a "power down" situation NPRREF also activates RAS.

NCONT1 (internal feed back into PAL) is active when:

```
   BACKL  = 0          Internal Access
   NPACC  = 0
   NRASD  = 1
   NCONT2 = 1
or
   NEXACC = 0          Accessed External
   BACKL  = 1
   NCONT2 = 1
or
   BACKL  = 0          Refresh
   NPACC  = 0
   NRASD  = 0
   NM1    = 0
or
   BACKL  = 0          Hold
   NPACC  = 0
   NRASD  = 0
   NM1    = 0
   NCONT1 = 0
```

NCONT2 is active when:

```
   NCONT1 = 0            Accessed External
   NEXACC = 0
   RDWR   = 1
   BACKL  = 1
or
   NCONT1 = 0            Internal Access
   NPACC  = 0
   NRASD  = 1
or
   NCONT2 = 0            Hold.  Accessed External
   RDWR   = 1
   BACKL  = 1
or
   NCONT2 = 0
   NPACC  = 0
   NRASD  = 1
```

RAS is fed to a multiplexer C2B6. During normal operation the signal STBMUX (Strobe Multiplexer) from the RESET/REFRESH LOGIC is low which means that RAS is connected to RAS1 and RAS2. These signals are sent to the RAM BANK. In the case of a power down situation STBMUX is actived, which means that STBREF (Strobe Refresh), output by the RESET REFRESH LOGIC is connected to RAS1 and RAS2.
During a refresh cycle, only the signals RAS1 and RAS2 need to be supplied to the RAM BANK.

RAMACC (Ram Access) and RAS are activated at the same time. The lower addressbyte is clocked into the RAM. After a delay of several ns, RAMAC1 (B6C6) is activated.
With both RAMAC1 and RAS active, MUXM (Multiplex Memory) output of gate C2C6 is active. With MUXM active, the high order addressbyte is available on the RAM.

RAMAC2 is activated, when RAMAC1 already is active. RAMAC2 is fed to two gates (C6C6) where it is, depending on the signals A and B, connected via the multiplexer with the signals CASL (Colomn Address Strobe Low) or CASH to the RAM BANK. On CASL or CASH active, the high order addressbyte is strobed into the RAM.
CASL is active when B (output of ROM E7B4) is active.
B is active high when: ADRL15 = 0

CASH is active when A is active.
A is active high when: ADRL15 = 1

Other signals generated by the ROM are:

NOUTEN1 (Out Enable 1)

```
   NMRCL   = 0          Memory R/W.  Odd addresses
   ADRL0   = 1
or
   NMRQL   = 0          Memory R/W.  Even addresses
   ADRL0   = 0          (Only with NBHEN active)
   NBHEN   = 0
```

NOUTEN2 (Out Enable 2)

```
   NMRCL   = 0           Memory R/W.  Even Addresses
   ADRL0   = 0
```

The signals WRENH (Write Enable High) and WRENL are active with NMRCL (Memory Read Command) is inactive.
WRENH is active when:

```
   NMRCL   = 1           Accessing Odd addresses
   ADRL0   = 1
   RAMACC  = 1
or
   NBHEN   = 0           Accessing Odd/Even addresses
   NMRCL   = 1
   RAMACC  = 1
```

WRENL is active when:

```
   ADRL0   = 0            Accessing Even adsresses
   NMRCL   = 1
   RAMACC  = 1
```

All these signals are fed to the RAM BANK.

NBUSE (Bus Enable) fed to the SYSTEM BUS CONTROL is active with N8HEN = 1

Besides the memory timing signals another signal is generated by the PAL. This signal NMACK (Memory Acknowledge) is sent to the local processor, during a local RAM acces, to indicate that the memory is ready to accept the command. During a system RAM acces it is sent (via the MASTER SLAVE COMMUNICATION) to the accessing device, for the same reason.

NMACK is active when:

```
   NPACC   = 0            R/W cycle
   BACKL   = 0
   NM1     = 1
   NRASD   = 1
or
   NPACC   = 0            Opcode Fetch
   BACKL   = 0
   NCONT1  = 0
   NM1     = 0
   NRASD   = 1
or
   NCONT2  = 0            Accessed External
   BACKL   = 1
   RDWR    = 1
or
   NPACC   = 0            Hold
   BACKL   = 0
   NMACK   = 0
```

15. RAM BANK

The RAM BANK consits of eight 16k4 memory chips with each time two chips in parallel to form an 8 bit data output. We will call this a pair.
The Ram Bank is in such a way organized, that there are two parts of 32k.
PART1: This part is selected by odd addresses, (with N8HEN = 0 also by even addresses which we will discuss later).
This part is formed by two pairs. We call them:
P1LP (Part 1 Lower Pair,chips D4A3,D8A3) addressable between 0000-7FFF odd /(even) addresses
P1HP (Part 1 Higher Pair,chips E2A3,E6A3) addressable between 8000-FFFF odd /(even) addresses
With NOUTEN1 (Out Enable 1) is inactive high, the output buffers DATL8-15 will stay in the high impedance state.

PART2: This part is selected by even addresses, and also formed by two pairs which we will call:

P2LP (Part 2 Lower Pair,chips B8A3,C2A3) addressable between 0000-7FFF even addresses.

P2HP (Part 2 Higher Pair,chips C6A3,D0A3) addressable between 8000-FFFF even addresses.

With NOUTEN2 is inactive high, the output buffers DATL0-7 will stay in the high impedance state.

In normal operation NBHEN is inactive high. At this moment during Ram access, when an odd address is on the address bus, the lines DATL8-15 are connected to DATL0-7 in the circuit. With NBHEN is active low a 16 bit master PMU can access the memory (seen as 32K words) with data on the lines DATL0-15.
PART1 and PART2 are then in parrallel, and only addressable on even addresses.

Although the addressing capability is 16K, only eight address lines are available on each chip. The fourteen bit address (to address 16K) must be supplied to the memory in two parts. Hence, one need for the ADDRESS MULTIPLEXER.
The eight low order address bits are placed on the addrees bus MADR0-MADR7, and clocked into the chips on the falling edge of the signal RAS1 (Row Address Strobe) for PART1, and RAS2 for PART2. RAS1 and RAS2 are supplied at the same time.
Then the six high order bits are placed on the address bus. There are two situations:

(i) An address between 0000-7FFF.
The address is clocked in on the falling edge of CASLP. (Colomn Address Strobe Lower Pairs).

(ii) An address between 8000-FFFF.
The address is clocked in on the falling edge of CASHP. (Colomn Address Strobe Higher Pairs).

The signals NWEL (Write Enable Low) for PART2, and NWEH (Write Enable High) for PART1 are used to indicate whether a read or write action is required. With NWEL or NWEH, high, indicating a read action, and low indicating a write action.

All these controll signals are supplied by the MEMORY TIMING circuit.
Because the memory chips are dynamic, refresh cycles must be performed at least once every 2ms (milliseconds). During refresh, the address is strobed into the memory on the falling edge of the signal RAS1 and RAS2. Only a eight bit address (representing 256 row addresses) is necessary, because the complete 64K can be refreshed in 256 cycles.

16. ADDRESS MULTIPLEXER

The address multiplexer consists about five multiplexers, and 2 counters.
Four Multiplexers (C686,D086,D486,D886) are of the type:dual 4 line to 1 line multiplexer.
There can be made a selection between, Refresh address, low order addressbyte and high order addressbyte.
Selection is achieved using the signals:

MUXRM	MUXM	
0	0	Refresh Address
0	1	Refresh Address
1	0	Lower addressbyte
1	1	Higher addressbyte

MUXRM selects between Refresh Address and Memory Address
MUXM selects between Low and High order addressbyte.

The multiplexer used at E2C5 is used to solve some timing problems. With ADRD (Address Disable) is active high, ADRP11-0 is disconnected from ADRL11-0 in the ADDRESS BUS CONTROL. Even so ADRP14-12 must be disconnected from the local processor. Normally it was done in the MEMORY MAPPING circuit, but with the gate at F1D4 it is delayed with several ns.
To prevent this, ADRP14-12 is directly disconnected with the multiplexer F2C5.

The purpose of the refresh counter (D0C6) is to supply an incrementing refesh address to the multiplexer. The counter is incremented by the signal COUNT (an output from the RESET REFRESCH LOGIC).
The refresh counter counts from 0-255, with the second half of the counter clocked by the signal REFA4. It should be noted that the complete 64K can be refreshed in 256 refresh cycles.

17. DATA HIGH/LOW CONNECTION

This circuit is used to transfer DATL15-8 to DATL7-0. NMRCL determines the direction of DATA.
This bus tranciever is enabled, with NBUFOE (Buffer Out Enable), under the following conditions:

NBUFOE is active low when:

```
ADRL0  = 1          Memory seen as 64K bytes
RAMACC = 1
N8HEN  = 1
```

During Local processing (ADRD is inactive low) N8HEN is inactive.
When the memory is accessed by another PMU, in the case of a 16 bit PMU, this memory can accessed as 32K by 16 bits (word). N8HEN is then active low.

18. ROM

The ROM used on the PMU80-3 is a single 8K chip containing an IPL (Initial Programm Loader) routine, and a hardware test program. The test program is located in the first 4K (address 000-FFF), and the IPL routine in the second 4K (1000-1FFF). The "in-system" memory address for the ROM is FE000-FFFFF.
To enable the ROM, the signal NROME (ROM Enable) must be active (low). It is active low when:

```
NZSEGDIS = 0
EXMAC    = 0
NMRCL    = 0
```

19. LOCAL I/O PORT

All PMU's have an I/O Port. By reading the input port the processor can determine the state of several status lines. And by writing the output port the processor can activate several condition lines.
The input port, (Port B of the Z8536 located at H7E3) is selected when the signal NCSCIO (Chip Select CIO) is activated.
The output port (C2E4) is selected when the signals NCSIOP (Chip Select CIO) and ADRL1 active low. With the output of K0D5 going active low the contents of the databus is clocked into the port.

INPUT PORT (ADDRESS 20)

Bit 7 6 5 4 3 2 1 0

a) Data Set Ready (V.24 Interface).....1
a) Test Indicate (V.24 Interface).....1
a) Set Process active (Channel B).....1
b) Master Identification.....1
c) Remote Power On from serial Interface.....1
d) Memory Not Maintained.....1
e) No IPL requested.....1
c.f.e.....1

The data path polarity into the CIO is programmed as inverting.
a) NDSRA (Data Set Ready Channel A)
NTIA (Test Indicater Channel)
NPWOFF (Power Off)
b) NMAST (Master) Indicates that the PMU80-3 acts as a master.
c) NDCDA (Data Carrier Detected Channel A)
d) BARE (Battery was off Automatic Restart Enable)
Indicates that the memory was not powered up during the last system off time.
e) IPLRQ (IPL Request)
Master/Slave Control Port bit, indicating that an IPL has not been requested.

OUTPUT PORT (ADDRESS 20)

Bit 7 6 5 4 3 2 1 0

Test LED Off.....0
a) Remote Loop Back V.24 Interface.....1
a) Local Loop Back V.24 Interface.....1
c.f.e
b) System Memory Access enable.....1
b) Memory Mapping Unit enable.....1
c) Power Off.....1
d) reset 'Remote Power On'.....1

a) REML (Remote Loop)
a) LOCL (Local Loop)
These are control lines off the V.24 Interface.
b) EXMAC (External Memory Access)
MAPEN (Map Enable)
The combination of these two bits determine several modes of memory access as follows:

EXMAC (Bit 4)	MAPEN (Bit 3)	ACCESS
0	0	Inside Test ROM
0	1	IPL ROM
1	0	Local RAM
1	1	System RAM

c) NRPON (Remote Power On) This line when active, tells the system power supply to switch off.
d) RRPO (Reset Remote Power On) not used.

20. LOCAL BUS ARBITRATION

This circuit (PLA at F6C0), located at a slave, decides at which moment a master can access the slaves memory.
If a device wants to perform a system memory action, then on the selected slave happens follow:

a. The signal NLBRQI (Local Bus Request Intern) in the SYSTEM BUS CONTROL is activated.
b. With NLBRQI low, NLBRQX (Local Bus Request) is activated on the rising edge of PRCLK.
c. With NLBRQX active, NLBUSY is activated on the rising edge of PRCLK (in the case of the local processor is busy).
   NLBUSY (internal feed back in the PLA) is active when:

```
   NLBRQX = 0          Internal Opcode Fetch
   NMRQ   = 0
   NRFSH  = 0
   NSBRQI = 1
or
   NLBRQX = 0          Memory R/W
   NMRQ   = 0
   NM1    = 1
or
   NLBRQX = 0          Internal I/O
   NIORQ  = 0
   NM1    = 1
or
   NLBRQX = 0          Hold
   LBSY   = 0
or
   NLBRQX = 0
   NMRQ   = 0
   NM1    = 0
   NSBRQI = 0
```

d. After finishing action of local processor, NCOMST is activated.

   NCOMST is active when:

```
   LBSY   = 0          R/W
   NMRQ   = 1
   NIORQ  = 1
or
   LBSY   = 0          Hold
   NCOMDIS= 0
or
   NADRD  = 1          Hold
or
   LBSY   = 0          External Access
   NSBRQI = 0
```

e. With NCOMST activated, COMDIS (Command Disable) is activated at the rising edge of PRCLK.

f. After COMDIS is active NADRD (Address Disable) is activated.

NADRD is active when:

LBSY = 0
NCOMDIS= 0

g. The SYSTEM ADDRESS DRIVERS are enabled.
h. At the rising edge of PRCLK NSYSCEN (System Commands Enable) is activated.

Note: The signal NLBUSY is active as long as NLBRQX is active.
With COMDIS actice, BACKL (Bus Acknowledge Local) is inactive high.
The WAIT STATE GENERATER inserts wait cycles into the last instruction of the local processor.

21. SYSTEM BUS ARBITRATION

The Arbitration Logic is used by the master PMU80-3 to decide which device can have bus control when it is requested. In the slave PMU80-3's its only purpose is to supply the bus priority "daisy chain".

When the processor wants bus control, the line SBRQX (System Bus Request) gated at H7D2 with NCBRQ (Common Bus Request) becomes active high.
NSBRQX is an output of the PLA G8C0 and is active low when:

NSBRQI = 0 (System Bus Request)

If another device did already a bus request a low condition on the "J" input (NCBRQ is active low) at the flip flop D904 ignores the request for bus control. In the case of NCBRQ is inactive, the SBRQX is granted at the falling edge of NBCLKI.

Normally the master PMU80-3 will have bus control. This condition is indicated by the NBUSY signal (output to other devices, e.g. SESC0) in the active state (low).
The lines NINJ and NINK (outputs of the PLA G8C0) are inputs of the "JK" flip flop D9D4.

NINJ is active when:

NSBRQX = 0 Set Buscontrol
NBPRI = 0 (At the moment another device gives the bus free,if
NBUSY = 1 in use.)
CBRQX = 1

or

NMAST = 0
NBPRI = 0
NBUSY = 1
NCBRQ = 1

NINK is active when:

NCBRQ = 0
NSBRQX = 1

When NINJ becomes active low, then at the falling edge of NBCLKI, BUSCON (Bus Connected) is active high.

The line BUSCON is used (when active) to place the master commands on the EMM Bus.

If the SESCO (for instance) wants buscontrol, it puts the signal NBPRI (Bus Priority In) high. NBPRI is input to the PLA G8C0. NINJ is deactevated.
Is for example the master performing a system action, NINK is inactive (high), the "JK" signals on the flip flop are both zero, so the outputs of the flip flop remain stable.
Therefore, if no system action is in progress, NINK is activated.
A high condition on the "K" input of the FF, will cause the lines BUSCON and NBUSCON to be deactivated on the next falling edge of NBCLKI. BUSCON inactive (low), releases NBUSY and the requesting can take bus control.

At the rising edge of BCLKI the signal NCDMEN (Command Enable), a signal of PLA G8C0 is active low. This signal is fed through the SYSTEM BUS CONTROL to the SYSTEM BUS DRIVERS where it enables the drivers for the four command lines.

NCDMEN is active when:

NSBRQX = 0
NSBRQI = 0
BUSCON = 1

One gate, E3D4 (output pin 6), is present on every PMU80-3 to maintain the NBPRI "daisy chain" to other devices. If a device of higher priority requests bus control then the line NBPRI goes high. NBPRI going high, it puts the line NBPRO (Bus Priority Out) also high.
If the master wants to perform a system bus action, with the lines CBRQX and SBRQX both high, it also puts NBPRO high.

22. SYSTEM BUS CONTROL

The identification, whether a PMU80-3 is a file master or slave, is achieved using a gate (I2C0), which has the lines SLL0-3 as input. In the case of the file master PMU80-3, all of these lines will be high. NMAST is in that case low.

For the file master or DC Node to access the system memory, the signal NSYSMEN (System Memory Enable)from the PLA circuit F2C0, must be active.
NSYSMEN is active when:

ADRP13-15	= 0	(System Memory Enable)
BACKL	= 0	(Logical address 1000-1FFF)
ADRP12	= 1	
MAPEN	= 1	
EXMAC	= 1	

For an access to the system IO area, the signal NSYSIO (on the file master), from the same PLA circuit must be active.

NSYSIO is active (low) when:

```
   NMAST  = 0                 System IO - Filemaster only
   BACKL  = 0
   ADRL6  = 1
or
   NMAST  = 0                 System IO - Filemaster only
   BACKL  = 0
   ADRL7  = 1
or
   ADRL5  = 0                 System IO - Slave only
   ADRL7  = 0
   ADRL6  = 1
   NMAST  = 1
```

These two signals are connected to the PLA G4C0, where the signal NSBRQI (System Bus Request Internal) goes active low when the master wants to perform a system action.
NSBRQI is active when:

```
   NSYSIO = 0           Master: Write to system IO area
   BACKL  = 0
   NIOWCL = 0
or
   NSYSIO = 0           Master: Read from system IO area
   BACKL  = 0
   NIORCL = 0
or
   NSYSMEN= 0           Master: Memory write to slave
   BACKL  = 0
   NMWCL  = 0
or
   NSYSMEN= 0           Master: Memory read from slave
   BACKL  = 0
   NMRCL  = 0
```

With NSBRQI active low, the flip flop at D5D5 is enabled. So with NCDMEN is active low, the output on pin 9 is activated (active low) on the rising edge of NBCLKI, which means that the signal NSCOME (output 3 of H7D2) is also active low. This signal is fed to the SYSTEM BUS DRIVERS where it enables the driver for the command signals.

During a system memory access by the file master or DC node, all of the slave PMU80-3's will check wether the address on the EMM Bus is meant for them. This check is made by the comparator H2C0. It compares the slot position (On the EMM Bus) of the slave (lines SLL0-3) with the memory address (NADR16-NADR19). If the comparison is true, the signal LMS (Local Memory Select) is activated (high).
If this PMU is not accessing another device, the signal NLBRQI (Local Bus Request In) is activated.

NLBRQI is active low, when:

	PMU80-3	Action
BUSCON = 0	Slave:	Master writing to system (slave) memory
NMWC = 0		
LMS = 1		
or		
BUSCON = 0	Slave:	Master reading system (slave) memory
NMRC = 0		
LMS = 1		
or		
BUSCON = 0	Slave:	The signal NSLOCK (System Lock), a signal from
NLBRQI = 0		the EMM Bus, when active low, keeps the signal
NSLOCK = 0		NLBRQI active low.

With NLBRQI is low, the flip flop at D5D5 is enabled. At the rising edge of PRCLK the signal NLBRQX (Local Bus Request) at pin 6 is active low.

The direction in which data must be transferred is determined by the level of the signal NDATDIR (Data Direction). This is an output from the PLA (G0C0) and an input to the SYSTEM BUS DRIVERS.
When this line is low, data direction is from the EMM Bus to the PMU80-3, and when it is high, data direction is from the PMU80-3 to the EMM Bus.

NDATDIR is active (low) when:

	PMU Action:
BUSCON = 0	Master writing to system (slave) memory.
NMWC = 0	
LMS = 1	
or	
NMWC = 0	Master reading from system (slave) memory.
BUSCON = 1	
or	
NIORC = 0	Master reads system IO area.
NADR6 = 0	
BUSCON = 1	
NADR7 = 1	
or	
NIORC = 0	Master reads system IO area.
NADR7 = 0	
BUSCON = 1	

The following signals generated by the PAL (F6C0) are active low when:

NSYSCEN (System Command Enable) is active low, when:

NLBSY = 0	
NADRD = 0	

This signal gated at E3D4 with NLBRQX, both low, enables the driver for the command lines.

NSYSADE (System Address Drivers Enable) is active low, when:

NSBRQI = 0	PMU acts as a master.
BUSCON = 1	

or

NADRD	= 0	PMU is accessed by a master.
NLBRQX	= 0	

NDHBEN (Data High Bus Enable) is active (low) when:

NBUSE	= 0	PMU is accessed by a master
NADRD	= 0	memory acess with DATL15-0
NSYSCEN	= 0	
NLBRQX	= 0	

23. SYSTEM BUS DRIVERS

The drivers in this circuit form the interface to the EMM Bus. An interface which consists of:
- 4 command lines
- 20 address lines
- 16 data lines

24. COMMAND LINES

The command bus driver G0A8 is enabled when the line NSCOME (System Command Enable) is active (low).
The direction of the commands is set by the line BUSCON. If BUSCON is low, the direction is from the EMM Bus to the PMU80-3.

25. ADDRESS LINES

The driver G6A8 controls the direction of the high order address lines ADRL16-ADRL19. If the line NBUSCON is active (low), the address lines are from the PMU80-3 to the EMM Bus.
If the line NADRD is active (low), the address lines are driven low.(the driver inputs are inverted)

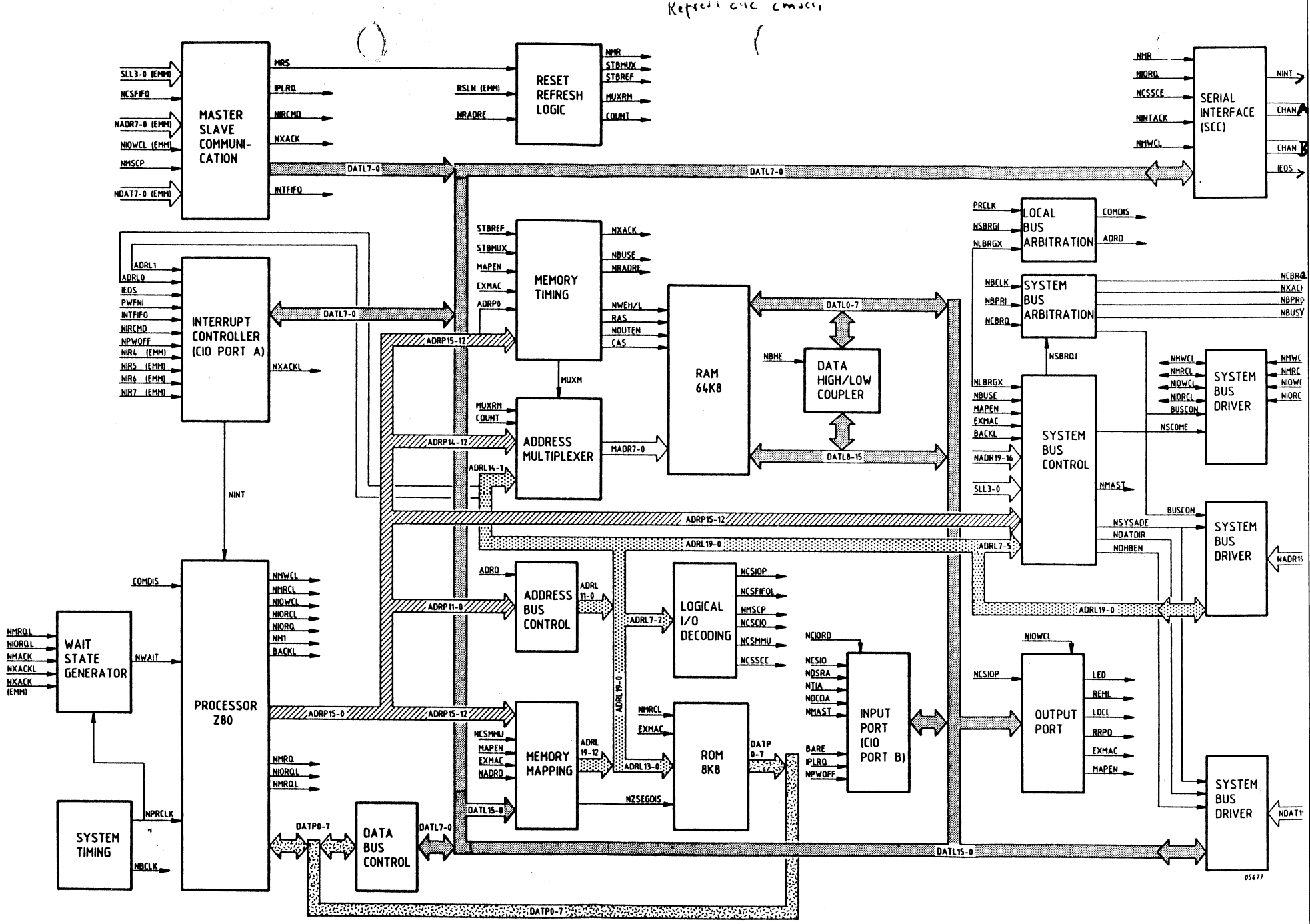
The low order address lines (ADRL0-ADRL15) are enabled when the signal NSYSADE (System Addresss Drivers Enable) is active (low).

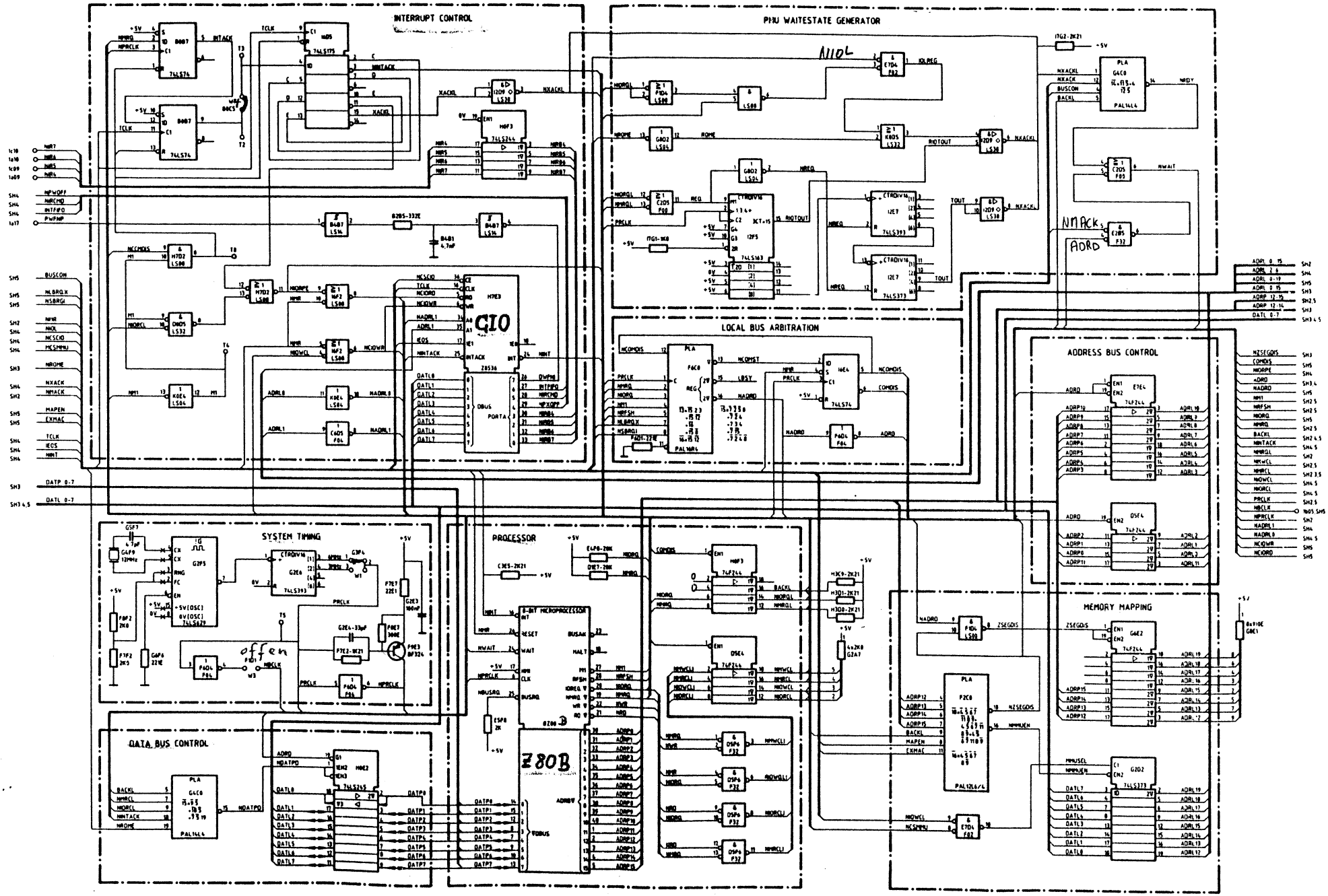
The address line direction is controlled by the signal BUSCON.

26. DATA LINES

The data lines are controlled by the drivers (I1A8,I6A8).
The direction of data transfer is controlled by the signal NDATDIR. A low level on this line enables transfer from the EMM Bus to the PMU80-3.

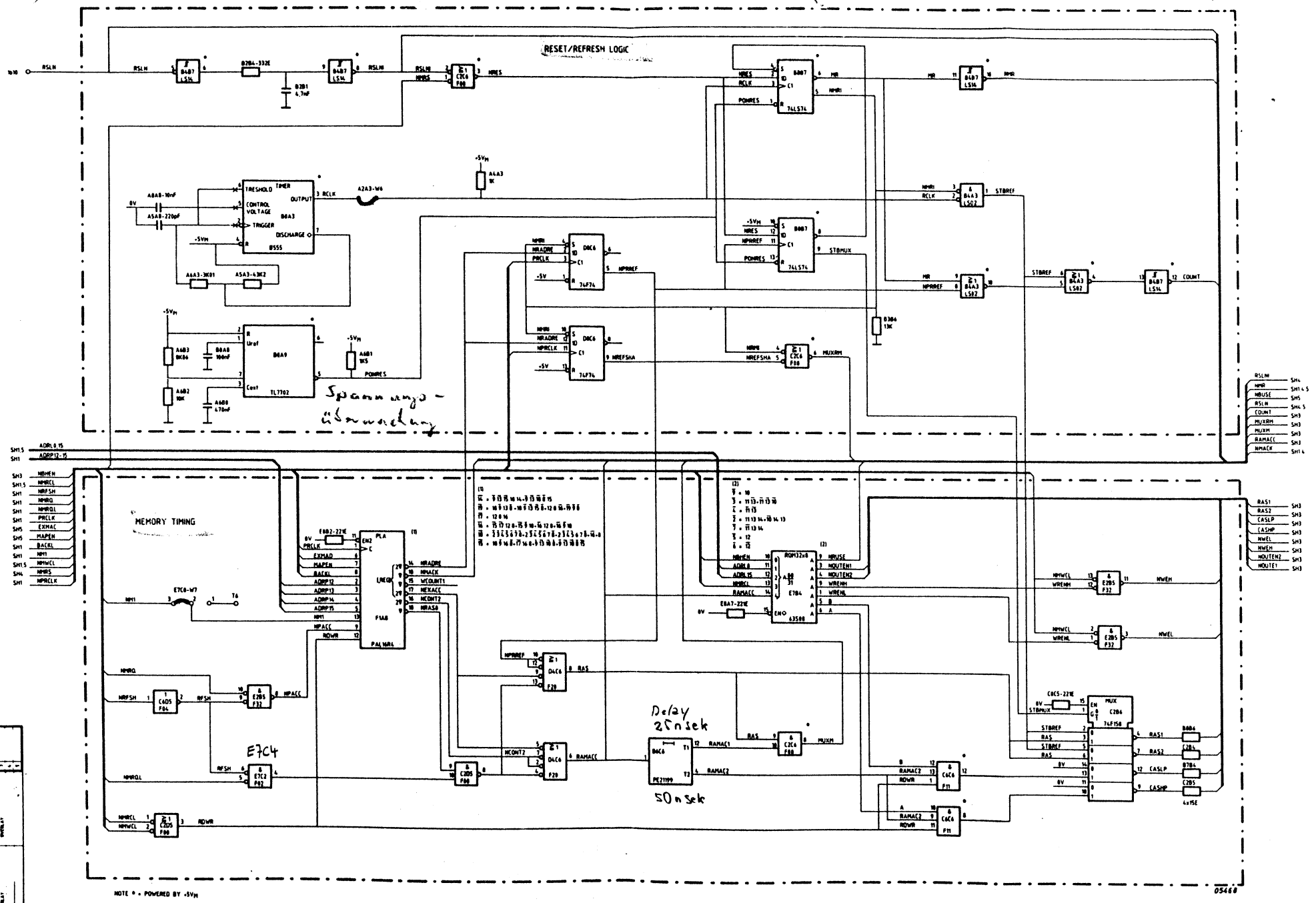
With NSYSADE active low, DATL7-0 can connected to the EMM Bus.
With NDHBEN active low, DATL15-8 can connected to the EMM Bus.


MASTER SLAVE COMMUNI-CATION
RESET REFRESH LOGIC
SERIAL INTERFACE (SCC)
INTERRUPT CONTROLLER (CIO PORT A)
MEMORY TIMING
RAM 64K8
DATA HIGH/LOW COUPLER
ADDRESS MULTIPLEXER
LOCAL BUS ARBITRATION
SYSTEM BUS ARBITRATION
SYSTEM BUS CONTROL
SYSTEM BUS DRIVER
PROCESSOR Z80
WAIT STATE GENERATOR
SYSTEM TIMING
ADDRESS BUS CONTROL
LOGICAL I/O DECODING
MEMORY MAPPING
ROM 8K8
DATA BUS CONTROL
INPUT PORT (CIO PORT B)
OUTPUT PORT
SLL3-0 (EMM)
NCSFIFO
NADR7-0 (EMM)
NIOWCL (EMM)
NMSCP
NDAT7-0 (EMM)
MRS
IPLRQ
NIRCMD
NXACK
INTFIFO
RSLN (EMM)
NRADRE
NMR
STBMUX
STBREF
MUXRM
COUNT
DATL7-0
DATL15-0
DATL8-15
DATL0-7
ADRL1
ADRL0
IEOS
PWFNI
NPWOFF
NIR4 (EMM)
NIR5 (EMM)
NIR6 (EMM)
NIR7 (EMM)
NXACKL
NINT
ADRP15-12
ADRP14-12
ADRP11-0
ADRP15-0
ADRL14-1
MUXM
MAPEN
EXMAC
ADRP0
NWEH/L
RAS
NOUTEN
CAS
NBUSE
NRADRE
NBHE
MADR7-0
ADRD
ADRL 11-0
ADRL19-0
ADRL7-2
ADRL7-5
ADRL 19-12
ADRL13-0
NCSMMU
NADRQ
NZSEGDIS
DATP 0-7
DATP0-7
NMWCL
NMRCL
NIOWCL
NIORCL
NIORQ
NM1
BACKL
NMRQL
NIORQL
NMACK
NXACKL
NXACK (EMM)
NWAIT
NPRCLK
NBCLK
COMDIS
NCSIOP
NCSFIFOL
NMSCP
NCSCIO
NCSMMU
NCSSCC
NCIORD
NCSIO
NDSRA
NTIA
NDCDA
NMAST
BARE
IPLRQ
NPWOFF
LED
REML
LOCL
RRPQ
EXMAC
MAPEN
PRCLK
NSBRGI
NLBRGX
NBCLK
NBPRI
NCBRQ
NSBRQI
COMDIS
ADRD
NCBRQ
NXACI
NBPRQ
NBUSY
NLBRGX
NBUSE
MAPEN
EXMAC
BACKL
NADR19-16
SLL3-0
NMAST
BUSCON
NSCOME
NSYSADE
NDATDIR
NDHBEN
NADR15
NDATT
05477

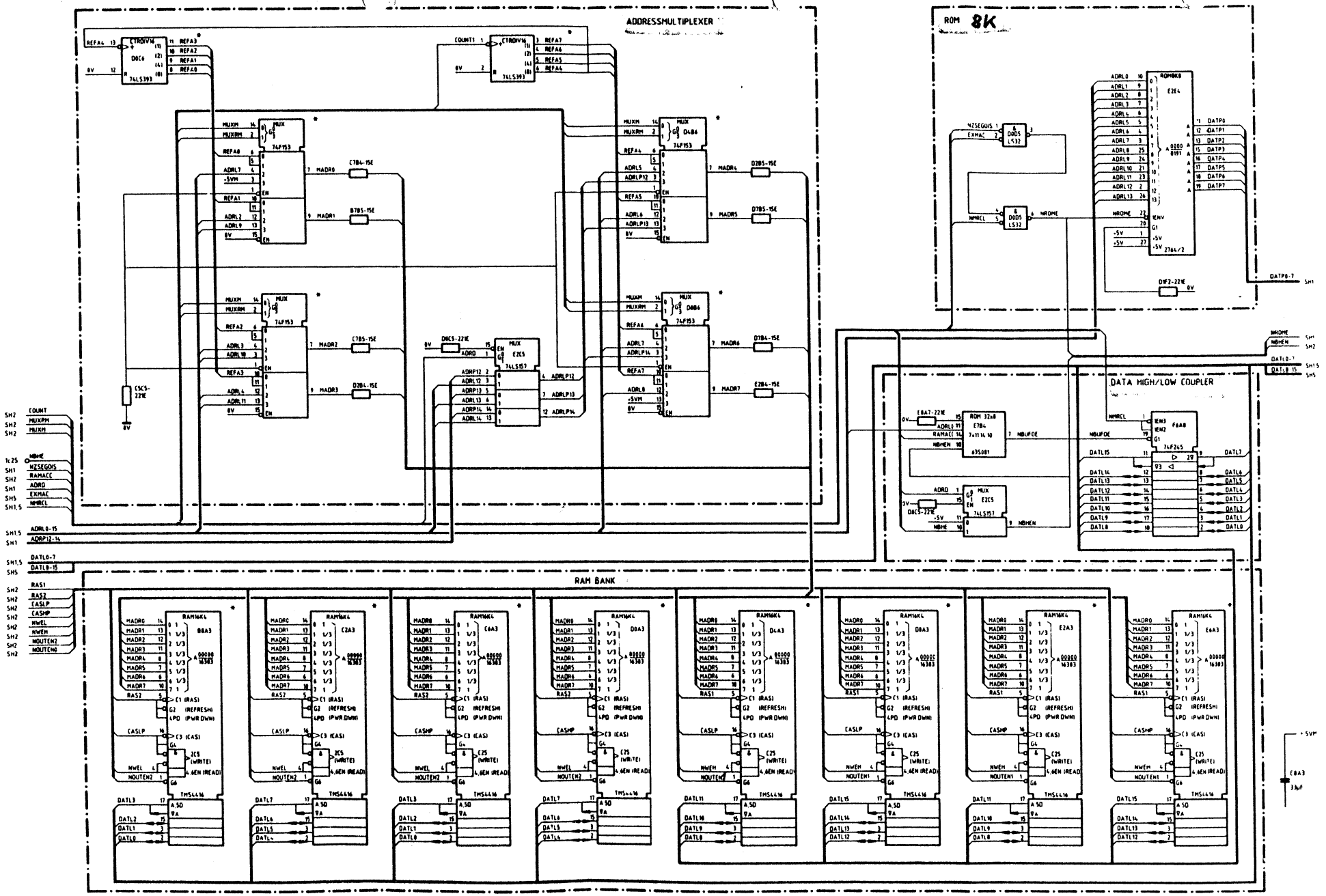

INTERRUPT CONTROL
PHU WAITESTATE GENERATOR
LOCAL BUS ARBITRATION
ADDRESS BUS CONTROL
SYSTEM TIMING
PROCESSOR
DATA BUS CONTROL
MEMORY MAPPING
CIO
Z80B
NMACK
ADRD

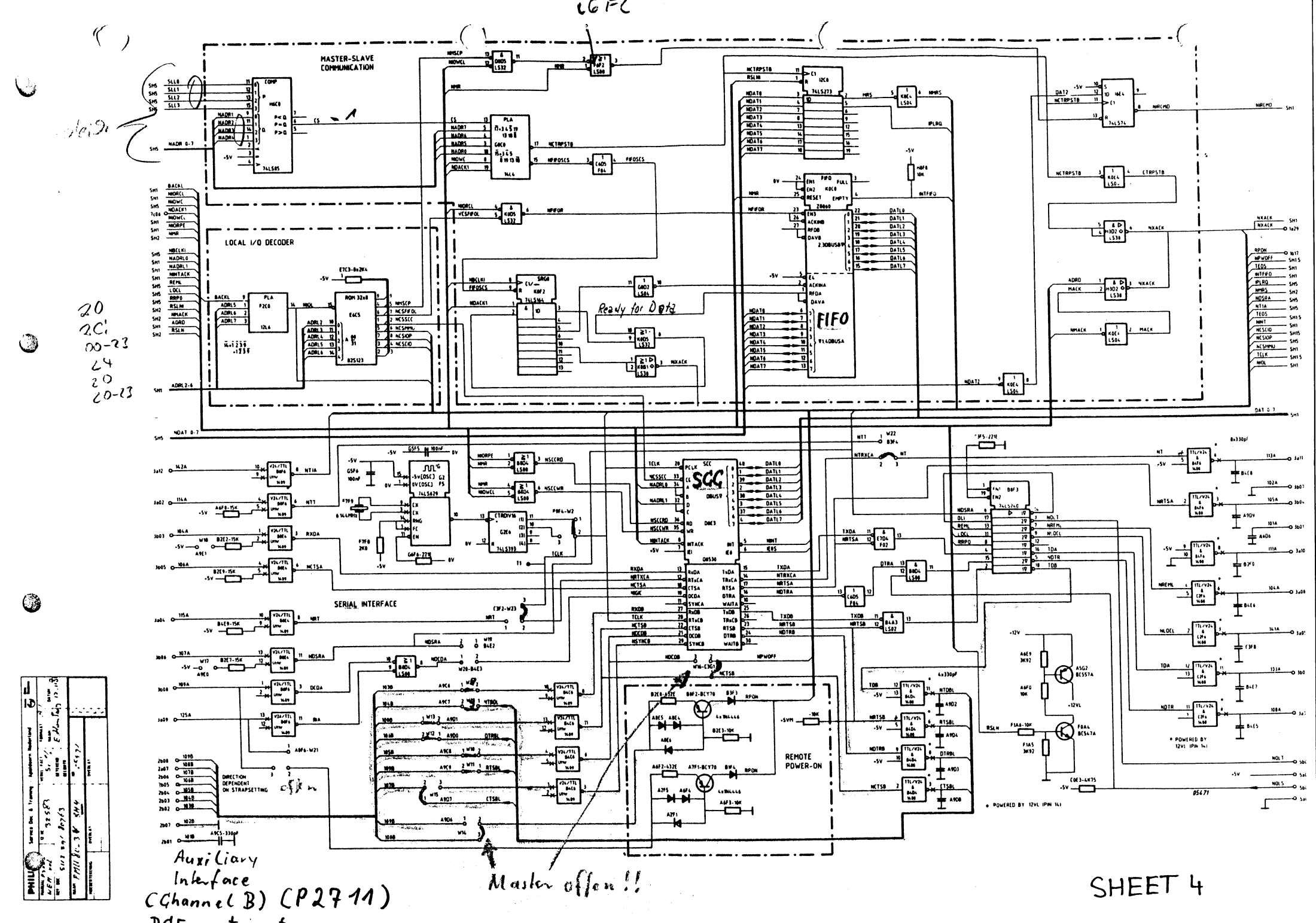
= NMR

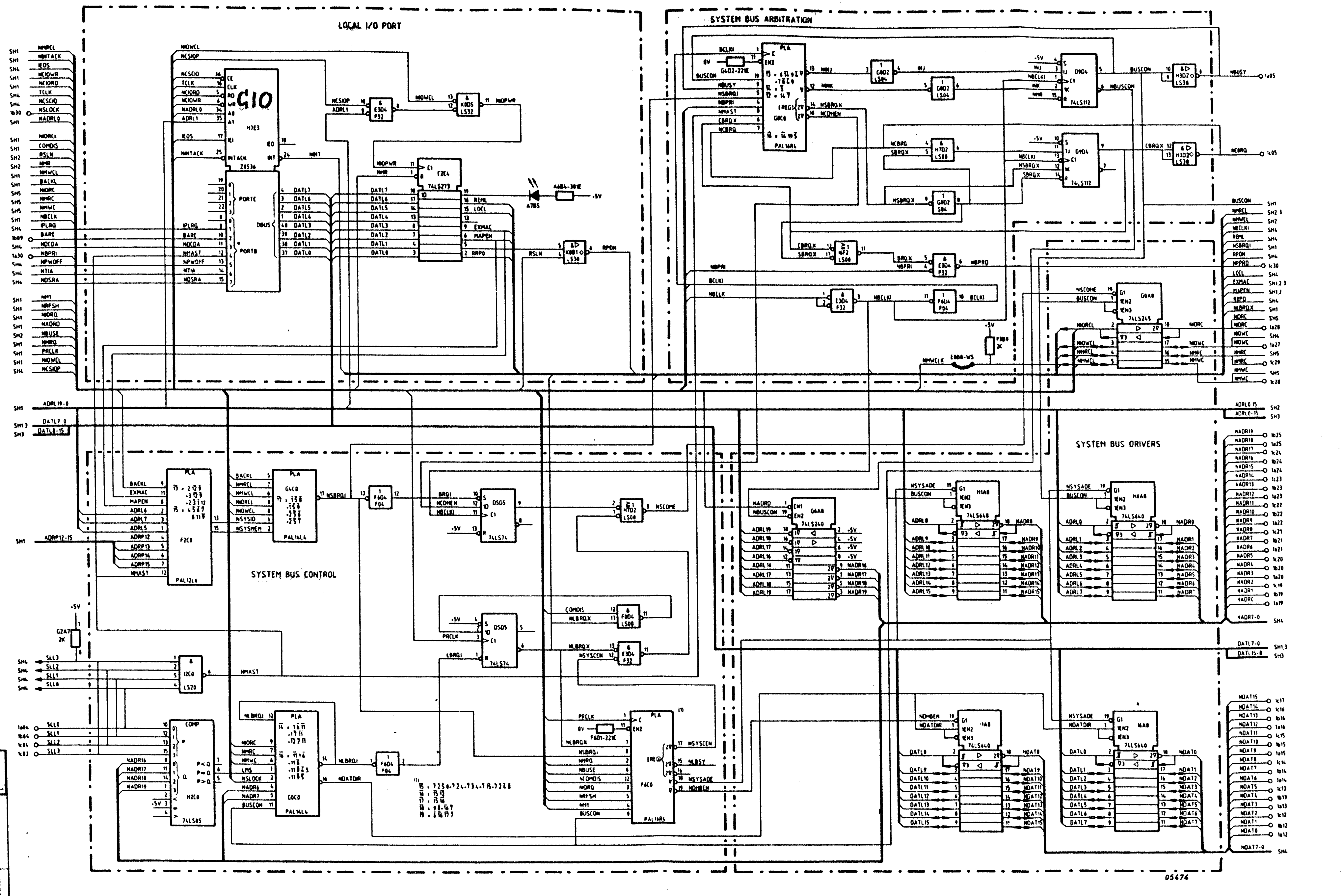
SHEET 1


RESET/REFRESH LOGIC
MEMORY TIMING
TIMER
TRESHOLD
CONTROL VOLTAGE
TRIGGER
OUTPUT
DISCHARGE
B555
TL7702
PLA
PAL16R4
ROM32x8
E7B4
MUX
C2B4
74F150
PE21199
Spaanungs-
überwachung
Delay
25 n Sek
50 n Sek
E7C4
NOTE * = POWERED BY +5VM
05468

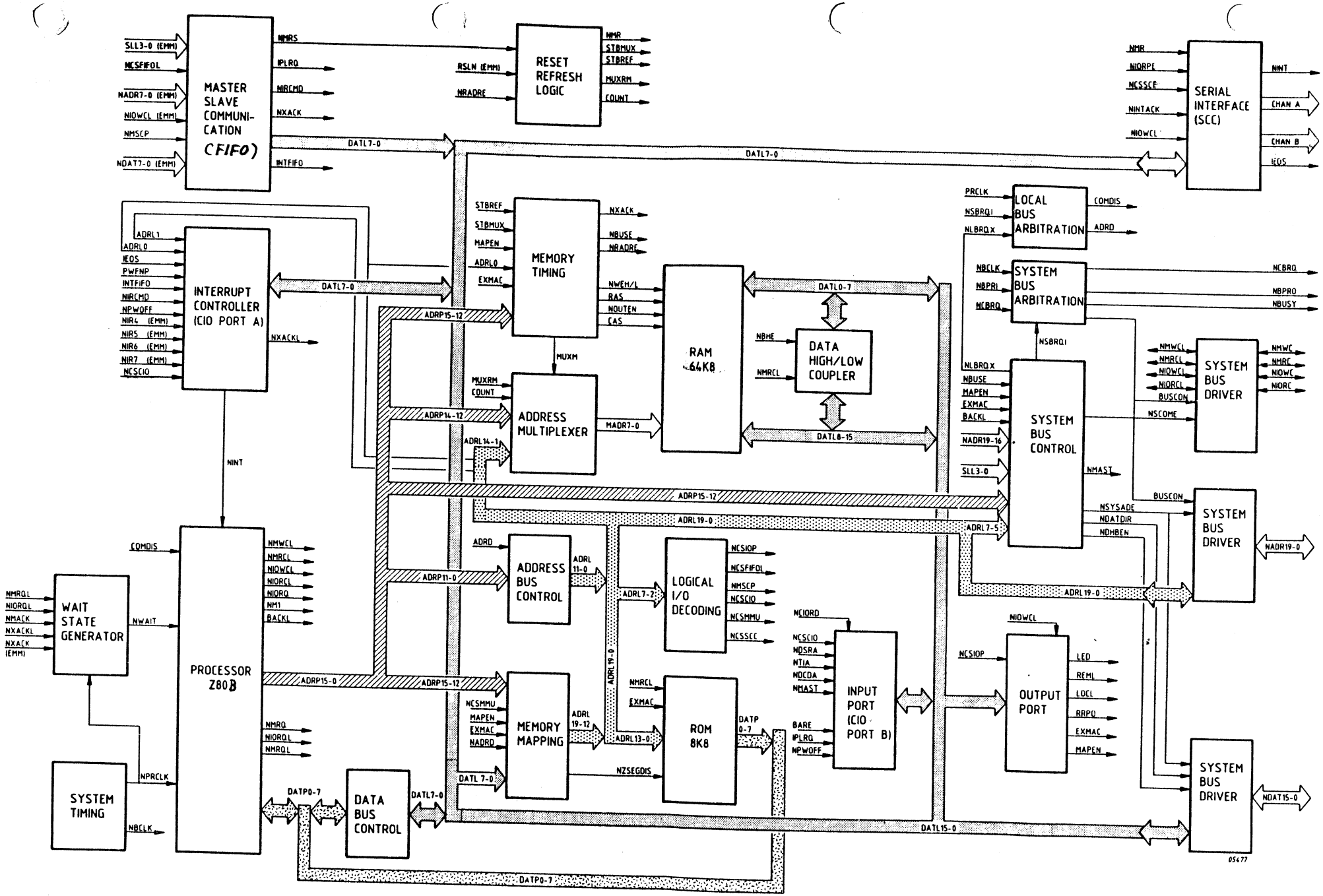
SHEET 2

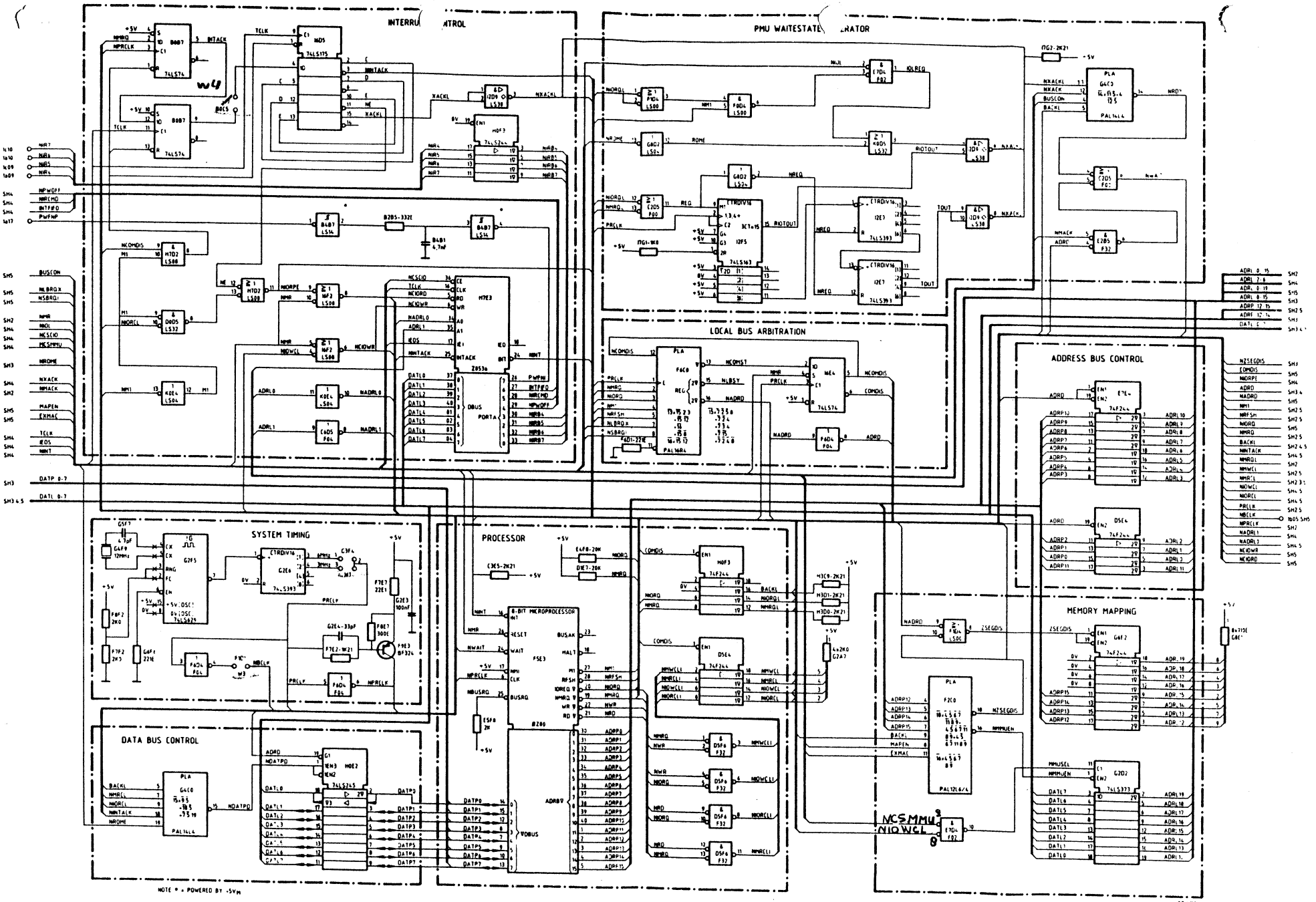

ADDRESSMULTIPLEXER
ROM 8K
DATA HIGH/LOW COUPLER
RAM BANK
SHEET 3

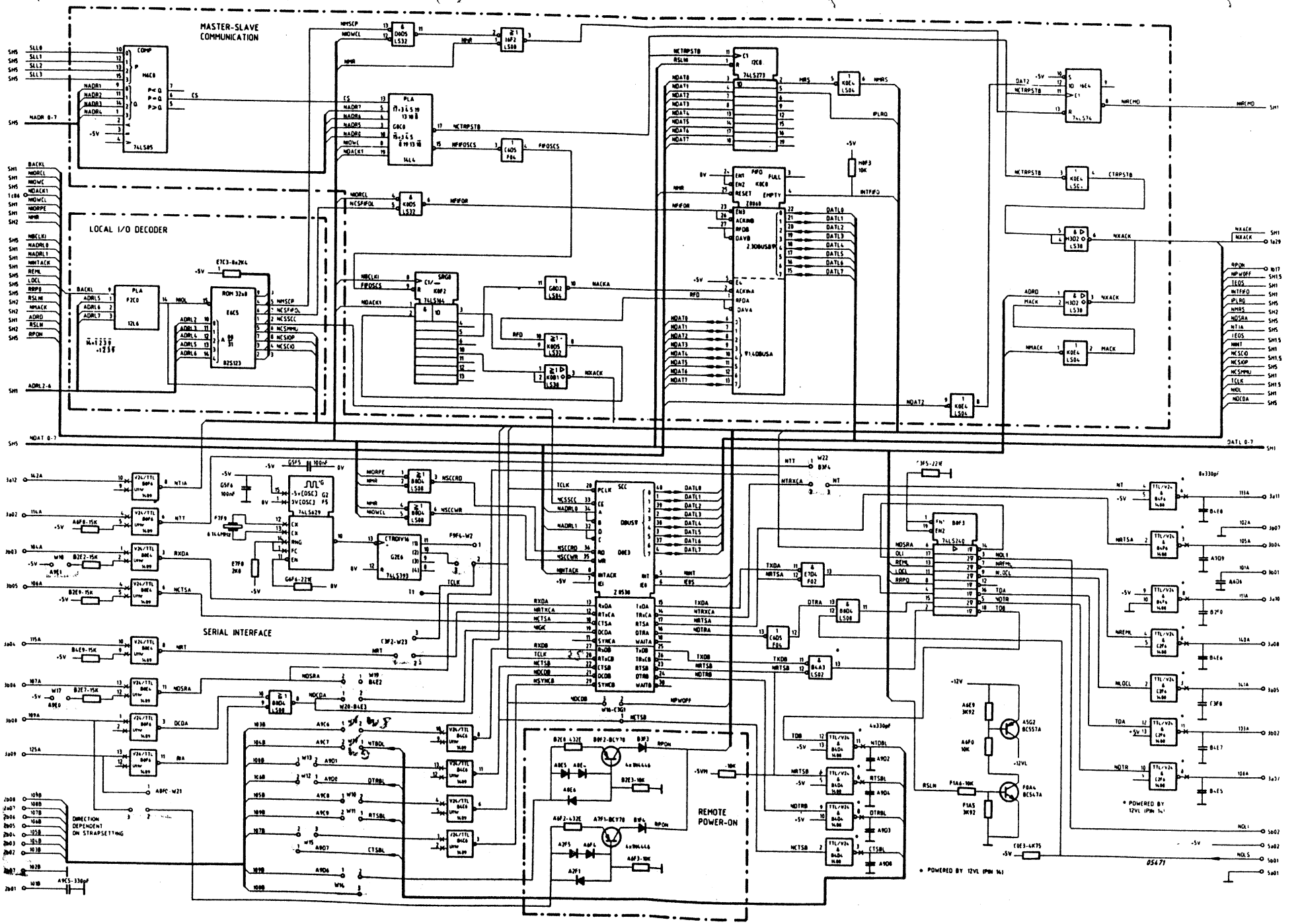

MASTER-SLAVE COMMUNICATION
LOCAL I/O DECODER
SERIAL INTERFACE
FIFO
SCC
REMOTE POWER-ON
Ready for Data
Auxiliary Interface (Channel B) (CP2711)
Master offon !!
SHEET 4


LOCAL I/O PORT
SYSTEM BUS ARBITRATION
SYSTEM BUS CONTROL
SYSTEM BUS DRIVERS
G10
Z8536
74LS273
74LS112
74LS245
74LS240
74LS640
74LS74
74LS85
PAL16R4
PAL14L4
PAL12L6
05474

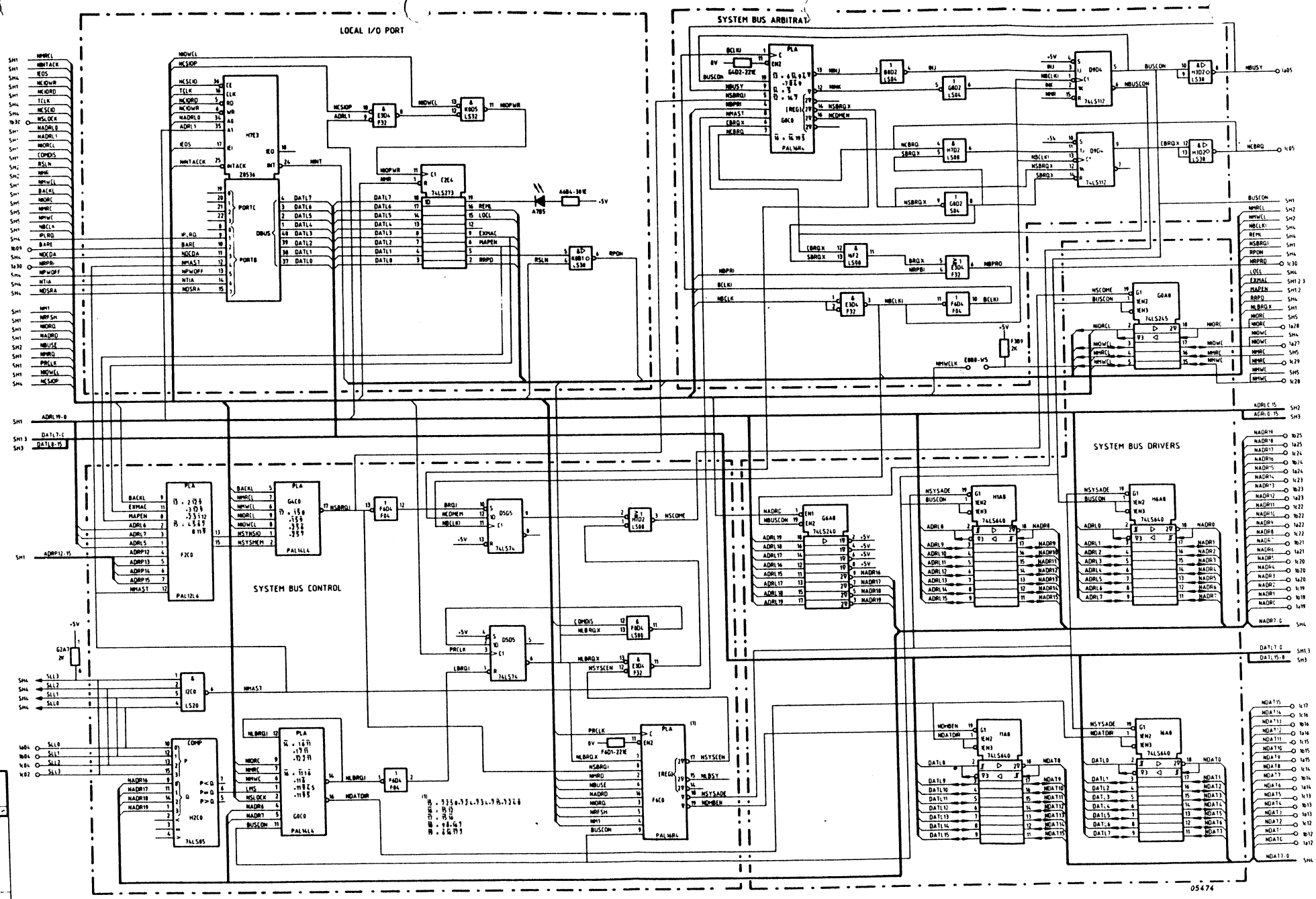
SHEET 5


MASTER SLAVE COMMUNI-CATION (FIFO)
RESET REFRESH LOGIC
SERIAL INTERFACE (SCC)
INTERRUPT CONTROLLER (CIO PORT A)
MEMORY TIMING
LOCAL BUS ARBITRATION
SYSTEM BUS ARBITRATION
RAM 64K8
DATA HIGH/LOW COUPLER
ADDRESS MULTIPLEXER
SYSTEM BUS CONTROL
SYSTEM BUS DRIVER
ADDRESS BUS CONTROL
LOGICAL I/O DECODING
WAIT STATE GENERATOR
PROCESSOR Z80B
MEMORY MAPPING
ROM 8K8
INPUT PORT (CIO PORT B)
OUTPUT PORT
SYSTEM TIMING
DATA BUS CONTROL
SLL3-0 (EMM)
NCSFIFOL
NADR7-0 (EMM)
NIOWCL (EMM)
NMSCP
NDAT7-0 (EMM)
NMRS
IPLRQ
NIRCMD
NXACK
INTFIFO
RSLN (EMM)
NRADRE
NMR
STBMUX
STBREF
MUXRM
COUNT
DATL7-0
NIORPE
NCSSCE
NINTACK
NIOWCL
NINT
CHAN A
CHAN B
IEOS
ADRL1
ADRL0
IEOS
PWFNP
INTFIFO
NIRCMD
NPWOFF
NIR4 (EMM)
NIR5 (EMM)
NIR6 (EMM)
NIR7 (EMM)
NCSCIO
NXACKL
NINT
STBREF
STBMUX
MAPEN
ADRL0
EXMAC
NXACK
NBUSE
NRADRE
NWEH/L
RAS
NOUTEN
CAS
MUXM
MUXRM
COUNT
ADRP15-12
ADRP14-12
ADRL14-1
MADR7-0
DATL0-7
DATL8-15
NBHE
NMRCL
PRCLK
NSBRQI
NLBRQX
COMDIS
ADRD
NBCLK
NBPRI
NCBRQ
NBPRO
NBUSY
NSBRQI
NLBRQX
NBUSE
MAPEN
EXMAC
BACKL
NADR19-16
SLL3-0
NSCOME
NMAST
NMWCL
NMRCL
NIOWCL
NIORCL
BUSCON
NMWC
NMRC
NIOWC
NIORC
ADRP15-12
ADRL19-0
ADRL7-5
NSYSADE
NDATDIR
NDHBEN
BUSCON
NADR19-0
ADRL19-0
COMDIS
NMWCL
NMRCL
NIOWCL
NIORCL
NIORQ
NM1
BACKL
ADRD
ADRP11-0
ADRL 11-0
ADRL7-2
NCSIOP
NCSFIFOL
NMSCP
NCSCIO
NCSMMU
NCSSCC
NCIORD
NCSCIO
NDSRA
NTIA
NDCDA
NMAST
BARE
IPLRQ
NPWOFF
NIOWCL
NCSIOP
LED
REML
LOCL
RRPQ
EXMAC
MAPEN
NMRQL
NIORQL
NMACK
NXACKL
NXACK (EMM)
NWAIT
NPRCLK
NBCLK
ADRP15-0
ADRP15-12
NMRQ
NIORQL
NMRQL
NCSMMU
MAPEN
EXMAC
NADRD
DATL 7-0
ADRL 19-12
ADRL19-0
ADRL13-0
NMRCL
EXMAC
DATP 0-7
NZSEGDIS
DATP0-7
DATL7-0
DATL15-0
NDAT15-0
05477


INTERRUPT CONTROL
PMU WAITESTATE GENERATOR
LOCAL BUS ARBITRATION
ADDRESS BUS CONTROL
SYSTEM TIMING
PROCESSOR
8-BIT MICROPROCESSOR
DATA BUS CONTROL
MEMORY MAPPING
NOTE * = POWERED BY +5VM
SHEET 1


MASTER-SLAVE COMMUNICATION
LOCAL I/O DECODER
SERIAL INTERFACE
REMOTE POWER-ON
DIRECTION DEPENDENT ON STRAPSETTING
* POWERED BY 12VL (PIN 14)
05471

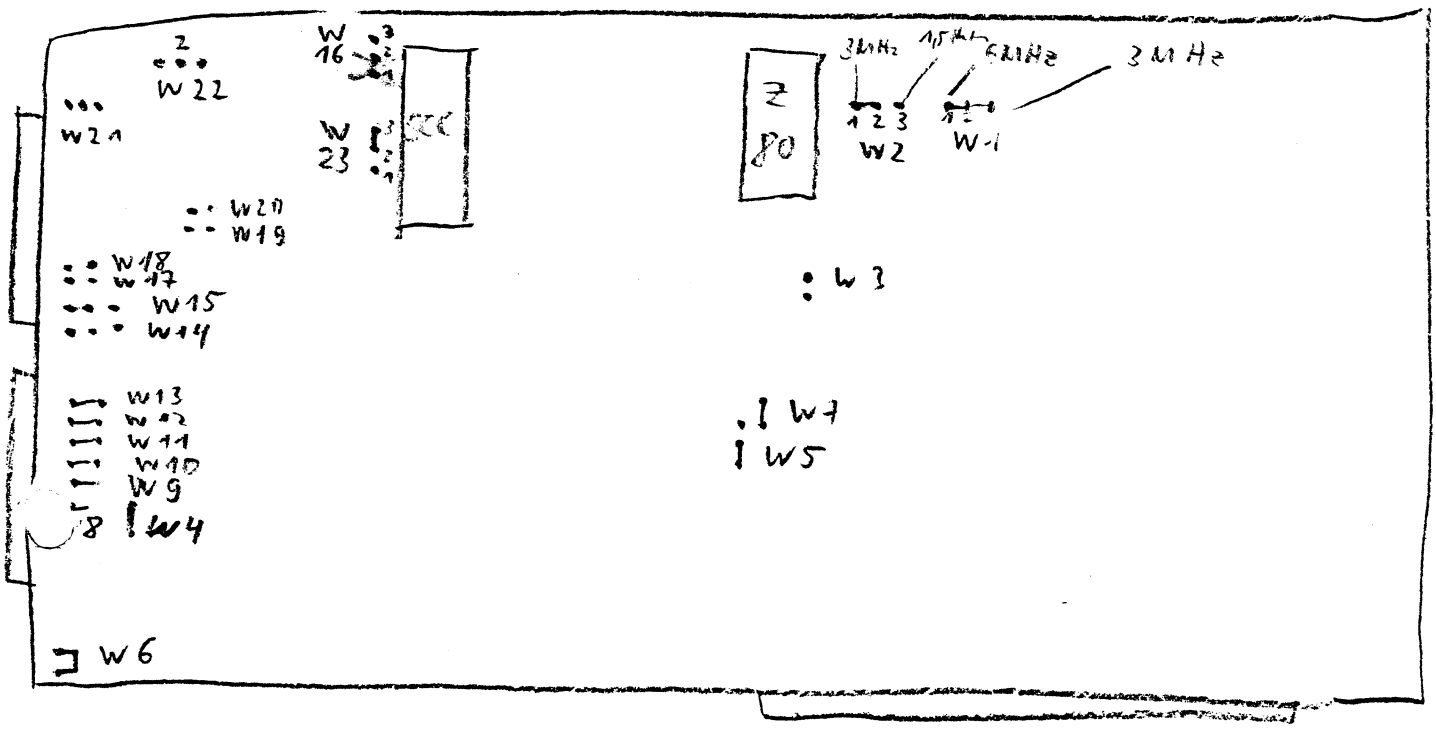
SHEET 4


LOCAL I/O PORT
SYSTEM BUS ARBITRATION
SYSTEM BUS CONTROL
SYSTEM BUS DRIVERS
05474

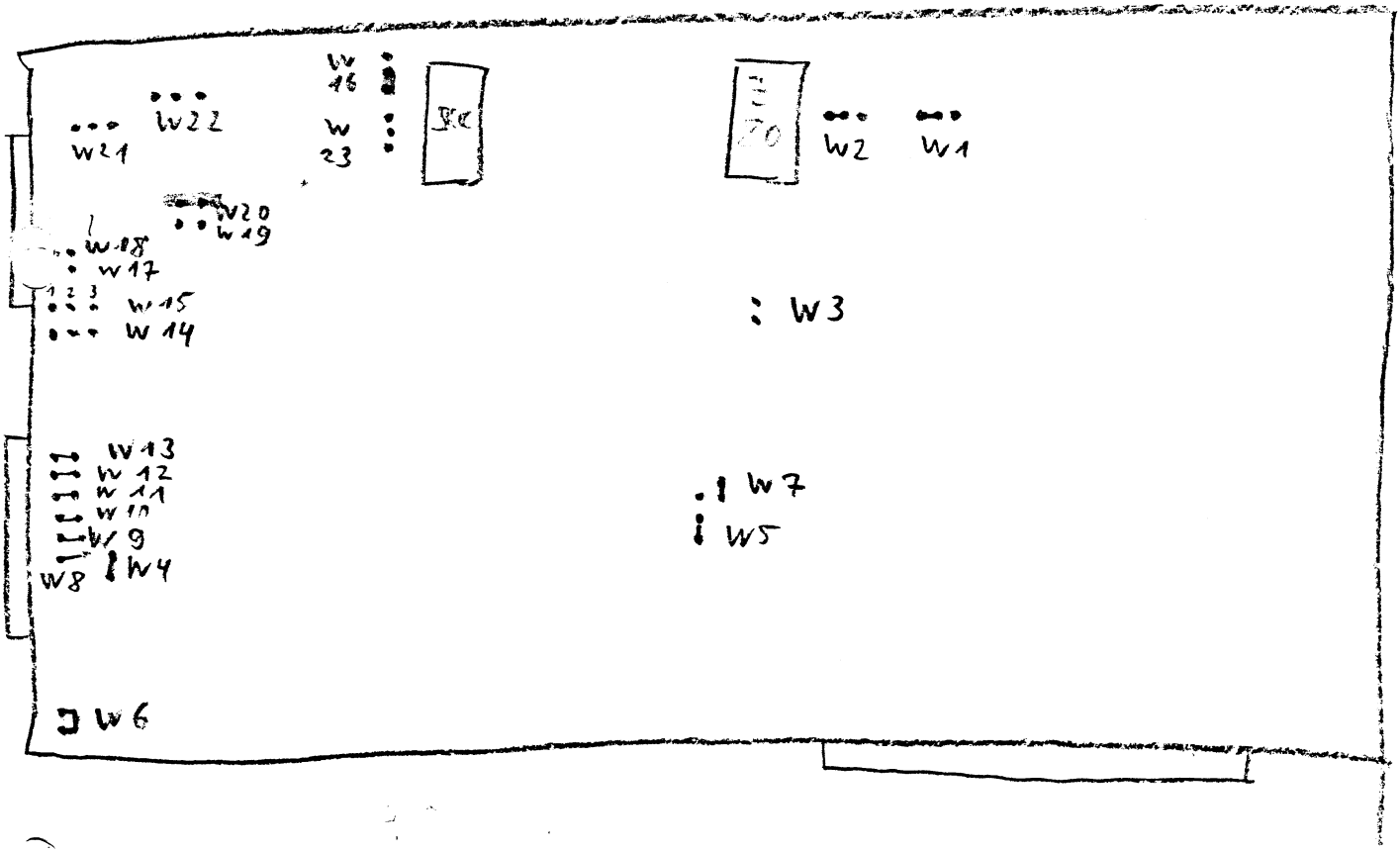
SHEET 5

PMM 80-3

MASTER



SLAVE



STRAP	1 0	2 0	3 0	Master	Slave	Bem.
W1	1			1-2	1-2	1-2 = 6MHz , 2-3 = 3MHz
W	2			1-2	1-2	TCLK 1-2 3MHz 2-3 1,5 " für SCC
W	3			offen	offen	Bus Clock zum EMM-B
W	4			H	H	
W	5			H	H	
W	6			H	H	
W	7			I	I	1-2 2-3
W	8			H	H	
W	9			H	H	
W	10			H	H	
W	11			H	H	
W	12			H	H	
W	13			H	H	
W	14			offen	2-3	1-2 109 2-3 108 ab RX
W	15			1-2	1-2	107
W	16			offen	1-2	NPWOFF 1-2 108 DCE 2-3 109 DTE
W	17			off	off	
W	18			offen	offen	
W	19			offen	?	
W	20			offen	?	
W	21			offen	offen	1-2 DCDA für A12F Channel A 2-3 A
W	22			2-3	2-3	
W	23			2-3	2-3	1-2 2-3 TCLK-RTxCB Channel B

NAME: PMU88S-1CPV 12NC: 5112 291 9822x	CONFIGURATION INDEX								
CONTENTS	MODIFICATION LEVEL x								
PAGE	1	2	3	4	5	6	7	8	9
	. . . . .		850801	850801	850801				
	. . . . .		850801	850801	850801				
	. . . . .		850801	850801	850801				
	. . . . .		850801	850801	850801				
	. . . . .		850801	850801	850801				
	. . . . .		850801	850801	850801				
	. . . . .		850801	850801	850801				
	. . . . .		850801	850801	850801				
	. . . . .		850801	850801	850801				
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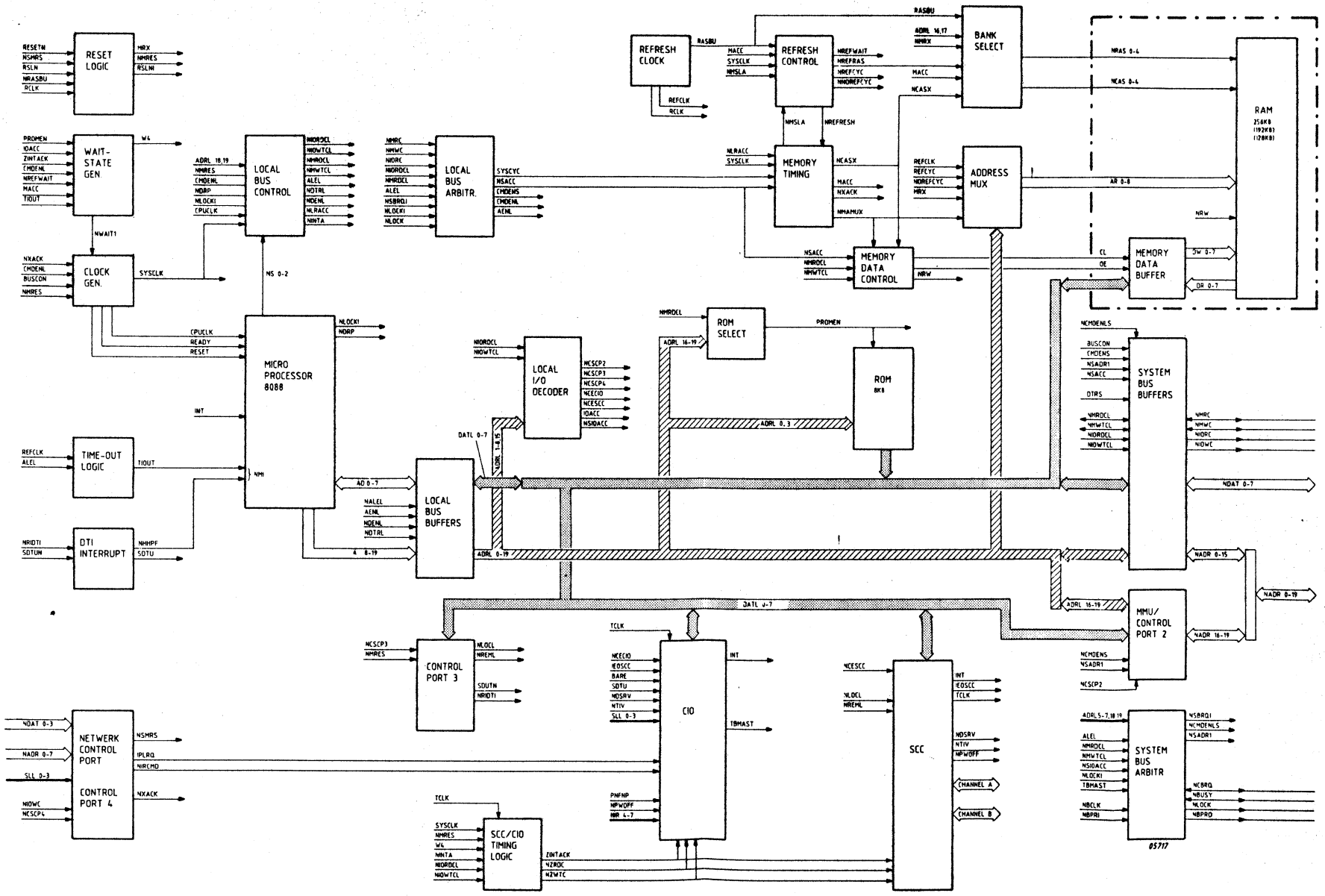
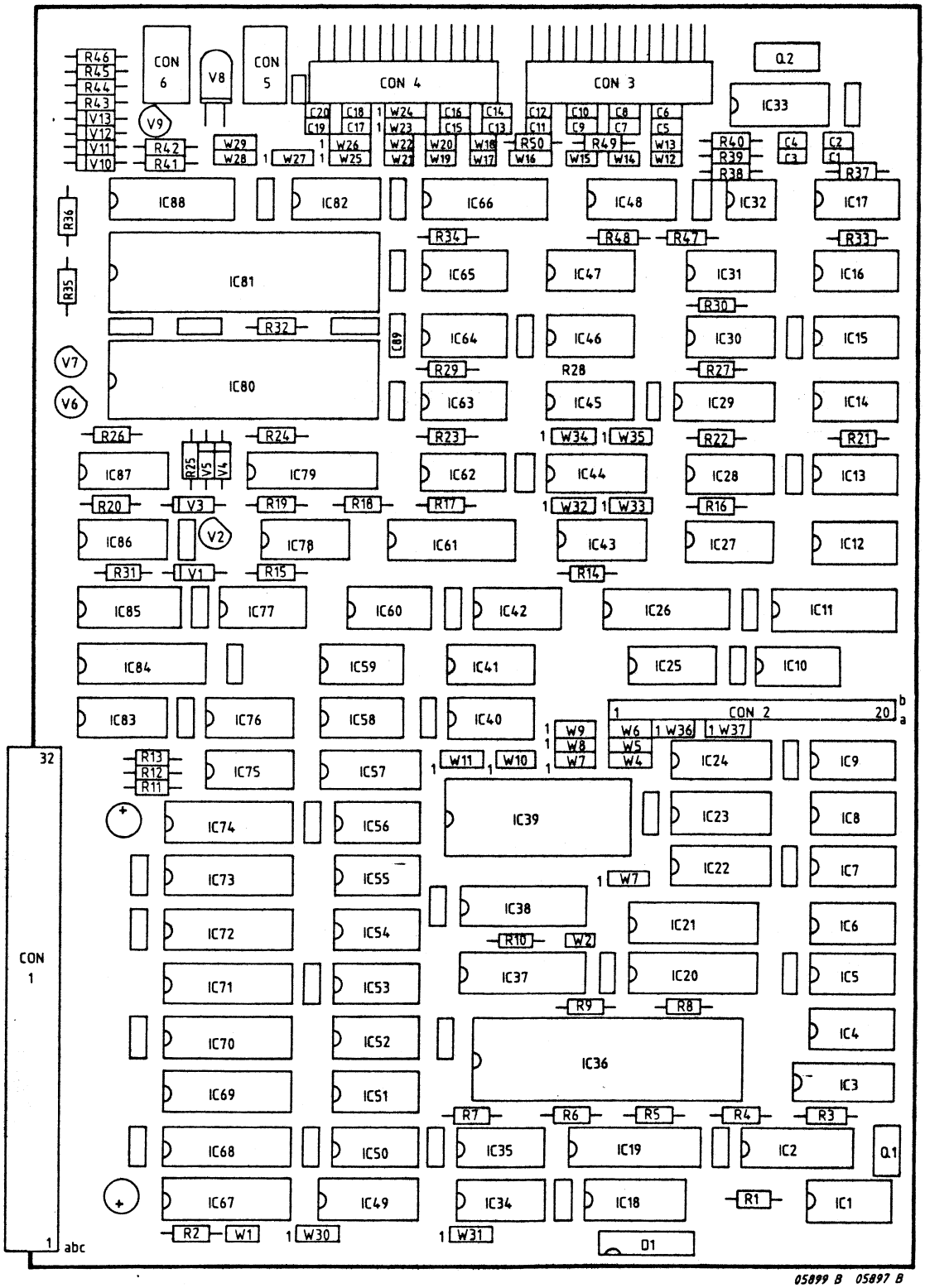
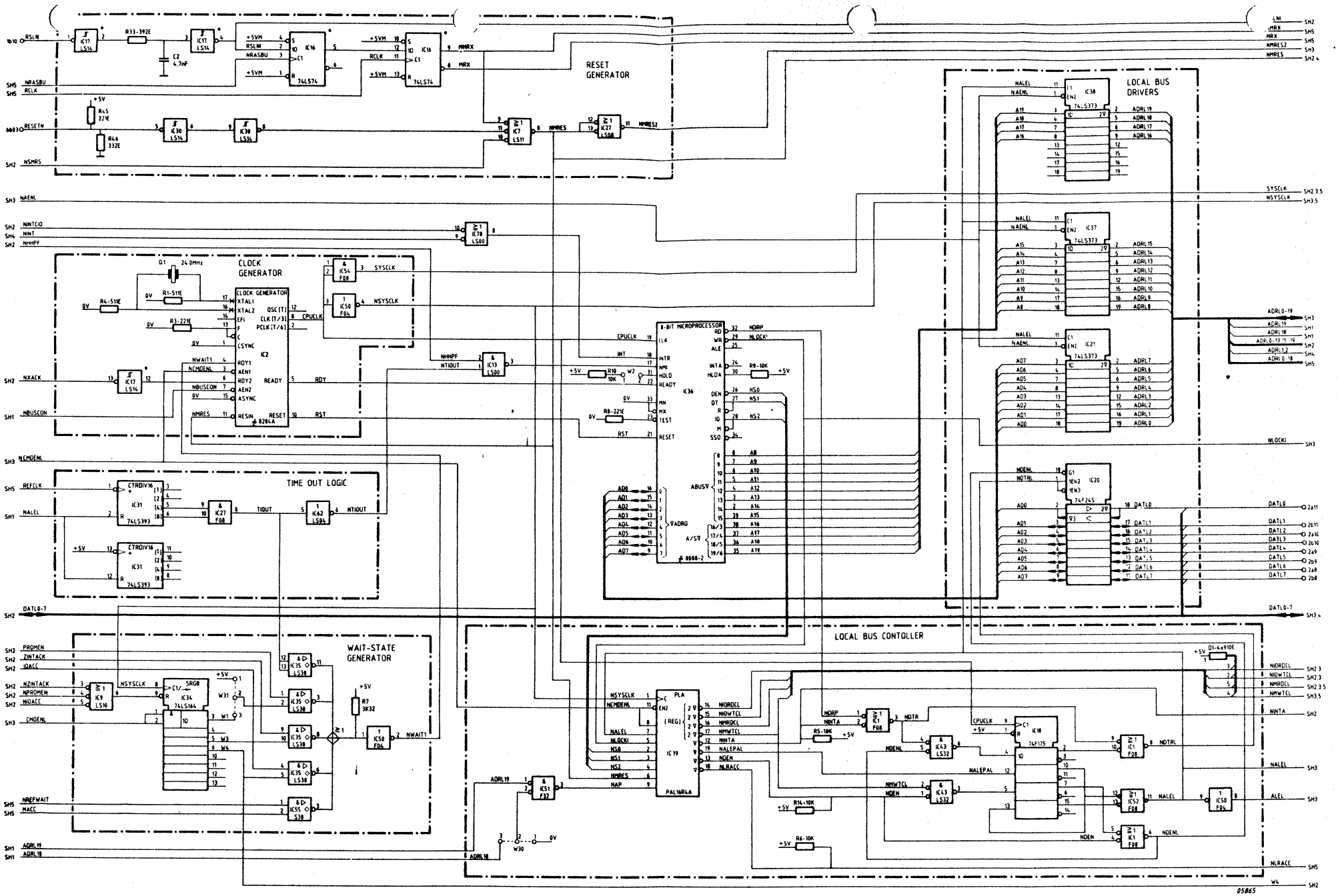
	. . . . .		850801	850801	850801				
	. . . . .		850801	850801	850801				
	. . . . .		850801	850801	850801				
	. . . . .		850801	850801	850801				
RELEVANT SI-NUMBER: P3500-			orig.	068	068				
P3800-			orig.	028	028				

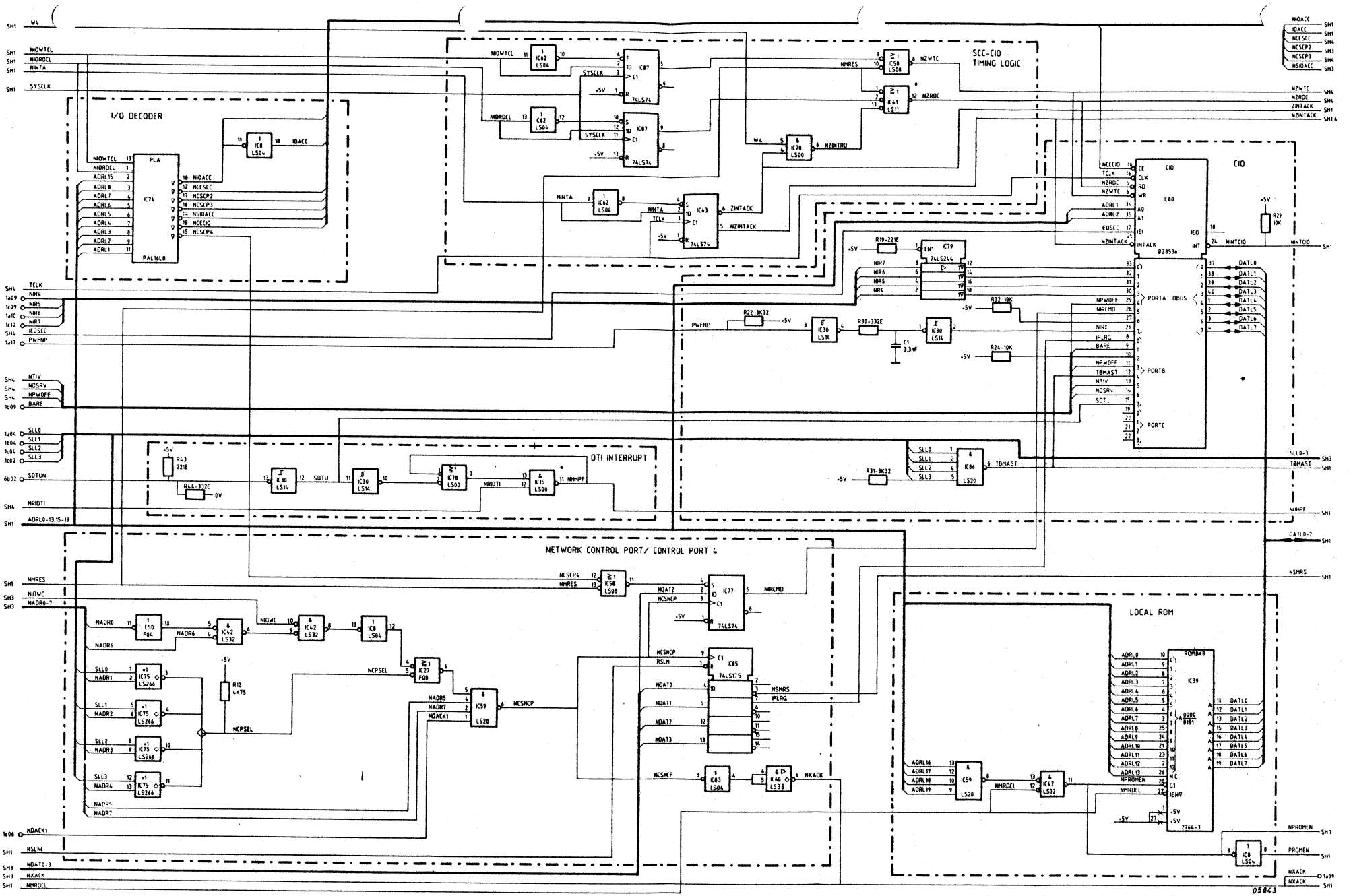


BLOCKDIAGRAM PMU88S-1CPV

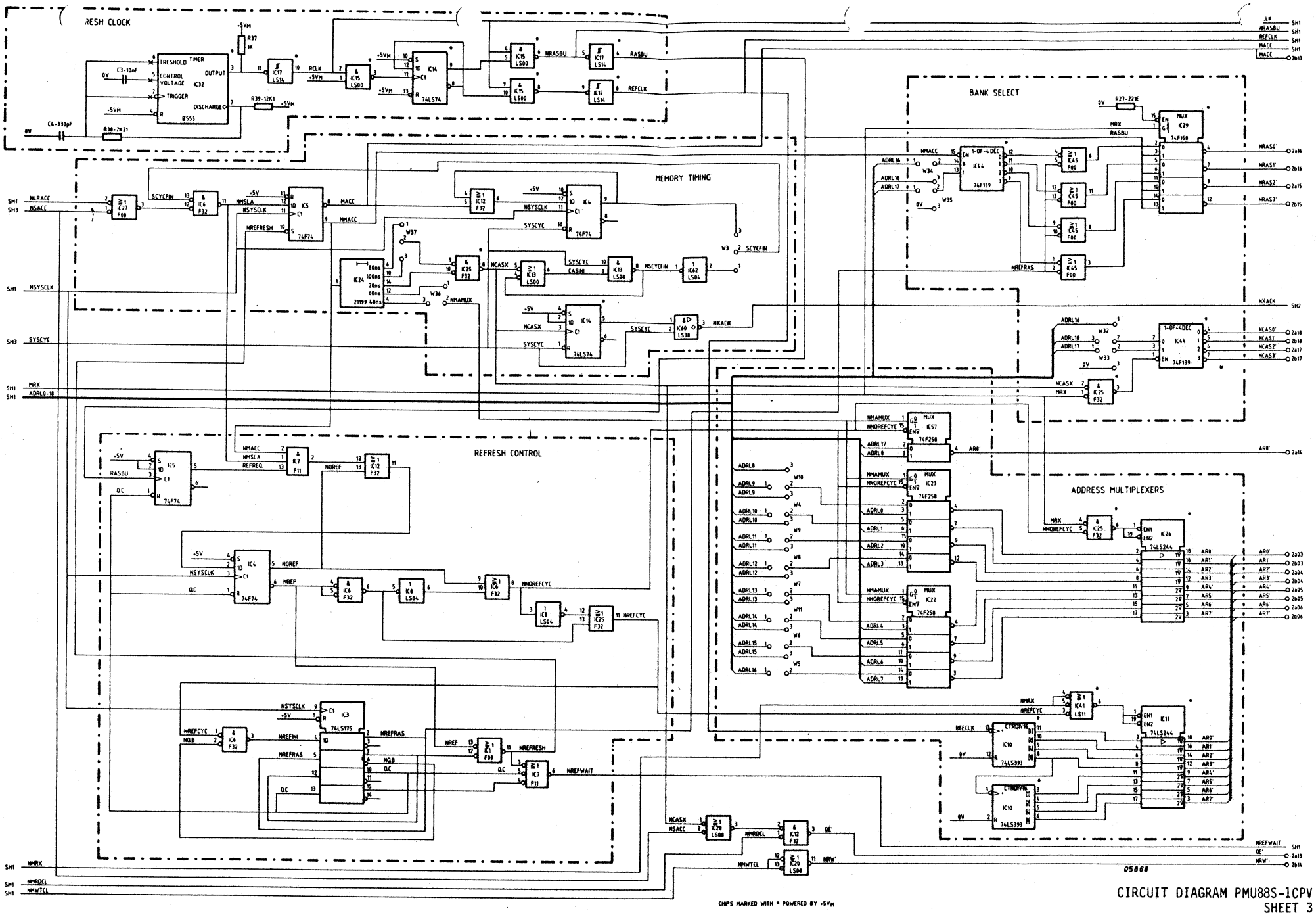

CON 6
V8
CON 5
CON 4
CON 3
Q2
IC33
IC88
IC82
IC66
IC48
IC32
IC17
IC81
IC65
IC47
IC31
IC16
IC80
IC64
IC46
IC30
IC15
IC63
IC45
IC29
IC14
IC87
IC79
IC62
IC44
IC28
IC13
IC86
IC78
IC61
IC43
IC27
IC12
IC85
IC77
IC60
IC42
IC26
IC11
IC84
IC59
IC41
IC25
IC10
IC83
IC76
IC58
IC40
CON 2
IC75
IC57
IC24
IC9
IC74
IC56
IC39
IC23
IC8
IC73
IC55
IC22
IC7
IC72
IC54
IC38
IC21
IC6
IC71
IC53
IC37
IC20
IC5
IC70
IC52
IC36
IC4
IC69
IC51
IC3
IC68
IC50
IC35
IC19
IC2
Q1
IC67
IC49
IC34
IC18
IC1
D1
CON 1
05899 B 05897 B



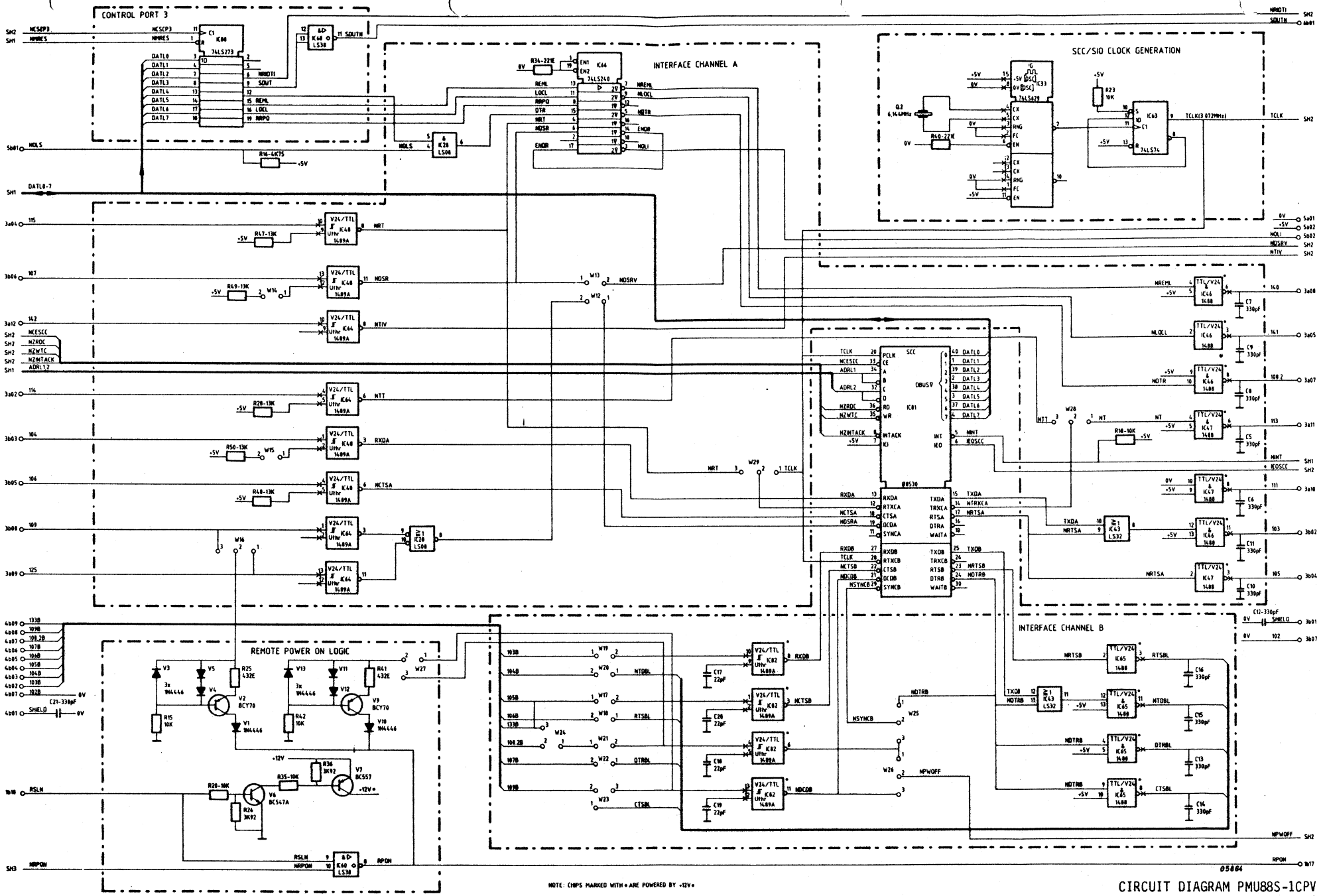
CIRCUIT DIAGRAM PMU88S-1CPV
SHEET 1



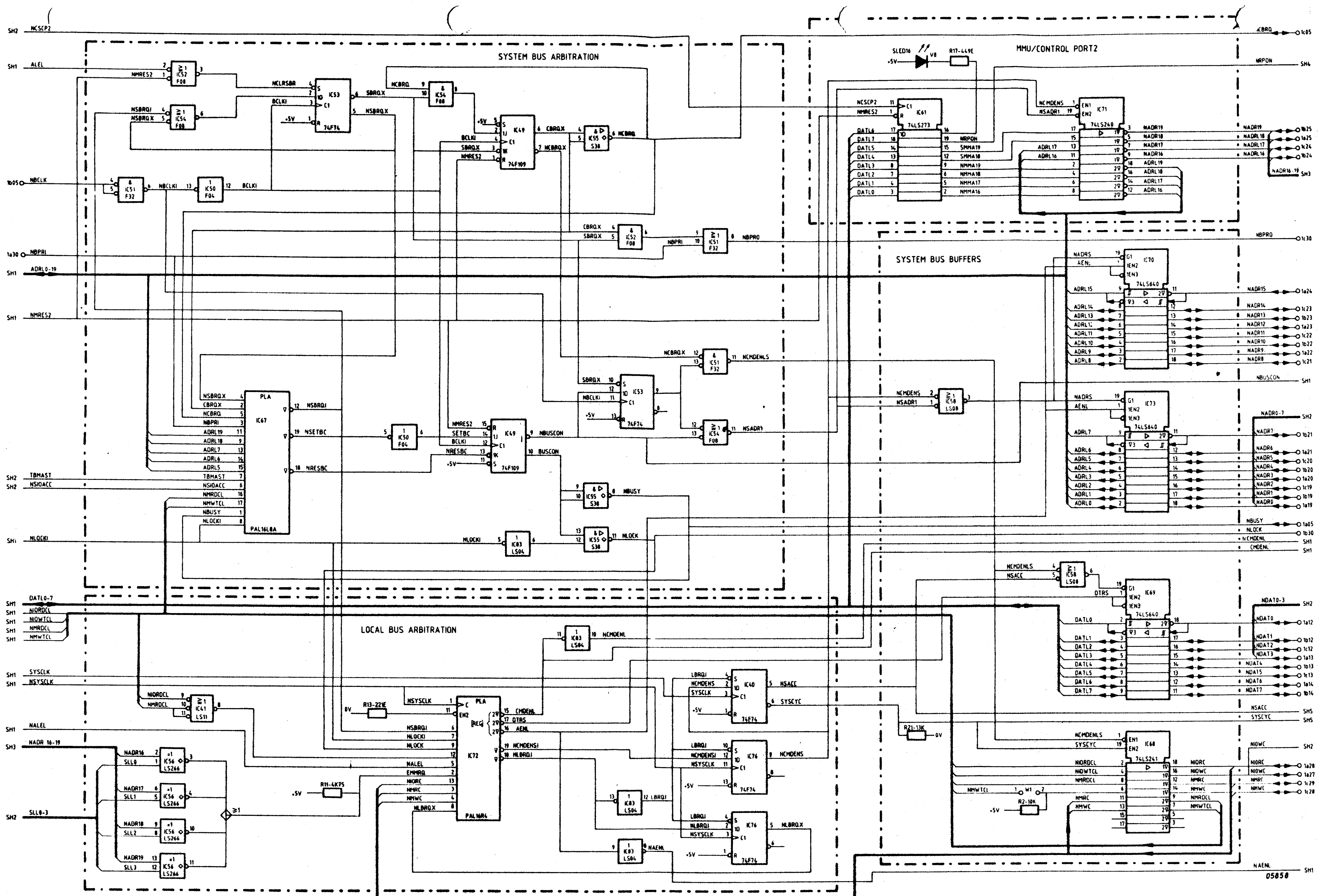
CIRCUIT DIAGRAM PMU88S-1CPV
SHEET 2



CIRCUIT DIAGRAM PMU88S-1CPV
SHEET 3



CIRCUIT DIAGRAM PMU88S-1CPV
SHEET 4



CIRCUIT DIAGRAM PMU88S-1CPV
SHEET 5

PMU 88S-1CPV	PAL DESCRIPTION
IC 19 (PAL 16R4)	$\overline{I2}$ = $\overline{02}.\ \overline{03}.\ \overline{04}.\ \overline{07}.\ \overline{08}.\ \overline{09}$
	+ $\overline{05}.\ \overline{08}.\ \overline{I2}$
	+ $\overline{02}.\ \overline{03}.\ \overline{04}.\ \overline{08}.\ \overline{I2}$
	+ $\overline{07}.\ \overline{08}.\ \overline{I2}$
	$\overline{I3}$ = $05.\ \overline{08}.\ \overline{I2}$
	+ $\overline{08}.\ \overline{I4}.\ 15.\ 16.\ 17$
	+ $\overline{08}.\ 14.\ \overline{I5}.\ 16.\ 17$
	+ $\overline{08}.\ 14.\ 15.\ \overline{I6}.\ 17$
	+ $\overline{08}.\ 14.\ 15.\ 16.\ 17$
	$\overline{I4}$:= $02.\ \overline{03}.\ \overline{04}.\ \overline{07}$
	$\overline{I5}$:= $\overline{02}.\ 03.\ \overline{04}.\ \overline{07}$
	$\overline{I6}$:= $\overline{02}.\ \overline{03}.\ 04.\ \overline{07}$
	+ $02.\ \overline{03}.\ \overline{04}.\ \overline{07}$
	$\overline{I7}$:= $\overline{02}.\ 03.\ 04.\ \overline{07}$
	$\overline{I8}$ = $\overline{02}.\ \overline{03}.\ 04.\ \overline{07}.\ \overline{08}.\ \overline{09}$
	$02.\ \overline{03}.\ 04.\ \overline{07}.\ \overline{08}.\ \overline{09}$
	$\overline{02}.\ 03.\ 04.\ \overline{07}.\ \overline{08}.\ \overline{09}$
	$\overline{02}.\ \overline{03}.\ 04.\ \overline{08}.\ \overline{I8}$
	$02.\ \overline{03}.\ 04.\ \overline{08}.\ \overline{I8}$
	$\overline{02}.\ 03.\ 04.\ \overline{08}.\ \overline{I8}$
	$\overline{I9}$ = $\overline{02}.\ \overline{03}.\ 06$
	+ $\overline{02}.\ 03.\ 06$
	+ $02.\ \overline{03}.\ 06$
IC 67 (PAL 16L8)	$\overline{I2}$ = $\overline{06}.\ 07.\ \overline{I3}.\ 14.\ \overline{I5}$
	+ $\overline{06}.\ \overline{07}$
	+ $\overline{09}.\ 11.\ \overline{I6}.\ 17$
	+ $\overline{09}.\ 11.\ 16.\ \overline{I7}$
	$\overline{I8}$ = $\overline{02}.\ \overline{05}.\ \overline{08}$
	$\overline{I9}$ = $01.\ 02.\ \overline{03}.\ \overline{04}$
	$01.\ \overline{03}.\ 05.\ \overline{07}$
IC 72 (PAL 16R4)	$\overline{I5}$:= $05.\ 07.\ \overline{08}$
	+ $\overline{05}.\ \overline{06}.\ \overline{08}$
	+ $\overline{I5}.\ \overline{I6}$
	$\overline{I6}$:= $05.\ 07.\ \overline{08}.\ 16$
	+ $\overline{05}.\ \overline{06}.\ \overline{08}$
	+ $\overline{08}.\ \overline{I6}$
	+ $\overline{09}.\ \overline{I6}$
	+ $\overline{I6}.\ \overline{I9}$
	$\overline{I7}$:= $\overline{04}.\ 05.\ \overline{08}$
	$\overline{04}.\ \overline{05}.\ \overline{08}.\ \overline{I6}$
	$\overline{08}.\ \overline{I6}.\ \overline{I7}$
	$08.\ \overline{I2}.\ 16$
	$\overline{I8}$ = $02.\ \overline{03}.\ 04$
	+ $02.\ 03.\ \overline{04}$
	$\overline{I9}$ = $\overline{08}.\ \overline{I5}.\ \overline{I6}$
IC 74 (PAL 16L8)	$\overline{I2}$ = $\overline{01}.\ \overline{02}.\ \overline{03}.\ \overline{04}.\ \overline{05}.\ \overline{06}.\ \overline{07}.\ \overline{08}.\ 13$
	+ $01.\ \overline{02}.\ \overline{03}.\ \overline{04}.\ \overline{05}.\ \overline{06}.\ \overline{07}.\ \overline{08}.\ \overline{13}$
	$\overline{I4}$ = $\overline{01}.\ \overline{02}.\ \overline{03}.\ \overline{04}.\ 05.\ 13$
	+ $01.\ \overline{02}.\ \overline{03}.\ \overline{04}.\ 05.\ \overline{13}$
	+ $\overline{01}.\ \overline{02}.\ \overline{03}.\ 04.\ 13$
	+ $01.\ \overline{02}.\ \overline{03}.\ 04.\ \overline{13}$
	+ $\overline{01}.\ \overline{02}.\ 03.\ 13$
	+ $01.\ \overline{02}.\ 03.\ \overline{13}$

PMU 88S-1CPV PAL DESCRIPTION

$$
\begin{aligned}
\overline{I5} &= 01.\,\overline{02}.\,03.\,\overline{04}.\,\overline{05}.\,06.u\overline{07}.\,08.\,\overline{09}.\,11.\,\overline{13}\\
\overline{I6} &= 01.\,\overline{02}.\,\overline{03}.\,\overline{04}.\,\overline{05}.\,06.\,\overline{07}.\,08.\,\overline{09}.\,\overline{11}.\,\overline{13}\\
\overline{I7} &= 01.\,\overline{02}.\,\overline{03}.\,\overline{04}.\,\overline{05}.\,06.\,\overline{07}.\,\overline{08}.\,\overline{09}.\,11.\,\overline{13}\\
\overline{I8} &= \overline{01}.\,\overline{02}.\,\overline{03}.\,\overline{04}.\,\overline{05}.\,13\\
&\quad + 01.\,\overline{02}.\,\overline{03}.\,\overline{04}.\,\overline{05}.\,\overline{13}\\
\underline{19} &= \overline{01}.\,\overline{02}.\,\overline{03}.\,\overline{04}.\,\overline{05}.\,06.\,\overline{07}.\,\overline{08}.\,\overline{09}.\,\overline{11}.\,13\\
&\quad + \overline{01}.\,\overline{02}.\,\overline{03}.\,\overline{04}.\,\overline{05}.\,06.\,\overline{07}.\,\overline{08}.\,\overline{09}.\,11.\,13\\
&\quad + \overline{01}.\,\overline{02}.\,\overline{03}.\,\overline{04}.\,\overline{05}.\,06.\,\overline{07}.\,\overline{08}.\,09.\,\overline{11}.\,13\\
&\quad + \overline{01}.\,\overline{02}.\,\overline{03}.\,\overline{04}.\,\overline{05}.\,06.\,\overline{07}.\,\overline{08}.\,09.\,11.\,13\\
&\quad + 01.\,\overline{02}.\,\overline{03}.\,\overline{04}.\,\overline{05}.\,06.\,\overline{07}.\,\overline{08}.\,09.\,11.\,\overline{13}
\end{aligned}
$$

CONNECTOR LAYOUT PMU88S-1CPV

CONNECTOR 1

	a	b	c
1	+5V	+5V	+5V
2	OV	+5V	SLL3
3	OV	OV	OV
4	SLL0	SLL1	SLL2
5	NBUSY	NBCLK	NCBRQ
6			NDACK1
7			
8			
9	NIR4	BARE	NIR5
10	NIR6	RSLN	NIR7
11	OV	OV	OV
12	NDAT0	NDAT1	NDAT2
13	NDAT3	NDAT4	NDAT5
14	NDAT6	NDAT7	
15			
16			
17	PWFNP	RPON	
18	OV	OV	OV
19	NADR0	NADR1	NADR2
20	NADR3	NADR4	NADR5
21	NADR6	NADR7	NADR8
22	NADR9	NADR10	NADR11
23	NADR12	NADR13	NADR14
24	NADR15	NADR16	NADR17
25	NADR18	NADR19	
26			
27	NIOWC		
28	NIORC		NMWC
29	NXACK		NMRC
30	NBPRI	NLOCK	NBPRO
31	+12V	+5VM	+5VM
32	-12V		

CONNECTOR 2

	a	b
1	OV	OV
2	+5V	+5VM
3	AR0'	AR1'
4	AR2'	AR3'
5	AR4'	AR5'
6	AR6'	AR7'
7		
8	DATL6	DATL7
9	DATL4	DATL5
10	DATL2	DATL3
11	DATL0	DATL1
12		
13	OE'	MACC
14	AR8'	NRW'
15	NRAS2'	NRAS3'
16	NRAS0'	NRAS1'
17	NCAS2'	NCAS3'
18	NCAS0'	NCAS1'
19	+5VM	+5VM
20	OV	OV

CONNECTOR 3

	a	b
1		101
2	114	103
3		104
4	115	105
5	141	106
6		107
7	108.2	102
8	140	109
9	125	
10	111	
11	113	
12	142	
13	////////	

CONNECTOR 4

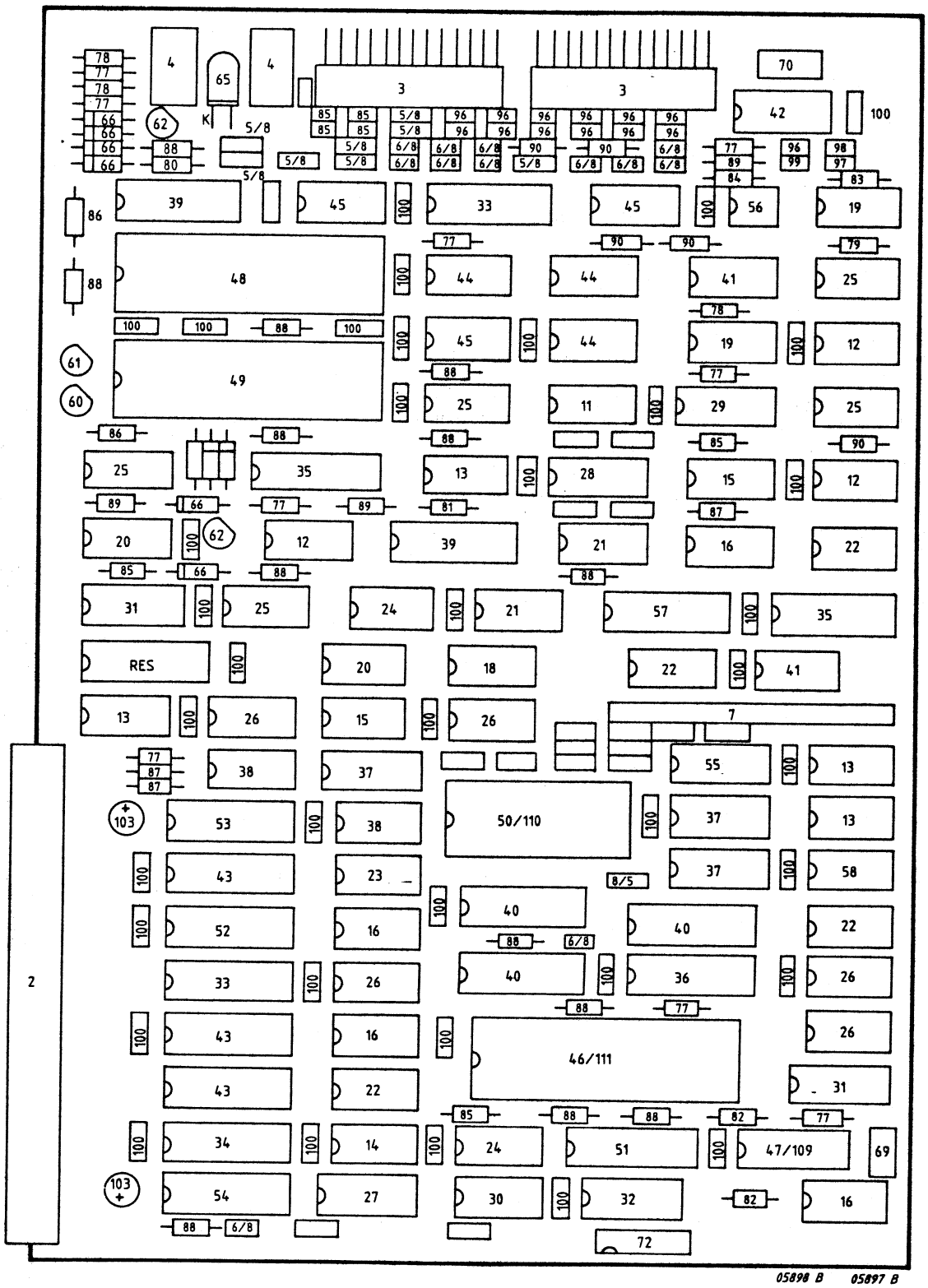
	a	b
1		101B
2		103B
3		104B
4		105B
5		106B
6		107B
7	108.2B	102B
8		109B
9		133B
10		
11		
12		
13	////////	

CONNECTOR 5

	a	b
1	OV	NOLS
2	+5V	NOLI
3	////////	

CONNECTOR 6

	a	b
1	OV	SDUTN
2	OV	SDTUN
3	////////	RESETN


05898 B
05897 B

PARTS LIST PMU88S-1CPV

Pos.	Art. Nr.	12-NC	Description
2	2422 025 89283	5322 265 64104	Male plug 96 pol
3	2422 062 92591	5322 267 54179	Connector 25 pol
4	2422 062 90591	5322 267 50537	Connector 5 pol
5	5112 211 03271	5322 265 64028	Connector 3 pol
6	5112 211 06041	5322 265 64028	Connector 2 pol
8	2422 024 88003	5322 263 64007	Female test COMA
12	9332 315 90112	5322 209 84823	IC N74LS0DA
13	9332 316 00112	4822 209 80783	IC 74LS04
14	9336 203 30112	5322 209 81577	IC 74F04PC
15	9332 735 20112	5322 209 84995	IC 74LS08
16	9336 179 40112	5322 209 81574	IC 74F08PC
17	9332 869 70112	5322 209 84996	IC N74LS10A
18	9332 746 70112	5322 209 85604	IC 74LS11
19	9332 759 70112	5322 209 85199	IC SN74LS14N
20	9332 870 30112	5322 209 85569	IC SN74LS20N
21	9332 870 90112	5322 209 85311	IC 74LS32
22	9336 179 50112	5322 209 81529	IC 74F32PC
23	9332 920 50112	5322 209 85677	IC N74S38A
24	9332 871 10112	5322 209 85605	IC 74LS38
25	9334 451 50112	4822 209 80782	IC 74LS74
26	9336 154 00112	5322 209 81474	IC 74F74PC
27	9336 203 70112	5322 209 81669	IC 74F109PC
28	9336 329 20112	5322 209 82234	IC 74F139PC
29	9336 180 40112	5322 209 82012	IC 74F158PC
30	9332 874 60112	5322 209 81487	IC N74LS164N
31	9332 874 90112	5322 209 84999	IC 74LS175
32	9336 329 30112	5322 209 81542	IC 74F175
33	9334 182 20112	5322 209 85862	IC SN74LS240N
34	9334 005 50112	5322 209 85873	IC SN74LS241N
35	9334 538 30112	5322 209 86017	IC N74LS244N
36	9336 716 00112	5322 209 82169	IC 74F245PC
37	9336 762 30112	5322 209 81769	IC 74F258PC
38	9334 199 70112	5322 209 86286	IC SN74LS266N
39	9333 948 70112	5322 209 85792	IC N74LS273N
40	9334 534 00112	5322 209 86062	IC SN74LS373J
41	9334 037 90112	4822 209 80447	IC N74LS393N
42	9335 855 80682	5322 209 81589	IC SN74LS629N-00
43	9336 110 10112	5322 209 81572	IC SN74LS640N
44	9332 991 80112	5322 209 84307	IC MC1488L
45	9334 912 90112	5322 209 86103	IC SN75189AN
46	5112 209 21721	5322 209 83017	IC D8088-2-SELECT
47	9336 527 00112	5322 209 10412	IC D8284A
48	9337 049 10112	5322 209 82023	IC Z8530PS
49	9337 062 30112	5322 209 82025	IC Z8536PS

PARTS LIST PMU88S-1CPV (CONT'D)

Pos.	Art. Nr.	12-NC	Description
50	5112 208 01921		PROM PMU88S
51	5112 208 02801	5322 209 83016	PAL16R4ACNSHRP/PMU88
52	5112 208 02183	5322 209 82836	AMPAL16R4LPC/PMU88S2
53	5112 208 02161	5322 209 82834	AMPAL16L8LPC/PMU88S1
54	5112 208 01901	5322 209 82872	PAL16L8ACNSHRP/PMU88
55	9360 049 70112	5322 209 82026	IC PE21199
56	9332 243 90112	4822 209 80775	IC NE555N
60	9331 976 20112	4822 130 41019	Transistor BC547A
61	9331 977 20112	4822 130 44484	Transistor BC557A
62	9330 441 00112	5322 130 40324	Transistor BCY70
65	9334 855 50112	5322 130 34822	Diode CQX42B
66	9331 126 60112	5322 130 30686	Diode 1N4446
69	5112 209 19721	5322 242 70978	Crystal 24MHZ
70	5112 209 12651	5322 242 70689	X-Tal 6,144MHZ
72	5112 209 01691	5322 209 84594	RNW ERC1179
77	2322 151 52211	4822 116 51223	Resistor 221E, 1%, 0.4W
78	2322 151 53321	4822 116 51226	Resistor 332E, 1%, 0.4W
79	2322 151 53921	4822 116 51228	Resistor 392E, 1%, 0.4W
80	2322 151 54321	4822 116 51229	Resistor 432E, 1%, 0.4W
81	2322 151 54991	5322 116 54524	Resistor 499E, 1%, 0.4W
82	2322 151 55111	4822 116 51282	Resistor 511E, 1%, 0.4W
83	2322 151 51002	4822 116 51235	Resistor 1KO, 1%, 0.4W
84	2322 151 52212	4822 116 51245	Resistor 2K21, 1%, 0.4W
85	2322 151 53322	4822 116 51247	Resistor 3K32, 1%, 0.4W
86	2322 151 53922	4822 116 51249	Resistor 3K92, 1%, 0.4W
87	2322 151 54752	5322 116 54008	Resistor 4K75, 1%, 0.4W
88	2322 151 51003	4822 116 51253	Resistor 10K, 1%, 0.4W
89	2322 151 51213	5322 116 50572	Resistor 12K1, 1%, 0.4W
90	2322 151 51303	5322 116 50522	Resistor 13K, 1%, 0.4W
95	2222 682 34229	5322 122 32242	Capacitor 22pF, 63V, 2%
96	2222 630 18331	4822 122 30055	Capacitor 330pF, 100V
97	2222 630 18332	4822 122 30099	Capacitor 3300pF, 100V, 10%
98	2222 630 18472	4822 122 30128	Capacitor 4700pF, 100V, 10%
99	2222 629 18103	4822 122 30043	Capacitor 10nF, 63V, 8%
100	9912 202 52151	5322 122 10313	Capacitor 100nF
103	2020 002 90542	5322 124 21335	Capacitor 33uF, 25V
109	2422 549 13657	4822 255 40239	IC-Socket 18 pol
110	2422 549 13644	5322 255 44234	Socket 28 pol (DIL)
111	2422 549 13647	5322 255 44235	Socket 40 pol (DIL)
11	9335 845 40682	5322 209 81534	IC 74F00
57	9336 120 50112	5322 209 81128	IC 74F244PC
58	9336 317 90112	5322 209 81536	IC 74F11PC

NAME: PMU88S-M256K 12NC: 5112 291 9576x	CONFIGURATION INDEX								
CONTENTS	MODIFICATION LEVEL x								
PAGE	1	2	3	4	5	6	7	8	9
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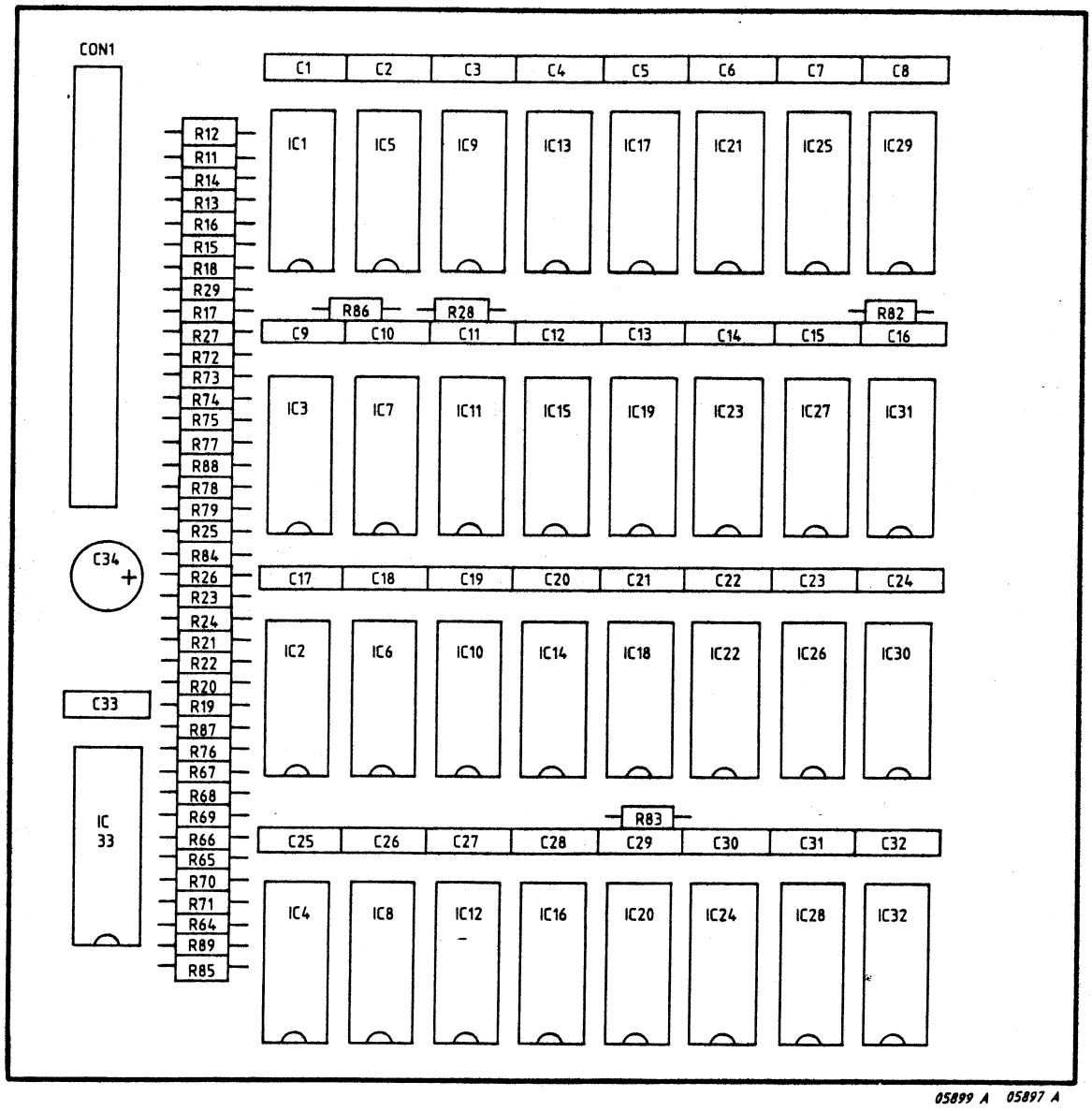
- Component Location 8-2	. . . . .		850801						
- Circuit Diagram 8-5	. . . . .		850801						
- Connector Layout 8-7	. . . . .		850801						
- Parts Location 8-8	. . . . .		850801						
- Parts List 8-9	. . . . .		850801						
- Printed Wiring 8-13	. . . . .		850801						
RELEVANT SI-NUMBER: P3500-			orig.						
P3800-			orig.						

NAME: PMU88S-M128K 12NC: 5112 291 9580x	CONFIGURATION INDEX								
CONTENTS	MODIFICATION LEVEL x								
PAGE	1	2	3	4	5	6	7	8	9
- Contents 8-1	. . .	850801							
- Component Location 8-3	. . .	850801							
- Circuit Diagram 8-5	. . .	850801							
- Connector Layout 8-7	. . .	850801							
- Parts Location 8-10	. . .	850801							
- Parts List 8-11	. . .	850801							
- Printed Wiring 8-13	. . .	850801							
RELEVANT SI-NUMBER: P3500-		orig.							
P3800-		orig.							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C1
C2
C3
C4
C5
C6
C7
C8
IC1
IC5
IC9
IC13
IC17
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IC29
R12
R11
R14
R13
R16
R15
R18
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R64
R89
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C10
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C13
C14
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C16
IC3
IC7
IC11
IC15
IC19
IC23
IC27
IC31
C34
C17
C18
C19
C20
C21
C22
C23
C24
IC2
IC6
IC10
IC14
IC18
IC22
IC26
IC30
C33
IC 33
R83
C25
C26
C27
C28
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IC8
IC12
IC16
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IC24
IC28
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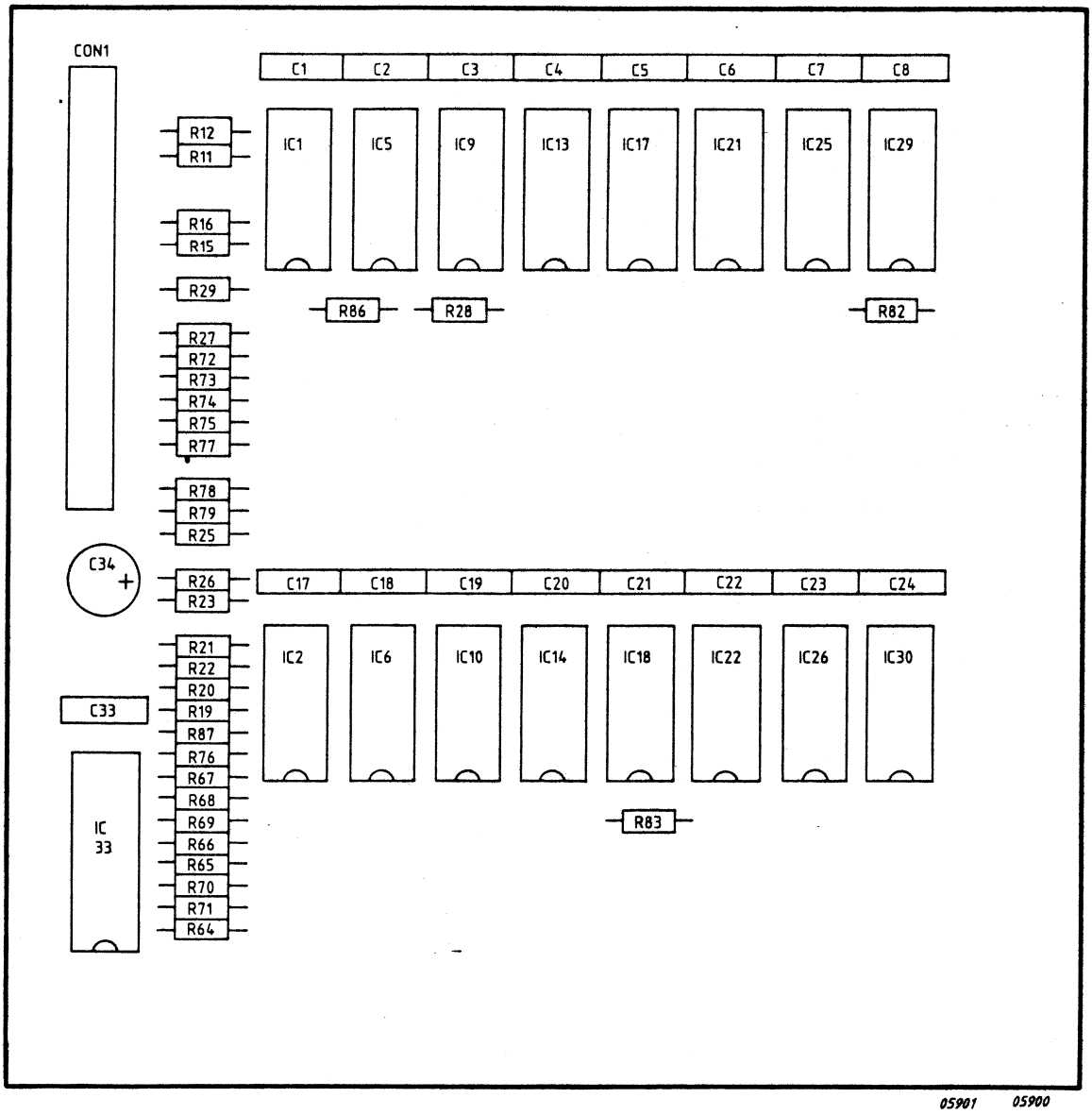
05897 A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C22
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C24
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IC6
IC10
IC14
IC18
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IC26
IC30
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R83
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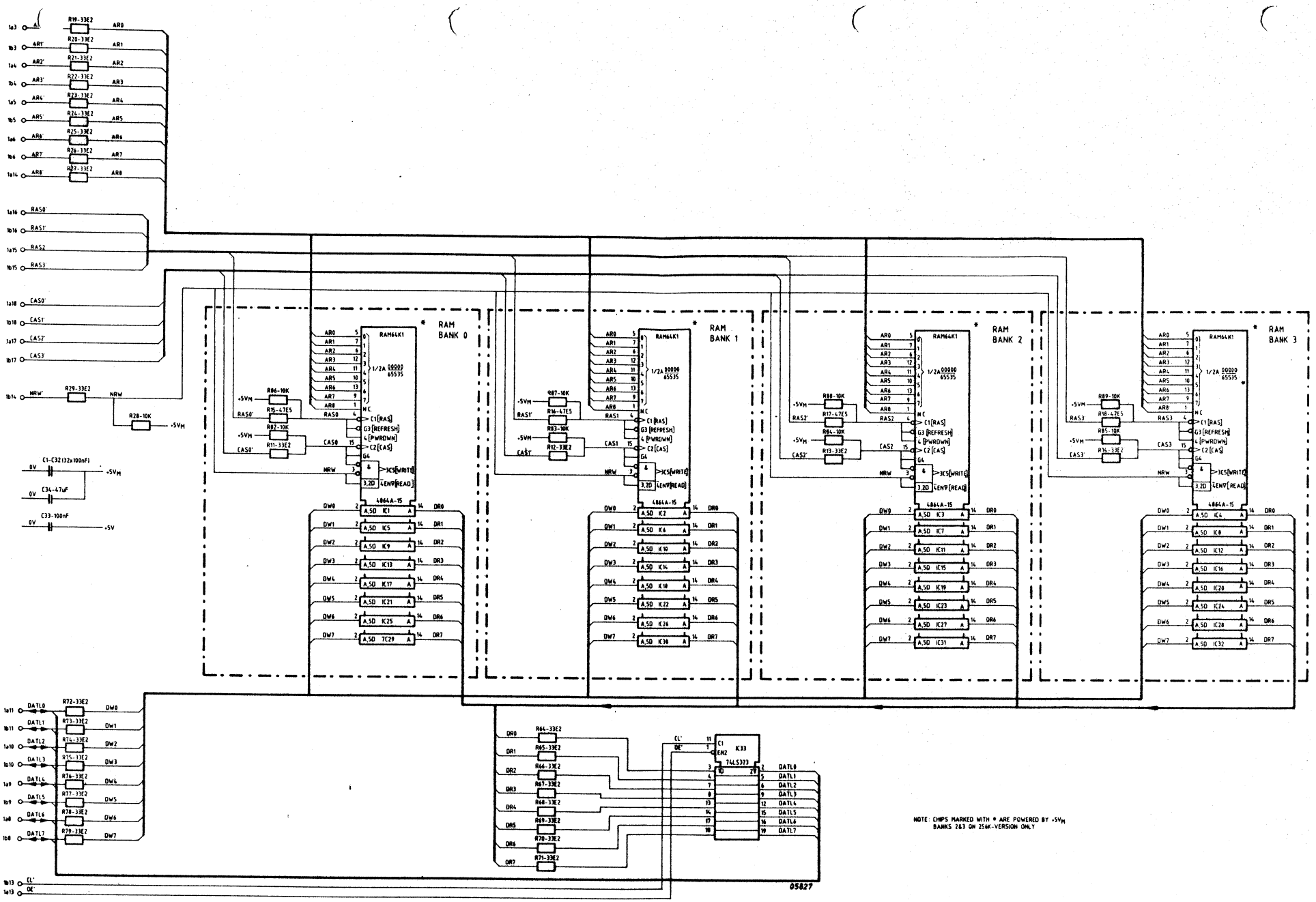
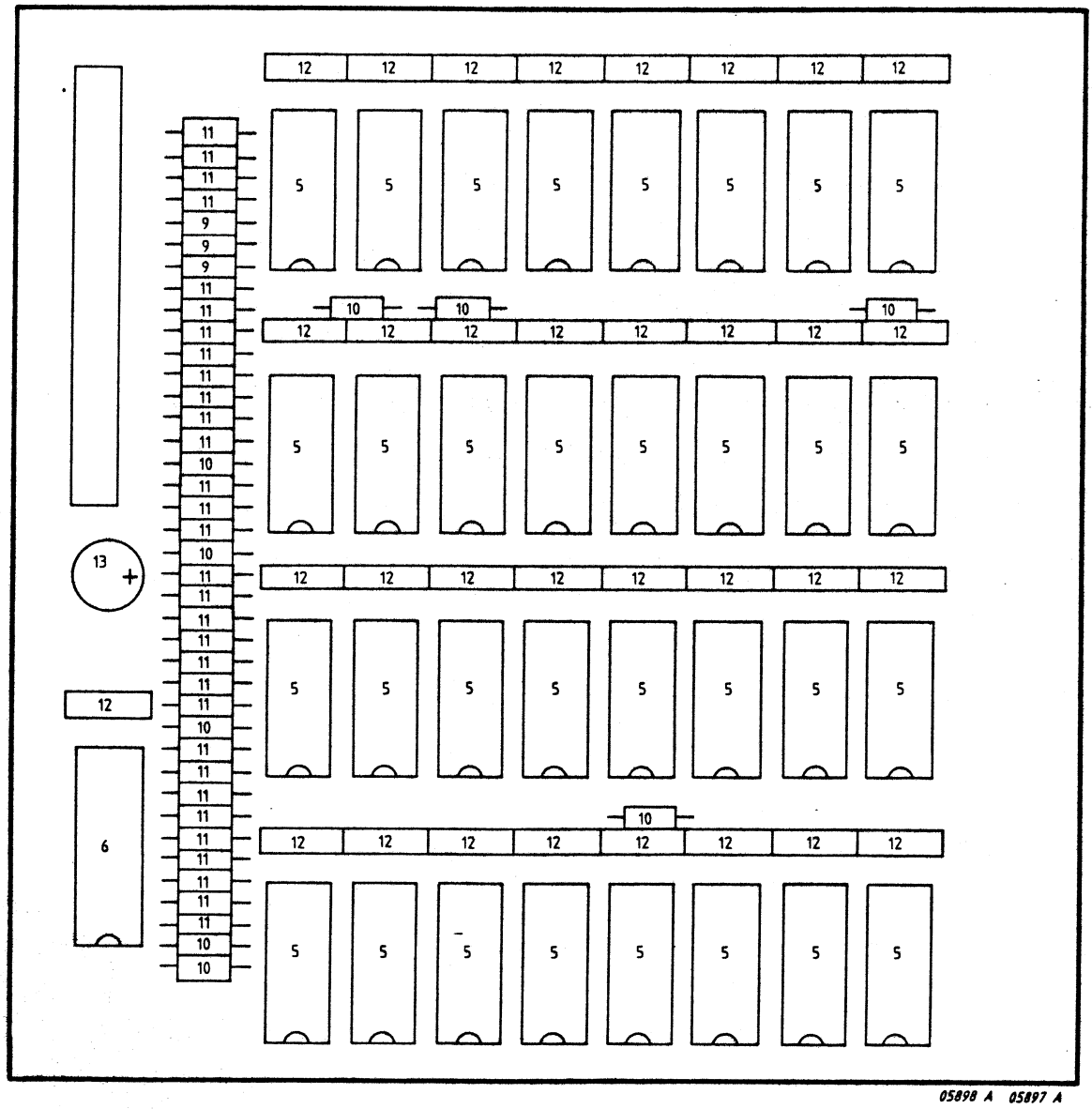


CIRCUIT DIAGRAM PMU88S-M/256K
PMU88S-M/128K
SHEET 1

CONNECTOR LAYOUT PMU88S-M/256K
PMU88S-M/128K

CONNECTOR 1

	a	b
1	0V	0V
2	+5V	+5VM
3	AR0'	AR1'
4	AR2'	AR3'
5	AR4'	AR5'
6	AR6'	AR7'
7		
8	DATL6	DATL7
9	DATL4	DATL5
10	DATL2	DATL3
11	DATL0	DATL1
12		
13	OE'	CL'
14	AR8'	NRW'
15	NRAS2'	NRAS3'
16	NRAS0'	NRAS1'
17	NCAS2'	NCAS3'
18	NCAS0'	NCAS1'
19	+5VM	+5VM
20	0V	0V


12
11
5
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13
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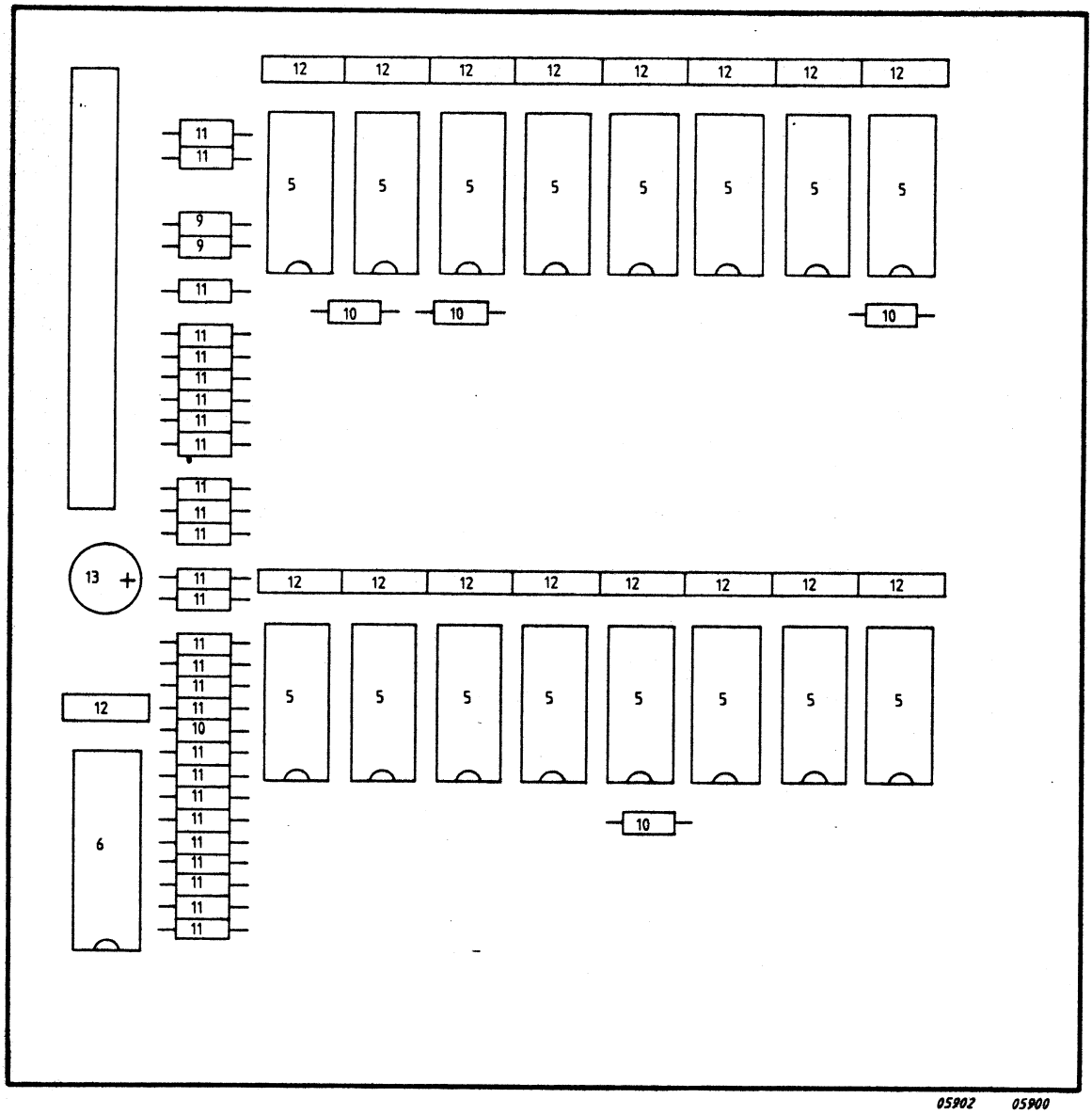
9
05898 A
05897 A

PARTS LIST PMU88S-M/256K (5112 291 9576X)

Pos.	Art. Nr.	12-NC	Description
5	9336 966 30112	5322 209 82822	IC HM4864AP-15
6	9334 534 00112	5322 209 86062	IC SN74LS373J
10	2322 151 51003	4822 116 51253	Resistor 10K, 1%, 0.4W
11	2322 151 53329	5322 116 50527	Resistor 33E2, 1%, 0.4W
12	9912 202 52151	5322 122 10313	Capacitor 100nF
13	2020 002 90542	5322 124 21335	Capacitor 33uF, 25V
9	2322 151 54759	5322 116 50952	Resistor 47E5, 1%, 0.4W


12
11
9
10
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05902
05900

PARTS LIST PMU88S-M/128K (5112 291 9580X)

Pos.	Art. Nr.	12-NC	Description
5	9336 966 30112	5322 209 82822	IC HM4864AP-15
6	9334 534 00112	5322 209 86062	IC SN74LS373J
10	2322 151 51003	4822 116 51253	Resistor 10K, 1%, 0,4W
11	2322 151 53329	5322 116 50527	Resistor 33E2, 1%, 0.4W
12	9912 202 52151	5322 122 10313	Capacitor 100nF
13	2020 002 90542	5322 124 21335	Capacitor 33uF, 25V
9	2322 151 54759	5322 116 50952	Resistor 47E5, 1%, 0.4W