Hardware Software Interface Manual
P3000

Data
Systems

PHILIPS

TABLE OF CONTENTS

1.1. Hardware structure

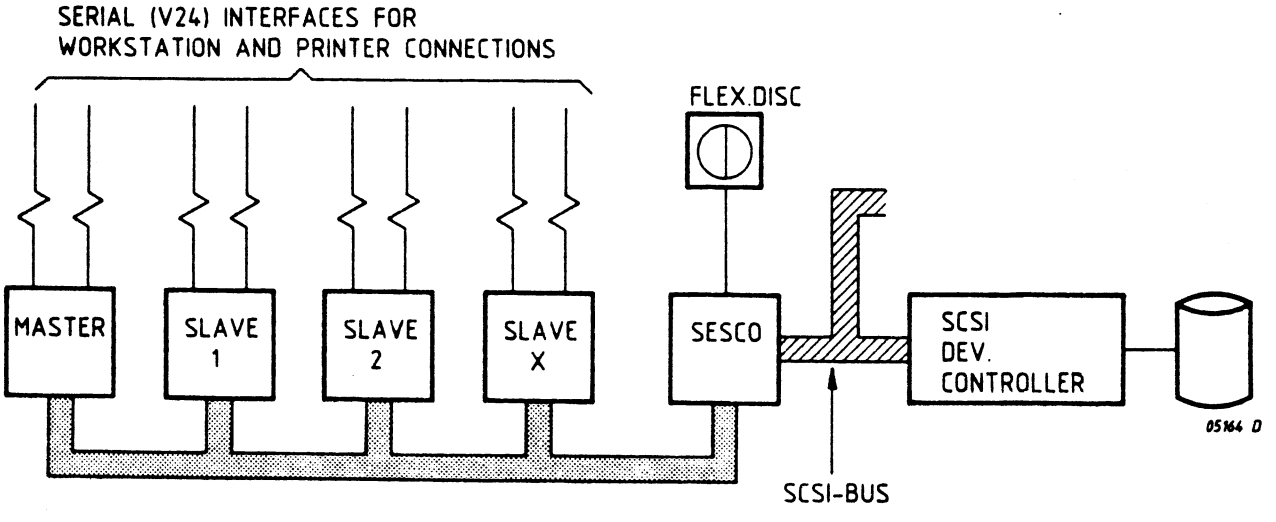
The P3500 / P3800 System is a multi-processor microcomputer system. Each user workstation is attached to a single board computer, called " Slave " processor. Either an 8-bit processor (PMU 80) or a 16-bit processor (PMU 186) can be used as slave processor.
On this board all the local processing is performed.

One processor, called "Master "or "File Master" , is added to the system. This processor (PMU 80) performs all the disk file access and controls the Shared printers.

Apart from these master and slave processors, one or more processors may be added to perform special tasks such as Batch Processing and Data Communication.

The Flexible disc control and adaption to the standard SCSI bus is done by the SESCO board, connected to the system bus.
Control of Fixed Disc and Disc Extensions is done by separate controller boards , mounted to the drive electronics.

A single user version of the system is also available.
In this case the local user processing is also executed by the master, which is the only processor in the system.



1.2 HW/SW Interface

In this manual the Hardware Software Interface is described as the lowest level on which the hardware can be accessed by machine language programs.

This is certainly not the level at which users or programmers are permitted to access the hardware. Several SSS publications describe the interfaces of the machine for users and programmers.

Information offered by this manual is to be used only by qualified Philips Specialists, as a tool for understanding and special repair activities.

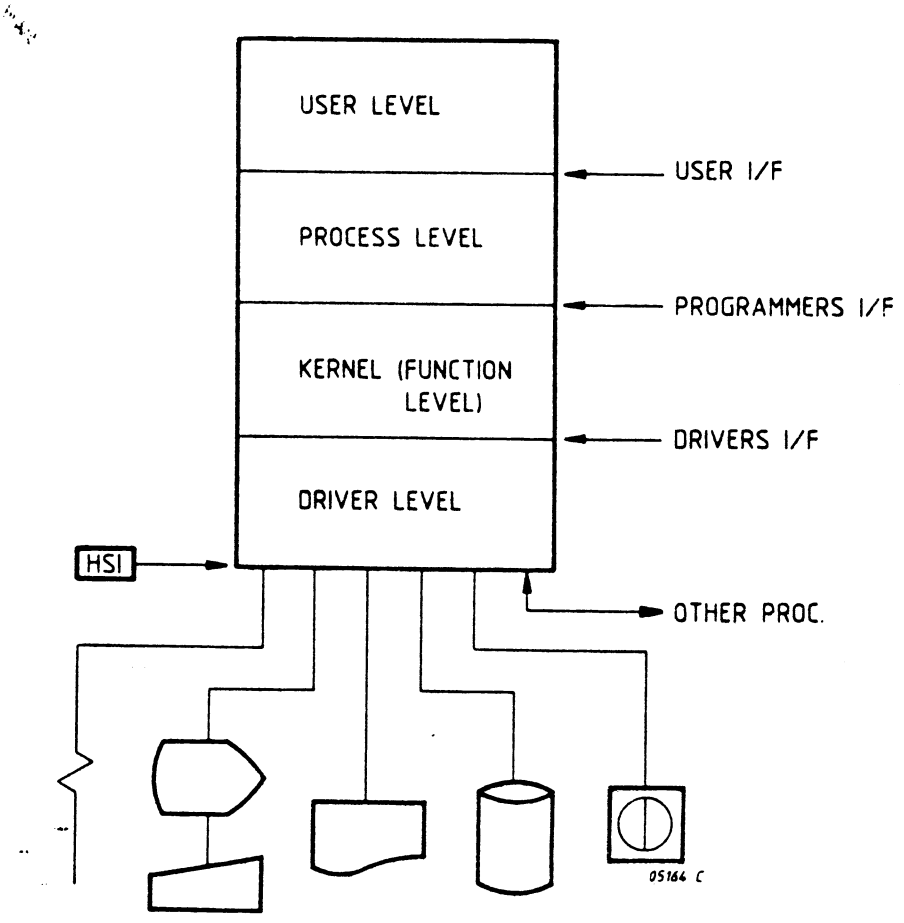


Fig.1.2 Software structure

Continue Next Page.

2.1 Z80 MICROPROCESSOR

For a description of the instruction set as well as all other relevant information refer to:

Training Manual Z80 , 12NC : 5122 991

2.1.1 Timing

The microprocessor is of the type Z80A.
The processor frequency is 3.6864 MHz for PMU 80-1
6.0000 MHz for PMU 80-3

The next timing states are required:

- Local Memory Access Fetch : 5 clock cycles
  Read : 3 clock cycles
  Write : 4 clock cycles (3 for PMU 80-3)
- I/O Access : 4 clock cycles
- Interrupt Acknowledge : 5 clock cycles (7 for PMU-80-3)

For System Bus Access additional clock cycles due to bus arbitration are required.

2.1.2 Interrupt System

The PMU 80 uses Interrupt Mode 2 of the Z80 Processor.
In this mode the interrupting device offers a "type code" to the processor in the Interrupt Acknowledge cycle. This type code points to a memory based vector table containing the start address of the interrupt service routine.

The Non Maskable interrupt input of the Z80 Processor is not used.

2.2 MEMORY SYSTEM

2.2.1 Local and System Memory

The processor board PMU-80 contains a number of memories, accessable by the Z-80 processor. This is called the "local" memory.
A "master" processor can also access memory on other boards.
This is called the "system" memory.

The local memory is formed by:

- 64 KB RAM

- 8 KB ROM devided in two pages of 4 KB :

  - 4 KB IPL-ROM
  - 4 KB TEST-ROM

The system memory is formed by the 64 KB RAM areas of all the "slave" processors, the hardware allows access to upto 15 slave memories.

2.2.2 Memory Mapping

The memory mapping unit takes care of mapping either the ROM, local RAM or system RAM into the address space of the Z-80.

The mapping unit regards the Z-80 address as 16 pages of 4 K each. Depending of the mapping mode, one page of Rom, Local Ram or System Ram is mapped in the Z-80 address space. The other 15 pages select the Local Ram.

The next four modes are supported:

- Mode 0 : Used at power-on

  Page 0 = TEST ROM
  Page 1-15 = Local RAM

- Mode 1 : Used at IPL time

  Page 0 = Local RAM
  Page 1 = IPL ROM or other ROM page
  Page 2-15 = Local RAM

- Mode 2 : Used in normal processing

  Page 0-15 = Local RAM

- Mode 3 : Used to access System memory

  Page 0 = Local RAM
  Page 1 = System RAM

2.2.3 Selection of Mapping Mode

Selection of mapping mode is done via two bits of output port 20.

For the PMU 80-3 this port can only be used after initialization of the Z8536 CIO according to section 2.5.

Output Port 20H

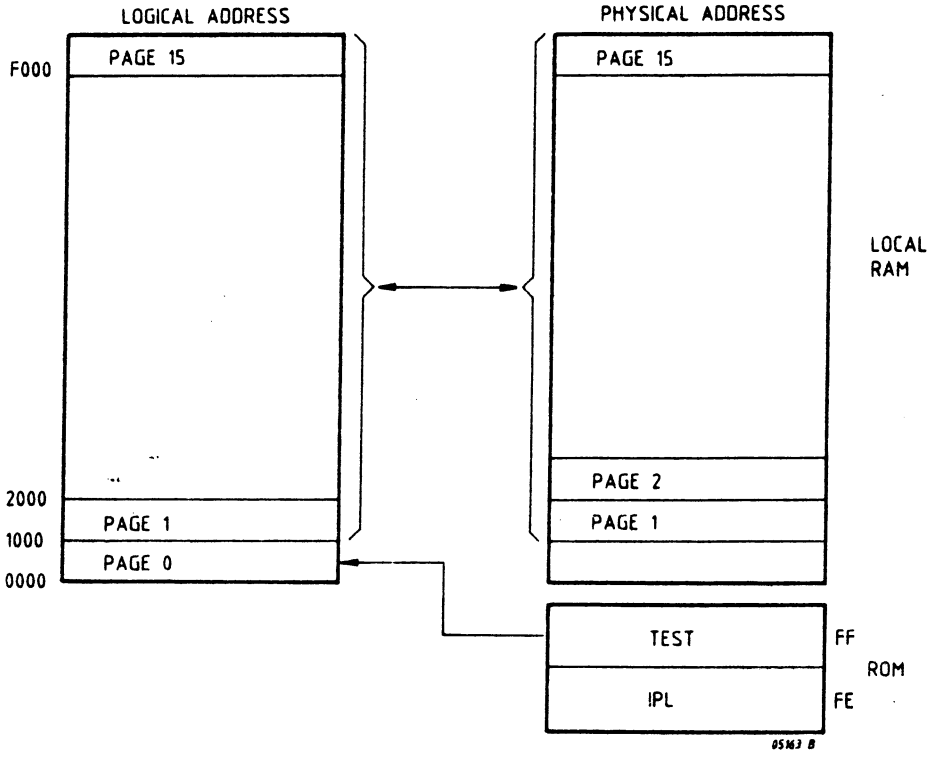
7	6	5	4	3	2	1	0

0	0	MODE 0 (TEST)
0	1	MODE 1 (IPL)
1	0	MODE 2 (LOCAL RAM)
1	1	MODE 3 (SYSTEM RAM)

TurboDOS keeps a copy of this output port at address 0008 H .

2.2.3.1 Mode 0

Page 0 of the processor address space is mapped to page FF of local memory extension (= Rom address 1000H-1FFFH > TEST ROM)



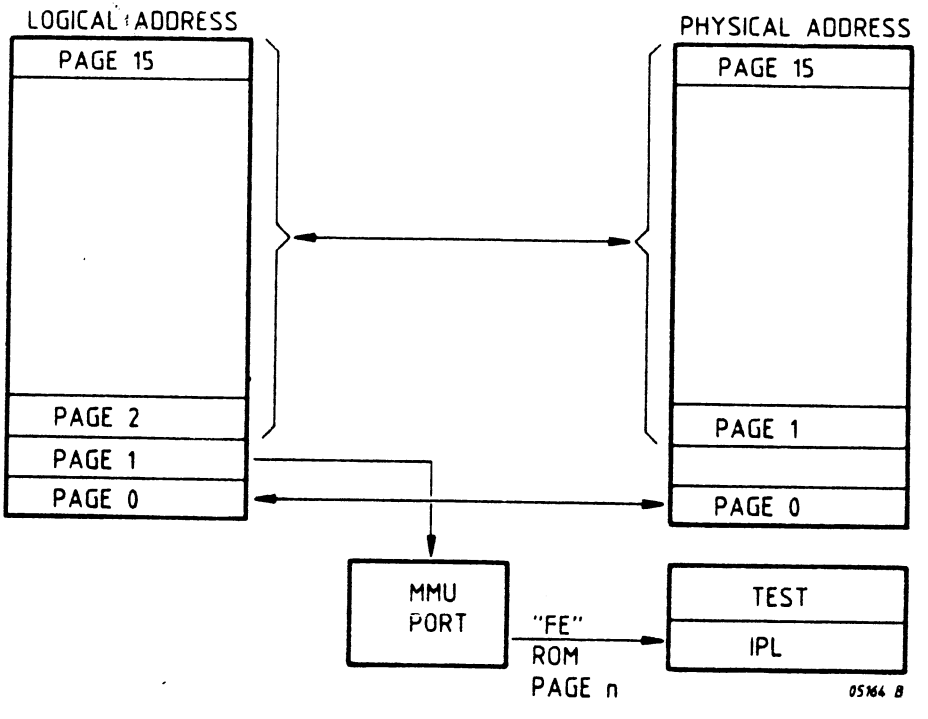
2.2.3.2 Mode 1

The MMU port (24 H) contains the Local memory extension page number which is mapped in page 1 of the processors map.

Port 24H = FFH >>> TEST ROM (Rom address 1000H-1FFFH)

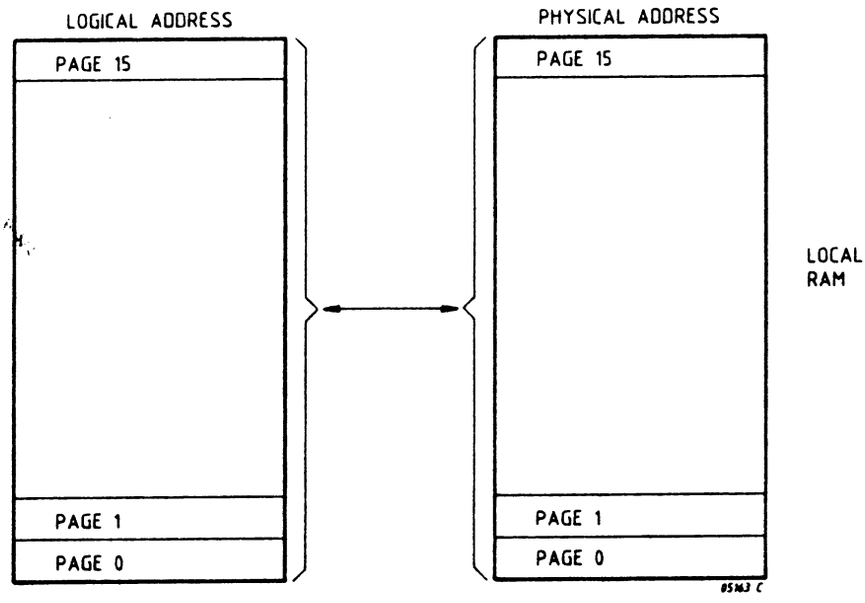
Port 24H = FEH >>> IPL ROM (Rom address 0000H-0FFFH)

To select the IPL Rom, the MMU port (24H) is set to FEH before the mapping is switched to Mode 1.



2.2.3.3 Mode 2

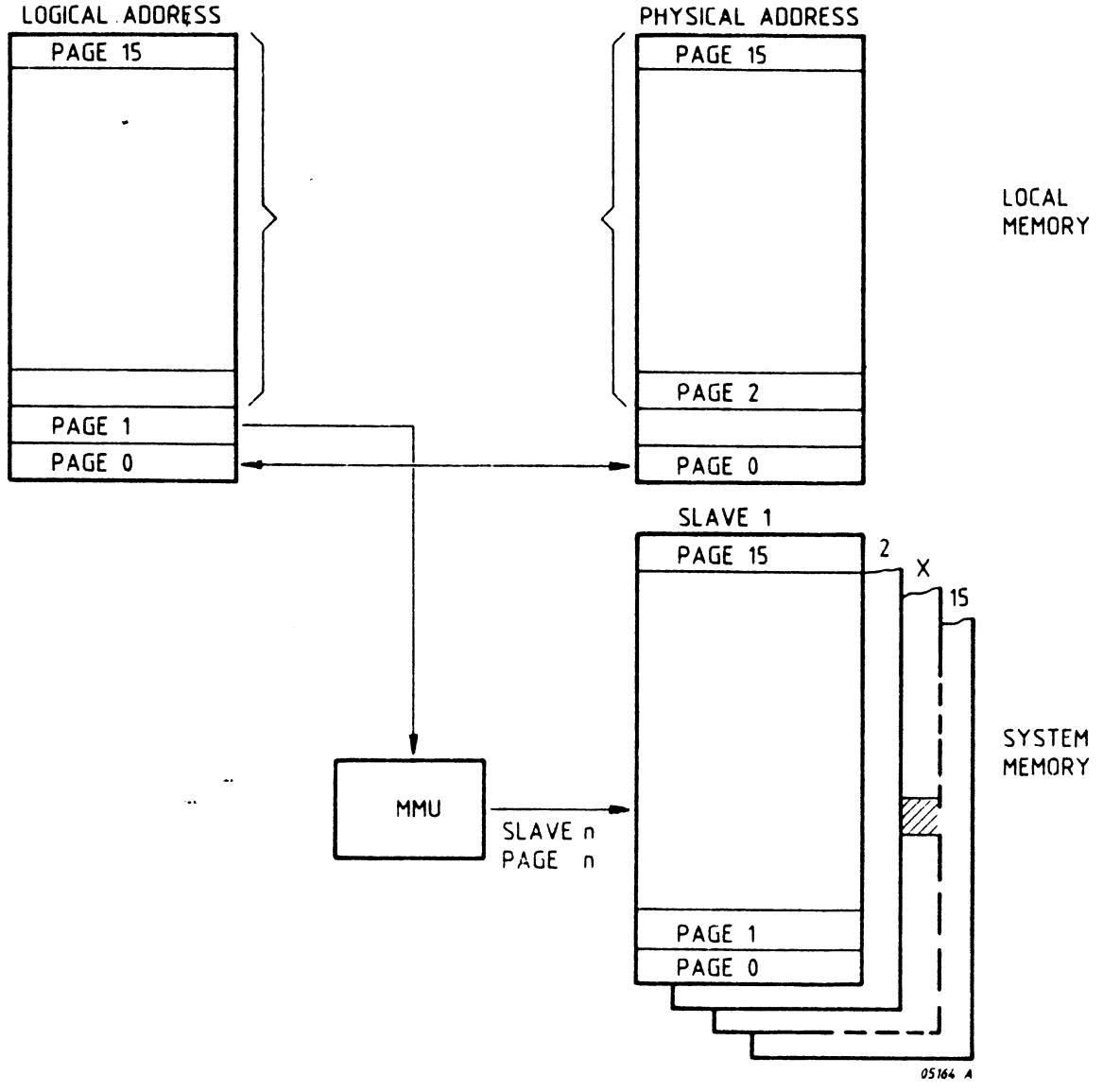
In this mode the processor address space is fully mapped to Local memory.



2.2.3.4 Mode 3

In this mode page 1 of the processor is pointing to the system memory on the EMM-bus. The Slave number and page number to be addressed are stored in the MMU-port.

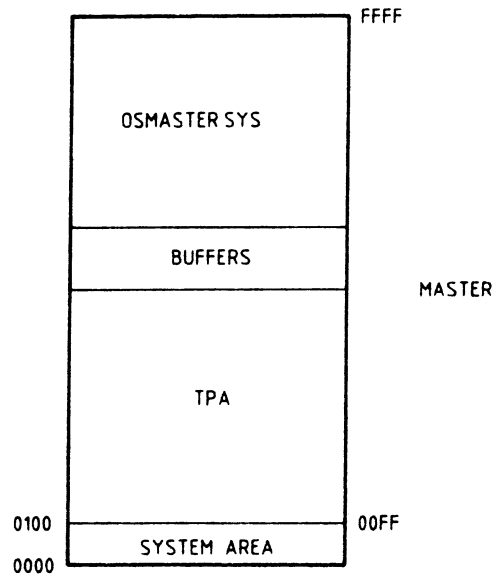
Port 24H	7	6	5	4	3	2	1	0	OUTPUT
	SLAVE				PAGE				

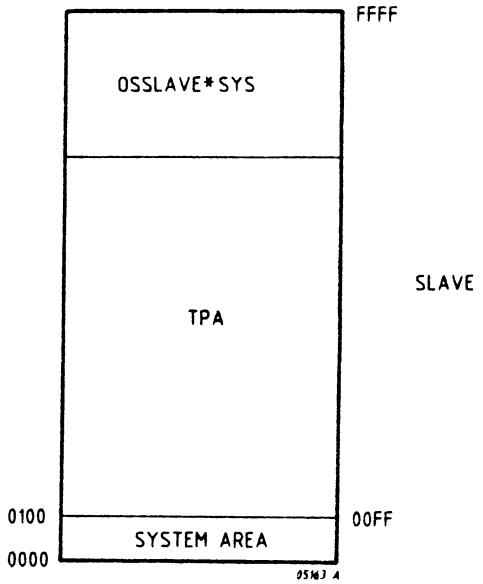


2.2.4 Memory Layout (TurboDOS)

2.2.4.1 TurboDOS Memory Occupation

The 64KB Ram Memory is used by TurboDOS according to the next figure for a Master and Slave respectively:





2.2.4.2 TurboDOS System Memory Area

The first 100H addresses in RAM are used by TurboDOS for several system functions, bus transfers, inside test,test and diagnostis, interrupts, power faillure routines etc.

2.2.4.2.1 System Area (Rel. 1/2)

```
0000-0002H      JMP WARMSTRT
0004H           DEFAULT USER/DRIVE NUMBER
0005-0007H      JMP TurboDOS
0008H           COPY OF OUTPUT PORT 20H
0009H           COPY OF SASI CONTROL PORT 2 (Master)
000AH           TDIND     ;Test & Diagnostic Indicator
0008-000CH      TDADDR    ;Address of T&D area within SP-driver
000DH           IPLFLG    ;IPL/Power-off flags (See 2.4.1.2)

000E-002FH      INTERRUPT VECTOR TABLE
000E-000FH      CTCIV     ;Timer
0010-0011H      PFLIV     ;Power failure Line
0012-0013H      RESIV     ;Reserved
0014-0015H      MSCIV     ;Master Slave Control
0016-0017H      TOFIV     ;Terminal OFf
0018-0019H      SASIV     ;SASI-Port(SCSI Bus)
001A-001BH      RES
001C-001DH      RES
001E-001FH      FDCIV     ;Flexible Disc Controller
0020-0021H      SIATIV    ;SIO-Channel A transmit-buffer-empty
0022-0023H      SIAEIV    ;               external-status
0024-0025H      SIARIV    ;               received-character
0026-0027H      SIASIV    ;               special-condition
0028-0029H      SIBTIV    ;SIO-Channel B transmit-buffer-empty
002A-002BH      SIBEIV    ;               external-status
002C-002DH      SIBRIV    ;               received-character
002E-002FH      SIBSIV    ;               special-condition

0040-0048H      MASTER-SLAVE COMMUNICATION AREA (See 2.3.4)
0049-004AH      RSTADR    ;Restore Address after Power Break Down
004C-0059H      INSADR    ; INSIDE TEST AREA (See 2.4.5)
005BH           CONTROLLER ERROR BYTE (T&D)
005C-007FH      DEFAULT FILE CONTROL BLOCK (TurboDOS)
0080-00FFH      DEFAULT DMA BUFFER ADDRESS (TurboDOS)
FFFEH           PBDFLG    ;Power Break Down Flag
```

2.2.4.2.2 System Area (Rel.3)

```
0000-0002H    JMP WARMSTRT
0004H         DEFAULT USER/DRIVE NUMBER
0005-0007H    JMP TurboDOS (C-Functions)
0008H         COPY OF OUTPUT PORT 20H
0009H         COPY OF SASI CONTROL PORT 2
000AH         TDIND     ;Test & Diagnostic Indicator
000B-000CH    TDADDR    ;Address of T&D area within SP-driver
000DH         IPLFLG    ;IPL/Power-off flags (See 2.4.1.2)

              INTERRUPT VECTOR TABLE PMU 80-1
000E-000FH    CTCIV     ;Timer
0010-0011H    PFLIV     ;Power failure Line
0012-0013H    RESIV     ;Reserved
0014-0015H    MSCIV     ;Master Slave Control
0016-0017H    TOFIV     ;Terminal OFf
0018-0019H    SASIV     ;SASI-Port(SCSI Bus)
001A-001BH              ;RESERVED
001C-001DH              ;RESERVED
001E-001FH    FDCIV     ;Flexible Disc Controller
0020-0021H    SIBTIV    ;SIO-Channel B transmit-buffer-empty
0022-0023H    SIBEIV    ;              external-status
0024-0025H    SIBRIV    ;              received-character
0026-0027H    SIBSIV    ;              special-condition
0028-0029H    SIATIV    ;SIO-Channel A transmit-buffer-empty
002A-002BH    SIAEIV    ;              external-status
002C-002DH    SIARIV    ;              received-character
002E-002FH    SIASIV    ;              special-condition
              INTERRUPT VECTOR TABLE PMU 80-3
000E-000FH    RTCIVW    ;Timer
0010-0011H    FLDIV3    ;Flexible Disc Controller
0012-0013H              ;Reserved
0014-0015H              ;Reserved
0016-0017H    SASIV3    ;SASI-port (SCSI Bus)
0018-0019H    TOFIV3    ;Terminal OFf
001A-001BH    MSCIV3    ;Master Slave Control
001C-001DH    FIFOIV    ;FIFO Port
001E-001FH    PFLIV3    ;Power Failure Line
0020-0021H    SIBTIV    ;SCC-Channel B transmit-buffer-empty
0022-0023H    SIBEIV    ;              external-status
0024-0025H    SIBRIV    ;              received-character
0026-0027H    SIBSIV    ;              special-condition
0028-0029H    SIATIV    ;SCC-Channel A transmit-buffer-empty
002A-002BH    SIAEIV    ;              external-status
002C-002DH    SIARIV    ;              received-character
002E-002FH    SIASIV    ;              special-condition

0040-0048H    MASTER-SLAVE COMMUNICATION AREA (See 2.3.4)
0049-004AH    RSTADR    ;Restore Address after Power Break Down
004B          CIRCUT    ; CIRCUiT empty indicator
004C          LAMP FIELD T&D
004D-004EH    ADDRESS T&D AREA (See section 2.4.5)
0050-0052H    JMP TurboDOS (T-Functions)
0059H         CONCHA    ;Copy of TurboDOS CONsole Assignment CHannel
005AH         MSGINT    ;MeSsaGe INTerface byte (See 2.3.4.2)
005BH         CONTROLLER ERROR BYTE INSIDE TEST (See 2.4.5)
005C-00FFH    DEFAULT FCB / DMA Address (TurboDOS)
FFFEH         PBDFLG    ;Power Break Down Flag
```

2.3 Input/Output System PMU 80 / PMU 80-1

This section gives the programming information for the PMU-80 on HSI-level. As much as possible the default settings for the TurboDOS System are given.

2.3.1 Real Time Clock

The Processor Board includes a programmable Z80-CTC device. Channel 3 of this CTC is used to generate an RTC interrupt.

Before loading the timer, the interrupt vector of the CTC has to be programmed. This is done by sending the next byte to channel 0 of the CTC:

Port 04H	7	6	5	4	3	2	1	0	OUTPUT
	0	0	0	0	1	1	1	0	Default 0EH
								0	vector word
						X	X		not used
	I	I	I	I	I				interrupt vector

Bit 1 and 2 of the vector word are supplied by the CTC, and filled with the channel number. The default interrupt vector points to address 000E-000FH for the RTC interrupt.

To program the CTC the next two bytes must be send to Port 07H:

Channel control word:

Port 07H	7	6	5	4	3	2	1	0	OUTPUT
	1	0	1	1	1	1	1	1	Default 0BFH
								1	control word
							1		software reset
						1			time constant follows
					1				automatic trigger
				1					trigger edge +
			1						prescaler value = 256
		0							timer mode
	1								interrupt enable

Time Constant Word:

Port 07H	7	6	5	4	3	2	1	0	OUTPUT
	1	1	1	1	0	0	0	0	default 0F0H for 60Hz

Frequency= 3.6864 MHz /binary value x prescaler(256)

2.3.2 Serial Interfaces

The PMU-80 provides two serial interfaces:

Channel A, a full V24-interface
Channel B, a short distance interface

These interfaces are controlled via a dual-channel Z80-SIO and two control ports: input port 20H and output port 20H.
For asynchronous communication also the Z80-CTC is used to provide the baud rate clocks for both channels.

The bit assignment of these ports is given in section 2.3.2.3

The next procedure must be used to perform a serial data transmission:

- Program the Z80-CTC for the required speed
- Program the Z80-SIO mode of operation
- Program Output Port 20H to set the required V24 signals
- Check Input Port 20H for correct return signals
- Program the Z80-SIO command (write and/or read)
- Wait for interrupts from Z80-SIO

The interrupt routine should check the SIO status and react on this with either send or receive data actions.

A SIO Write or Read Register cannot be accessed directly.
Before any write or read action to the SIO Internal registers, the particular register has to be selected.

This is done by sending the address of the register to be selected to the Command Register.

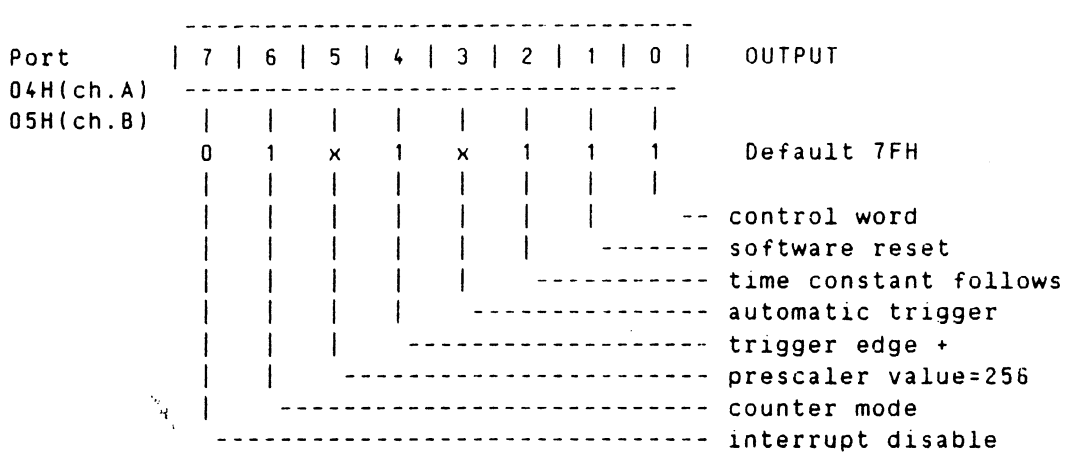
The next ports are assigned to the Z80-SIO:

PORT 00 H	DATA REGISTER	CHANNEL A
PORT 01 H	DATA REGISTER	CHANNEL B
PORT 02 H	COMMAND REGISTER	CHANNEL A
PORT 03 H	COMMAND REGISTER	CHANNEL B

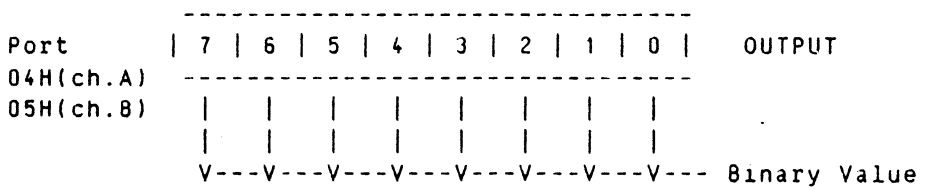
2.3.2.1 Programming the Baud Rate

When the PMU-80 is strapped for internal clocks, channel 0 and 1 of the CTC deliver the required clocks for channel A and B respectively. The next two bytes must be send to the required CTC Channel:

Channel Control Word:



Time Constant Word:



The frequency of the Baud Rate Clock must be calculated as follows:

f=921.6 KHz : binary value for channel B

f=460.8 KHz : binary value for channel A

Some Binary Values for standard Baud Rates:

Speed	port 04(ch.A)	port 05(ch.B)
19.200 KB	--------	03H
9.600	03H	06H
4.800	06H	0CH
2.400	0CH	18H
1.200	18H	30H

NOTE: The frequencies delivered in these examples are 16x the actual Baud Rate, because for asynchronous communications the Z80-SIO is normally programmed for a 16 x clock.
If this clock is used in synchronous applications as clock to modem (CT113), the programming values should be multiplied by 16.

2.3.2.2 CHANNEL A INTERFACE CONTROL

The next interface signals are used at channel A, the list explains via which port the signals can be accessed.

PIN	CCITT	NAME	I/O	PORT	BIT	DESCRIPTION
b1	101	GND	------			
b7	102	L	------			
b2	103	TMD	OUT	00H	0-7	DATA OUT
b3	104	RCD	IN	00H	0-7	DATA IN
b4	105	RTS	OUT	WR5	1	REQUEST TO SEND
b5	106	CTS	IN	RR0	5	CLEAR TO SEND
b6	107	DSR	IN	20H	7	DATA SET READY
a7	108.2	DTR	OUT	WR5	7	DATA TERMINAL READY
b8	109	DCD	IN	RR0	3	CARRIER DETECTED
a10	111	DRS	-------			HIGH
a11	113	TSET(M)	-------			INT.CLOCK TO MODEM(x16!)
a2	114	TSET	Strap			SYNCHR.TXCLOCK FROM MODEM
a4	115	RSET	Strap			SYNCHR.RXCLOCK FROM MODEM
a9	125	RIN	IN	RR0	4	CALLING INDICATOR
a8	140	REML	OUT	20H	6	REMOTE LOOP SETTING
a5	141	LOCL	OUT	20H	5	LOCAL LOOP SETTING
a12	142	TIN	IN	20H	6	TEST INDICATOR
			IN	20H	3	RPON (CT109/CT125)

NOTE: CT109 and CT125 can be strapped to supply Remote Power ON (RPON).
CT109 or CT125 can be read at port 20H, bit 3.

2.3.2.3 Channel B Interface Control

Channel B has limited control features . It is designed as Short Distance Interface, for direct connection of peripherals.
The next interface signals are used at channel B, the list explains via which port the signals can be accessed.

PIN	CCITT	NAME	I/O	PORT	BIT	DESCRIPTION
b1	101	GND	------			
b7	102	L	------			
b3	104	RCD	OUT	01H	0-7	DATA OUT
b2	103	TMD	IN	01H	0-7	DATA IN
b5	106	CTS	OUT	WR5	7	CLEAR TO SEND (= SIO-DTR)
b6	107	DSR	IN	RR0	5	LOOPED FROM DSR(= SIO-CTS)
a7	108.2	DTR	IN	20H	5	DATA TERMINAL READY(RPON)

NOTE: CT108.2 can be strapped to give Remote Power ON (RPON).
RPON condition can be read at port 20H, bit 5.

2.3.2.4 Internal Registers SIO

The Z80-SIO contains a number of Write and Read registers. A particular register is accessed in two steps:

First the register number to be accessed is written into the SIO - Command Register (WR0)- , then the information to or from the register can be read or written.

WRITE REGISTER 0 - COMMAND REGISTER

```
          ---------------------------------
Port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
02H(ch.A) ---------------------------------
03H(ch.B)   |   |   |   |   |   |   |   |
            0   0   0   1   1   0   0   0     Default 18H
            |   |   |   |   |   |   |   |
            |   |   |   |   |   Next Byte Pointer
            |   |   |   |   |   0   0   0  - register 0
            |   |   |       |   0   0   1  - register 1
            |   |   |   |   |   0   1   0  - register 2
            |   |   |   |   |   0   1   1  - register 3
            |   |   |   |   |   1   0   0  - register 4
            |   |   |   |   |   1   0   1  - register 5
            |   |   command code
            |   |   0   0   0  - null code
            |   |   0   0   1  - send abort(SDLC)
            |   |   0   1   0  - reset ext.status interrupts
            |   |   0   1   1  - channel reset
            |   |   1   0   0  - enable int. on next Rx char.
            |   |   1   0   1  - reset Tx int. pending
            |   |   1   1   0  - error reset
            |   |   1   1   1  - return from int.(CH.A only)
            reset code
            0   0  - null code
            0   1  - reset Rx CRC checker
            1   0  - reset Tx CRC generator
            1   1  - reset Tx underrun/ EOM latch
```

WRITE REGISTER 1 - INTERRUPT CONTROL

```
          ---------------------------------
port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
02H(ch.A) ---------------------------------
03H(ch.B)   |   |   |   |   |   |   |   |
            0   0   0   1   0   0   0   0    Default 10H
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 -- ext.interrupt enable
            |   |   |   |   |   |   1 ------ Tx interrupt enable
            |   |   |   |   |   1 ---------- status affects vector
            |   |   |   0   0 -- Rx int disable
            |   |   |   0   1 -- Rx int on first character
            |   |   |   1   0 -- int on all Rx char.(PE to IV)
            |   |   |   1   1 -- int on all Rx char.(no PE to IV)
            |   |   |
            |   |   1 - wait/ready on Rx/Tx
            |   1 ----- wait-n/ready function
            1 --------- wait/ready enable
```

WRITE REGISTER 2 - INTERRUPT VECTOR (CHANNEL B ONLY)

```
          ---------------------------------
Port 03H  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
          ---------------------------------
            |   |   |   |   |   |   |   |
            0   0   1   0   1   1   0   0     Default 2CH
```

Binary Value = Interrupt Vector

If write register 1, bit 2 is set the interrupt vector is modified as follows, to offer the interrupt vectors as stated in section 2.2.4.2

Bit 3 Channel A=0 B=1
Bit 2 Direction T=0 R=1
Bit 1 Comm/Data D=0 C=1

WRITE REGISTER 3 - RECEIVER CONTROL

```
          ---------------------------------
Port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
02H(ch.A) ---------------------------------
03H(ch.B)   |   |   |   |   |   |   |   |
            1   1   0   0   0   0   0   1     Default 0C1H
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 -- Receive Enable
            |   |   |   |   |   |   1 ------ Sync Char. Load Inhibit
            |   |   |   |   |   1 ---------- Address Search Mode(SDLC)
            |   |   |   |   1 -------------- Rx CRC Enable
            |   |   |   1 ------------------ Enter Hunt Phase
            |   |   1 ---------------------- Auto Enables
            0   0 -- Rx 5-bits/character
            0   1 -- Rx 7-bits/character
            1   0 -- Rx 6-bits/character
            1   1 -- Rx 8-bits/character
```

WRITE REGISTER 4 - RECEIVE/TRANSMIT CONTROL

```
          ---------------------------------
Port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
02H(ch.A) ---------------------------------
03H(ch.B)   |   |   |   |   |   |   |   |
            0   1   0   0   0   1   0   0     Default 44H
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 -- Parity Enable
            |   |   |   |   |   |   1 ------ Parity Even/Odd-N
            |   |   |   |   0   0 - Synchronous Mode
            |   |   |   |   0   1 - 1 stopbit/char
            |   |   |   |   1   0 - 1.5 stopbit/char
            |   |   |   |   1   1 - 2 stopbits/char
            |   |   0   0 - 8  bit sync character
            |   |   0   1 - 16 bit sync character
            |   |   1   0 - SDLC Mode
            |   |   1   1 - External Sync
            0   0 - x  1 Clock
            0   1 - x 16 Clock
            1   0 - x 32 Clock
            1   1 - x 64 Clock
```

WRITE REGISTER 5 - TRANSMITTER CONTROL

```
          ---------------------------------
port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
02H(ch.A) ---------------------------------
03H(ch.B)   |   |   |   |   |   |   |   |
            1   1   1   0   1   0   1   0    Default 0EAH
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 -- Tx CRC Enable
            |   |   |   |   |   |   1 ------ RTS
            |   |   |   |   |   1 ---------- SDLC-n/CRC16 Polynom.
            |   |   |   |   1 -------------- Tx Enable
            |   |   |   1 ------------------ Send Break
            |   0   0 - Tx 5 bits/character
            |   0   1 - Tx 7 bits/character
            |   1   0 - Tx 6 bits/character
            |   1   1 - Tx 8 bits/character
            |
            1 - DTR
```

WRITE REGISTER 6 - TRANSMIT SYNC CHARACTER

```
          ---------------------------------
port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
02H(ch.A) ---------------------------------
03H(ch.B)   |   |   |   |   |   |   |   |
```

Contains SYNC Character Code (Synchr. Mode)
or SDLC Address Field (SDLC Mode)

WRITE REGISTER 7 - RECEIVE SYNC CHARACTER

```
          ---------------------------------
port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
02H(ch.A) ---------------------------------
03H(ch.B)   |   |   |   |   |   |   |   |
```

Contains SYNC Character Code (Synchr. Mode)
or SDLC Address Field (SDLC Mode)

READ REGISTER 0 - STATUS

```
          ---------------------------------
port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   INPUT
02H(ch.A) ---------------------------------
03H(ch.B)   |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 -- Rx Char. Available
            |   |   |   |   |   |   1 ------ Int Pending (Ch.A only)
            |   |   |   |   |   1 ---------- Tx Buffer Empty
            |   |   |   |   1 -------------- DCD
            |   |   |   1 ------------------ Sync/Hunt(Ch.A:CT125)
            |   |   1 -------------------- CTS (Ch.B:CT108.2)
            |   1 ---------------------- Tx Underrun/EOM
            1 ------------------------ Break/Abort
```

READ REGISTER 1 - RECEIVE STATUS

```
          ---------------------------------
port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   INPUT
02H(ch.A) ---------------------------------
03H(ch.B)   |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 -- All Sent (Tx Empty)
            |   |   |   |   SDLC-Residue
            |   |   |   |   1   0   0       3 bits left in last I-word
            |   |   |   |   0   1   0       4
            |   |   |   |   1   1   0       5
            |   |   |   |   0   0   1       6
            |   |   |   |   1   0   1       7
            |   |   |   |   0   1   1       8
            |   |   |   |   1   1   1       9
            |   |   |   |   0   0   0      10 bits left in last I-word
            |   |   |   |
            |   |   |   1-- Parity Error
            |   |   1------ Rx Overrun Error
            |   1---------- CRC/Framing Error
            1-------------- End Of Frame(SDLC)
```

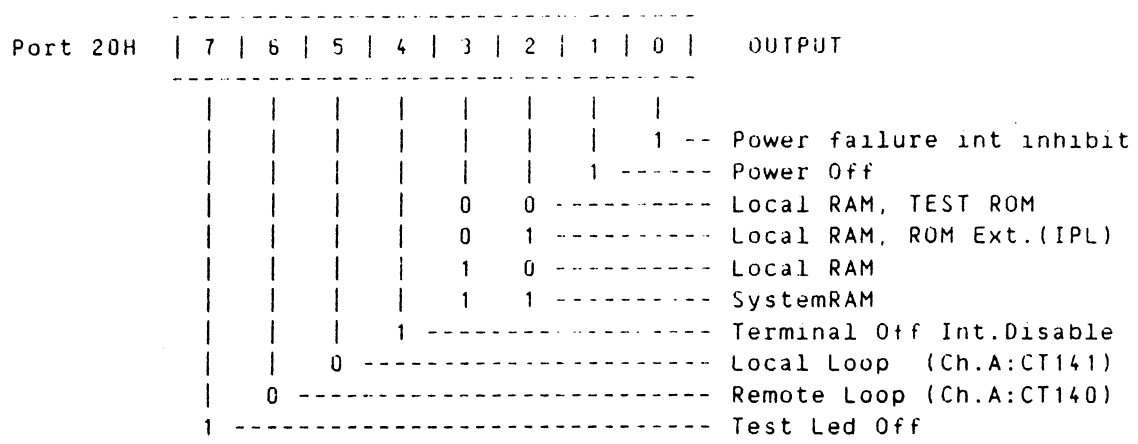
READ REGISTER 2 - INTERRUPT VECTOR (CHANNEL B ONLY)

```
          ---------------------------------
Port 03H  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   INPUT
          ---------------------------------
            |   |   |   |   |   |   |   |
```

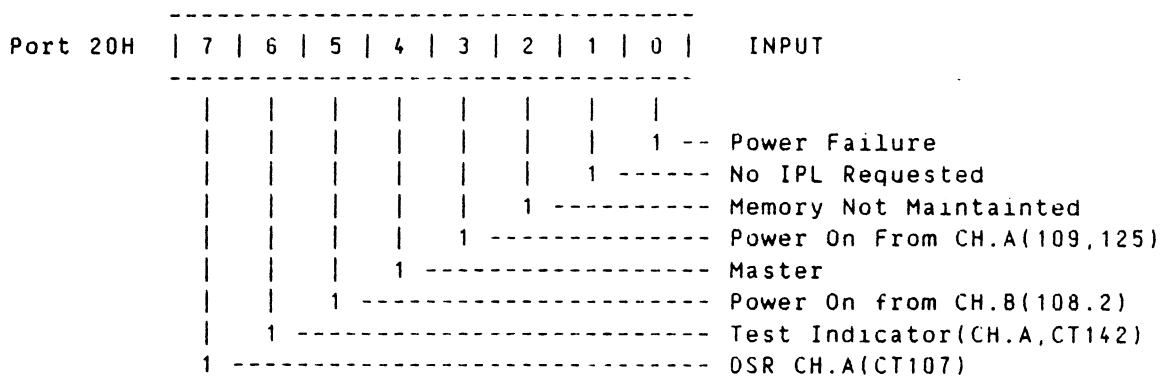
Contains (modified) Interrupt Vector
from WR2.

2.3.2.5 Control Port Overview

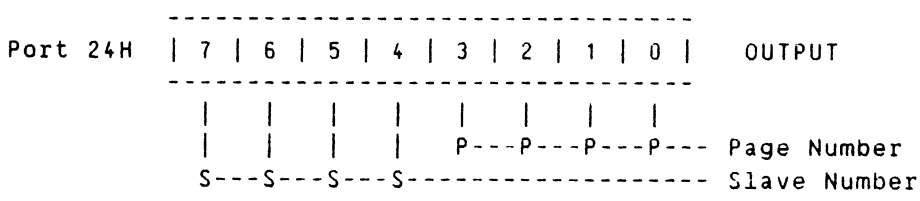
OUTPUT PORT 20H



INPUT PORT 20H



OUTPUT PORT 24H - MMU PORT



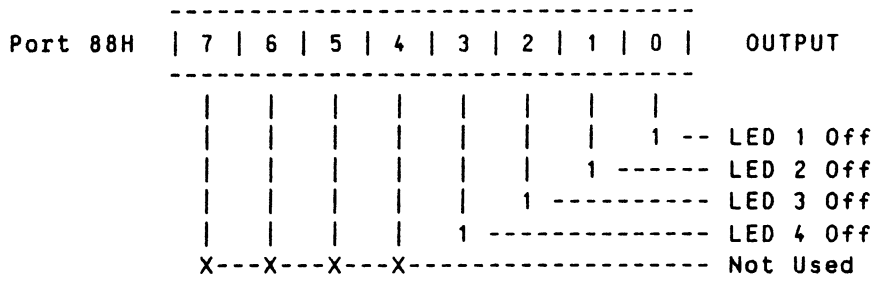
OUTPUT PORT 28H (CP3) - RESET M/S-COMMAND INTERRUPT

Any output to this port resets the Master/Slave Command interrupt. This interrupt can be set by the Master via the MSC- port (42H-5EH, bit 2).

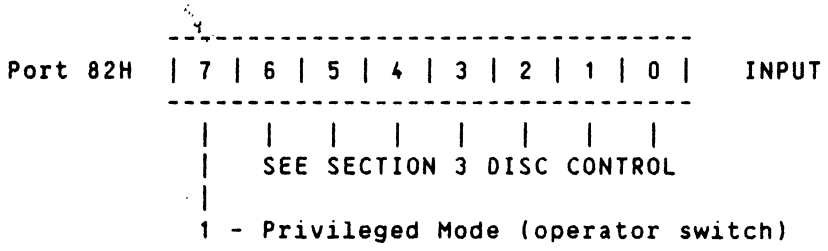
2.3.3 Operator Panel Control

Only the Master Processor has access to the operator panel.
The operator panel is connected to the SESCO board, accessable by the Master via the EMM-bus.

OPERATOR PANEL OUTPUT PORT (via SESCO)



OPERATOR PANEL INPUT (P3800 Only)



2.3.4 Master/Slave Control

The communication between master and slave boards is mainly executed via a polling mechanism of the Network Drivers, because the only way of communication between master and slaves is via the system memory mapping of the master.

2.3.4.1 Master/Slave Control Ports

Apart from the polling procedure, the master has access to the slaves via an I/O- port located at every slave.
This port is written to by the master, and cannot be accessed by the slave.

The port address depends on the slave number:

```
Port 42   Slave 1
     44   Slave 2
     46   Slave 3
     48   Slave 4
etc. till:
Port 5E   Slave 15
```

MASTER/SLAVE CONTROL PORT

```
          ---------------------------------
Port 42-  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
     5EH  ---------------------------------
            |   |   |   |   |   |   |   |
            X   X   X   X   X   |   |   0    Reset Slave
                                |   0 -----  IPL-request Slave
                                1 ---------  Interrupt  Slave
```

Bit 0 gives a hardware reset of the slave, this port excluded.
Bit 1 is read by the slave at Port 20H (bit 1), used to force the slave for a new IPL.
Bit 2 forces an MSC-interrupt at the slave, used to indicate a completed transfer.

2.3.4.2 Master/Slave Communication Area

The next bytes in the System area of the RAM are used to communicate between Master and Slave:

```
0040H     MSCMD     MASTER-SLAVE COMMAND BYTE

Bit  7    ----------
     6    terminal-off handling active        ;set by slave
     5    < Rel.2.1:receive-ready             ;set by master
     4    < Rel.2.1:send-ready                ;set by master
     3    ------------
     2    intermediate-boot-code-available    ;set by master
     1    interrupt-acknowledge-request       ;set by master
     0    batch-processor,IPL-requested       ;set by master


0041H     SMSTA     SLAVE-MASTER STATUS

Bit  7    slave-terminal-on                   ;set by slave
     6    slave-terminal-off                  ;set by slave
     5    < Rel.2.1:slave-receive-request     ;set by slave
     4    < Rel.2.1:slave-send-request        ;set by slave
     3    slave-IPL-request                   ;set by slave
     2    IPL-ready                           ;set by slave
     1    slave-interrupt-acknowledge         ;answer to MSCMD /1
     0    ---------------


0042H     SLPRES    SLAVE PRESENT BYTE

Bit  0    Slave present                       ;set by slave

     3    DC-data-transmitted                 ;set by DC-node


0043H     SMSGLN    SLAVE MESSAGE LENGTH

0044/45H  SMSGAD    SLAVE MESSAGE BUFFER ADDRESS

0046H     SMSDID    SLAVE MESSAGE DESTINATION ADDRESS

0047/48H  TABADR    ADDRESS OF CIRCUIT TABLE

005AH     MSGINT    MESSAGE INTERFACE (FROM REL.2.1)

Bit  3    Slave-receive-request               ;set by slave
     2    Slave-send-request                  ;set by slave
     1    Receive-ready                       ;set by master
     0    Send-ready                          ;set by master
```

2.4 SYSTEM PROCEDURES

2.4.1 Power On Procedure

2.4.1.1 Procedure Steps

The Power-on procedure involves the next steps:

1. Inside Test
2. Load OSLOAD.COM
3. OSLOAD.COM loads OSMASTER.SYS (including INTBOT.COM)
4. Slave is loaded with INTBOT.COM
5. Slave is downloaded with OSSLAVE*.SYS

Power on of the System is done after the first workstation is switched on (hardware switch-on of PSU).

After power-on all processors are mapped to ROM-page FFH (Test) and start their Inside Test.
The Inside Test is not executed if memory was maintained (Input port 20H, bit-2=0) AND save handling at PBD was completed (PBDFLG=0ABH).

At the end of Inside Test the next interface conditions are fulfilled before the IPL Program is started at address 1000H in Mode 1:

- Output port 20H = 95H (test led off, terminal off interrupt disabled, MMU enabled, Power-failure interrupt disabled)
- Interrupt register = 0
- Interrupt Mode = 2
- Interrupts disabled
- RAM address 0042H = 00H in case of defective PMU
- RAM address 004CH = copy of output port 88H (Test leds)

Within the Master the IPL-program is started directly, within the slaves after a delay of 4 seconds to get terminal-on line (108.2) stable. If memory was not maintainted the next Boot Program is executed:

The IPL-program of the Master searches for a file OSLOAD.COM in the directory of the Disks (first Flexible, then Fixed and then Fixed Disk Extension).
OSLOAD.COM is loaded into RAM starting at address 2000H, after which a short program (at 6000H) switches the mapping to Mode 2, moves OSLOAD.COM to 100H, and gives control to OSLOAD.

If memory was maintained and save handling at PBD had been completed, all processors restart at the position before power-off, and a possible Disk I/O is repeated.

In normal circumstances OSLOAD.COM then loads OSMASTER.SYS in the master, and via INTBOT the Slave Operating System OSSLAVE*.SYS is loaded in the connected Slaves.

For a Single User System , the master is directly started after the master system i.e. OSSINGLE.SYS is loaded.
In this case the system is switched off when the workstation is off for more than 4 seconds.
If during this delay the workstation is switched on again the program will be resumed.

2.4.1.2 IPL Flag

After IPL is completed the next information is located at address 000DH in RAM (IPLFLG):

```
BIT  1    ;TERMINAL ON FLAG,  used by Master to indicate a terminal
           switch-on during power-off handling.

BIT  2    ;NETWORK ACTIVE FLAG, used by Master to indicate an active
           Batch Processor during power-off handling.

BIT  3    ;OUTPUT ACTIVE FLAG, set by SP-driver,checked at power-off.

BIT  4    ;RESERVED

BIT  5    ;PMU-186 FLAG, local PMU is PMU-186

BIT  6    ;FIFO FLAG, Master is PMU 80-3 and FIFO- interrupt handling
           is possible.

BIT  7    ;PMU 80-3 FLAG, local PMU is PMU 80-3.
```

2.4.2 Normal processing

This section describes the functional operation of the TurboDOS Master/Slave Network drivers to explain the communication between master and slave processors.

The EMM-bus offers no interrupt feature from slave to master.
For this reason, the master processor has to poll the slave at regular moments. A number of bytes in RAM are used to communicate between the processors.

A slave indicates a send or receive request in the SMSTA-byte. After the master has transferred the message it sets the corresponding ready flag in the MSCMD-byte and interrupts the slave. The slave then checks the ready flags and proceeds with the corresponding processing.

When after IPL an active slave has made no request for more than 2 seconds it is interrupted by the master processor and asked for an acknowledgement. If the slave does not react on this within 4 seconds it is assumed to have crashed ,and will be reset by the master.

After being loaded/restarted the master sets for each Batch processor a flag in the corresponding memory (MSCMD, bit 0=1).
It then polls all present slaves and checks the flags of the SMSTA-byte and MSGINT-byte whether a slave requires any action.

When a workstation is switched-on (Input port 20H, bit-5 or-3=1) the slave informs the master of this event (SMSTA, bit-7=1). Additonally the IPL-requested flag (SMSTA,bit 3=1) is set.
These flags are also set for a Batch processor (MSCMD, bit-0=1).

2.4.3 Power-Off Procedure

When a Slave gets a terminal-off interrupt, a 4 seconds delay is activated.
If after this delay the terminal is on again, the program in the slave is resumed.
Otherwise the slave informs the master and waits for a new terminal-on.
Detecting the terminal-off flag, the master cancels the slave from its list of active slaves. When all the slaves are inactive the master finishes all remaining print-jobs and all other activities in the master and within the Batch processors.
The Extension Cabinets are switched off and the System cabinet is switched off.

2.4.4 Power Break Down / Restart Procedure

If the Battery Back Up option is installed in the system, and set active via the Battery-On Switch , the memory of the system is maintained.
At PBD Interrupt the system saves all CPU registers and sets the PBD-Completed byte (FFFE) to 0ABH.
At Power Restart the CPU Registers are restored and program restarts from the point where it was interrupted.
A pending Fixed Disc Access at the moment of PBD is restarted.

2.4.5 Test and Diagnostic Interface

The status of the inside test is stored at RAM address 004C-005AH. From Rel.3 onwards this area is copied by the driver initialization routines to high memory. The start-address of this area (T&D) is found at location 004D-004EH (T&D AREA).

T&D0 LAMP FIELD
T&D1-T&D3 DEFECTIVE UNIT
T&D4 UNIT/SUBUNIT
T&D5 LENGTH OF STATUS AREA (02-08)
T&D6-T&DE STATUS AREA

004CH/ T&D0

7	6	5	4	3	2	1	0	
1	1	1	1	1	1	1	1	-- No Error
1	1	1	1	0	0	0	0	-- PMU Defect
1	1	1	1	0	1	0	0	-- Sesco Defect
1	1	1	1	0	0	1	0	-- Int. Fixco Defect
1	1	1	1	0	1	1	0	-- Int. Fixed Drive Defect
1	1	1	1	0	0	0	1	-- Int. Flexible Defect
1	1	1	1	0	1	0	1	-- No Int. Flexible Ready
1	1	1	1	0	0	1	1	-- Ext. 8" Flexible Defect

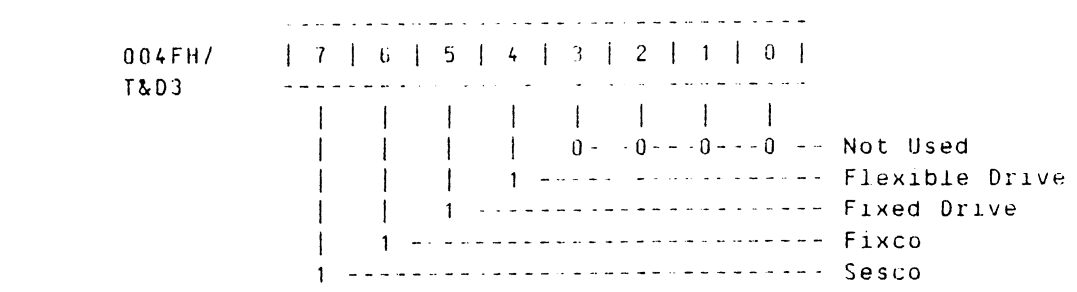
This is a copy of the info send to Output port 88H (LED).
Also the Drivers may use location 004CH.

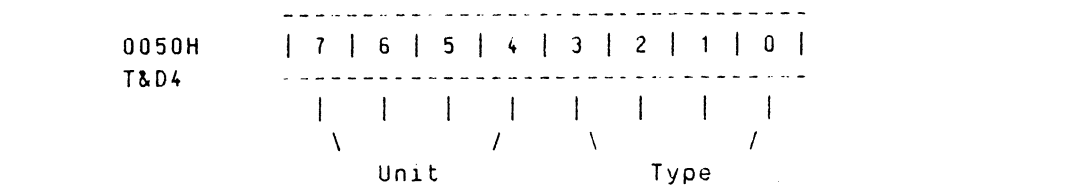
004DH/ T&D1

7	6	5	4	3	2	1	0	
							1	-- Slave 7
						1		------ Slave 6
					1			---------- Slave 5
				1				---------- Slave 4
			1					---------- Slave 3
		1						---------- Slave 2
	1							---------- Slave 1
1								---------- Master

004EH/ T&D2

7	6	5	4	3	2	1	0	
				0	0	0	0	--- Not Used
			1					---------- Slave 11
		1						---------- Slave 10
	1							---------- Slave 9
1								---------- Slave 8





UNIT:
The value of this tetrad depends on the contents of address 004CH.

Value	Unit
0	Master
1-8	Slave 1-11
C	Sesco
D	Fixco
E	Fixed Drive
F	Flexible Drive

TYPE:
The meaning of the value of this tetrad depends on Address 004CH.

Value	Type(PMU)	Type(Sesco)	Type(Fixco)
0	No Error	No Error	-----
1	Instr.test	Output Time out	Output Time out
2	MMU	Input Time Out	Input Time Out
3	RAM Address	Not allowed R/W	Controller Diagn
4	RAM Cell	Int. not recogn.	------
5	ROM Test	No Int. at RDY change	------
6	Timer Test	Abnorm. Termin Seek/Recal	------
7	SIO Test	No Step Pulses from FDC	------
8	M/S Comm.	No Read Started by FDC	------
9	Interr. test	FDC Error after 2 retries	------

Value	Type(Fixed Drive)	Type(Flexible Drive)
1	Not Ready after 60 Sec.	No Seek/Recalibrate
2	Drive Diagnostic error	No data from drive

Some meanings of the status area from address 0052H/ T&D6:

```
ROM Test:  0052 MSB of expected hash total
           0053 LSB of expected hash total
           0054 MSB of actual hash total
           0055 LSB of actual hash total

RAM Adr:   0054 Defective Address Line +1

RAM Cell:  0052 MSB of Defective address
           0053 LSB of defective address
           0054 Expected value
           0055 Actual value

Timer:     0052 Bit 0-3: Channel 0-3

SIO:       0052 Bit 1= Status error after init, ch.B
                Bit 2= Error in Interrupt handling
                Bit 3= Transmit Error
                Bit 4= Status error after transmit

M/S Comm:  0052 1= Slave gets no IPL request
                2= No interrupt in Slave

Interr.:   0052 LSB of interrupt vector
           0053 MSB of interrupt address
           0054 LSB of interrupt address
```

2.4.6 Interface to Power Supply

The interface to the PSU and BBU provide for the following functions:

- Master reset of all logic.
- Power Failure indication to support Power Break Down/Restart.
- Remote Power On.
- Controlled Power Off.
- Surveillance of BBU status during power off.

The following signals are used to realize these functions:

- RSLN (ReSet Line Not)

Resets all logic at Power Off and Power On switching.

- PWFN (PoWer Failure Not)

Indicates that the mains voltage has become below its minimum value and causes an interrupt to a power failure save routine.

- RPON (Remote Power ON)

Used to switch on the system remotely.
This signal is activated via either of the signals 109 or 125 of serial interface A or via signal 108.2 of serial interface B, strap selectable with jumpers on the processor boards.
The signal is deactivated via an output to Port 20-Bit 1, causing controlled power off of the system.

- BARE (BAttery was off/REstart enable)

Reflects the status of the Battery Backup Unit during system off state. The signal is available at input port 20, and can be used to decide if an automatic restart routine can be initiated.

2.5 INPUT / OUTPUT SYTEM PMU 80-3

This section gives the programming information for the PMU 80-3 on HSI-level.
As much as possible the default settings for the TurboDOS System are given.

The main differences between PMU 80-1 and PMU 80-3 are found in the Master / Slave communication and the serial interfaces.

The other functions are mainly the same , only other hardware is used in the realization at the PCB.

Programmable I/O circuits

Used circuits:
---

* Z8536-CIO Counter/Timer and Parallel I/O Port including:

- Port B assigned to Control Port 1, Input Port 20
- Port C assigned to Control Port 3, Port 21(Reserved)
- Control Registers , accessed via Port 22
- Port A assigned to Interrupt Lines (NIR0 - NIR7),Input Port 23

Port A, B, C are directly accessable.
All internal registers are accessed via a two-step sequence to port 22.
First the address of the internal register is written to Port 22, then the target register can be accessed via Port 22.

* Z8530 SCC Serial Communications Controller including:

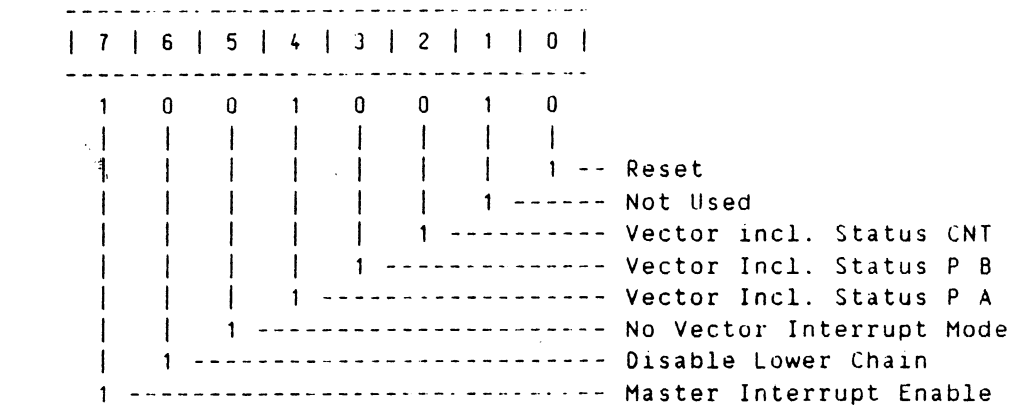
- Channel A Data Register
- Channel A Control/Status Register
- Channel B Data Register
- Channel B Control/Status Register

2.5.1 INITIALIZATION OF Z8536-CIO

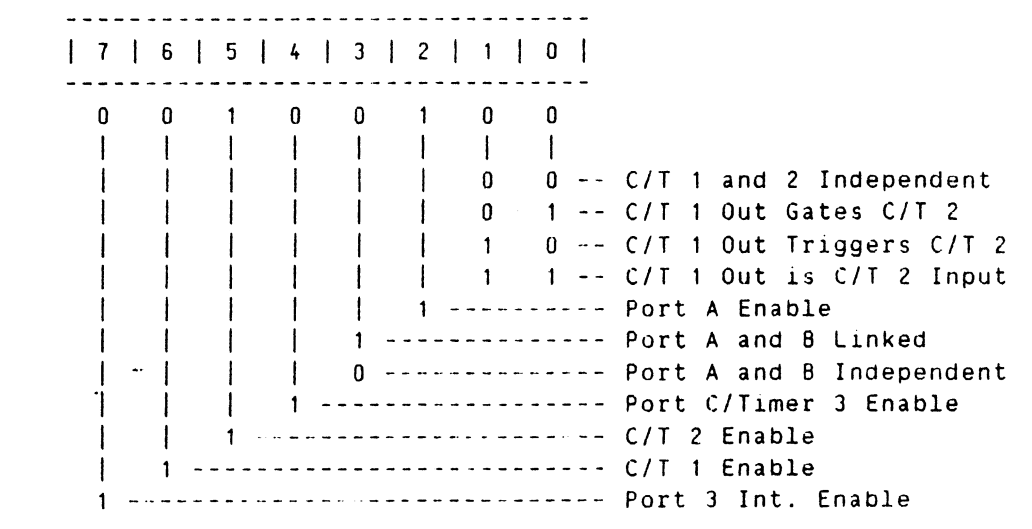
2.5.1.1 Master Control Registers

These registers specify the general operation of the CIO.
The Master Interrupt Control Register specifies which ports can raise an interrupt and the conditin to do this.
The Master Configuration Control Register specifies which CIO Ports are enabled and how they are linked to each other.

ADDRESS	NAME	DEFAULT
22H-00H	Master Interrupt Control	92H



ADDRESS	NAME	DEFAULT
22H-01H	Master Configuration Control	24H



2.5.1.2 Port Specification Registers

These registers specify in more detail the mode of operation of ports A and B.
The Mode Specification Register defines the port as input, output or bit-dependent in/out port. Also the conditions to generate an interrupt are specified in detail in this register.
The Port Handshake Specification Register is used to define the way in which data to and from ports A and B are transferred using Port C as handshaking signals (not used on PMU 80).
The Port Command and Status Register is to be used to obtain status information from a port such as : Interrupt Pending etc.
The Interrupt status can also be reset via this register.

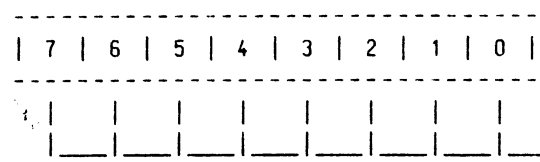
ADDRESS	NAME	DEFAULT
22H-20H	Port A Mode Specification	06H
22H-28H	Port B Mode Specification	00H

7	6	5	4	3	2	1	0	
0	0	0	0	0	1	1	0	Default A
0	0	0	0	0	0	0	0	Default B
							1	-- Latch on Pattern(Bit)
								Deskew Timer(Handshake)
					0	0	------	Disable Pattern Match
					0	1	------	OR Mode
					1	0	------	AND Mode
					1	1	------	OR-Priority Vector Mode
				1	----------			Interrupt on Match Only
			1	----------				Single Buffered Mode
		1	----------					Interrupt on two Bytes
0	0	----------						Bit Port
0	1	----------						Input Port
1	0	----------						Output Port
1	1	----------						Bidirectional port

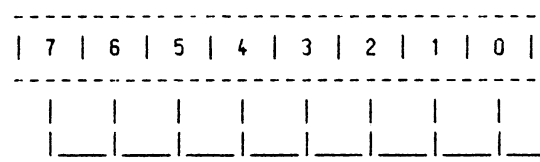
2.5.1.3 Bit Path Definition Registers

These Registers define the data path of the CIO Ports.
The Data Polarity Registers define if the port is used as inverting or Non-inverting Port.
The Data Direction Register defines every bit of a Bit Port as either Input or Output bit.
The Special I/O Control Register can be used to specify an Input bit as normal or 1's catcher and an Output bit can be specified as open-drain output.

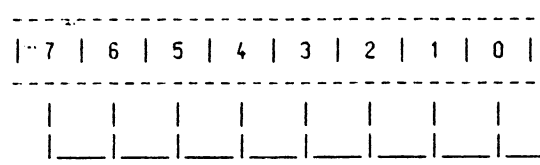
ADDRESS	NAME	DEFAULT
22H-22H	Data Polarity Port A (INT)	FFH
22H-2AH	Data Polarity Port B (CP1)	FFH



ADDRESS	NAME	DEFAULT
22H-23H	Data Direction Port A (INT)	FFH
22H-28H	Data Direction Port B (CP1)	FFH



ADDRESS	NAME	DEFAULT
22H-24H	Special I/O Control Port A (INT)	00H
22H-2CH	Special I/O Control Port B (CP1)	00H



2.5.1.4 Pattern Definition Registers

These Registers are used to specify independent for each bit of Port A and B the condition on which an interrupt is generated (high, low, transition, masked).

ADDRESS	NAME	DEFAULT
22H-25H	Pattern Polarity Port A (INT)	10H
22H-2DH	Pattern Polarity Port B (CP1)	00H

7	6	5	4	3	2	1	0

ADDRESS	NAME	DEFAULT
22H-26H	Pattern Transition Port A (INT)	00H
22H-2EH	Pattern Transition Port B (CP1)	10H

7	6	5	4	3	2	1	0

ADDRESS	NAME	DEFAULT
22H-27H	Pattern Mask Port A (INT)	I *
22H-2FH	Pattern Mask Port B (CP1)	00H

7	6	5	4	3	2	1	0

0	0	X	Bit Masked Off
0	1	X	Any Transition
1	0	0	Zero
1	0	1	One
1	1	0	One to Zero
1	1	1	Zero to One

* I = Dependent on Interrupt Mask

2.5.1.5 Counter/Timer Registers

The CIO contains three internal timers which can be programmed via the following registers.

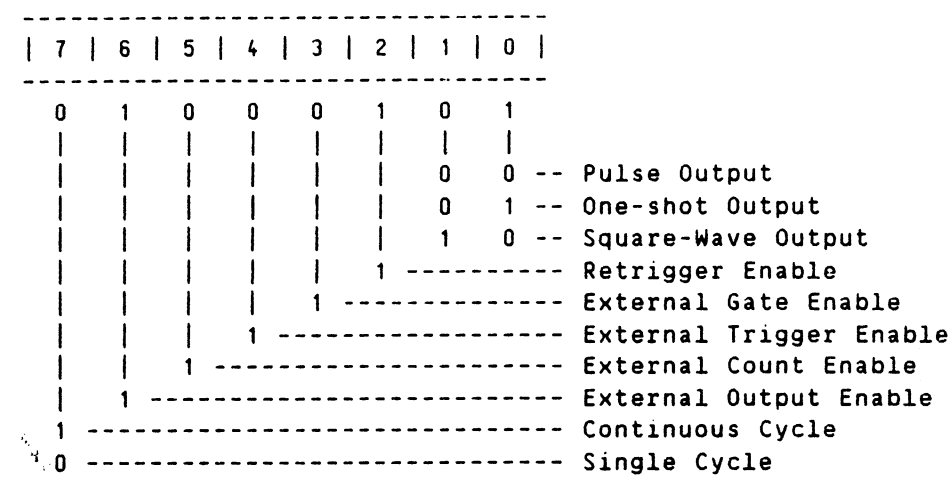
The Counter/Timer Command and Status Registers can be read to obtain status of the timer. A write into this register can be used to start and reset the timer.
The Mode Specification Registers define the mode of operation, interrupt enable etc.
The Counter/Timer value can be read via the Current Count Registers and programmed via the Time Constant Registers.

ADDRESS	NAME	DEFAULT
22H-0AH	Command/Status C/T 1	45H
22H-0BH	Command/Status C/T 2	45H
22H-0CH	Command/Status C/T 3	00H

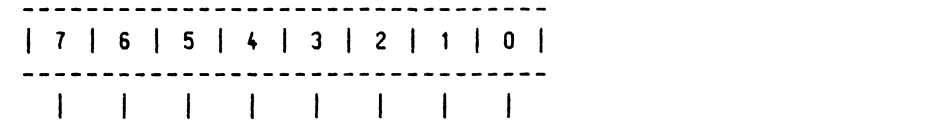
7	6	5	4	3	2	1	0	
0	1	0	0	0	1	0	1	
							1	Count In Progress (R)
						1		Trigger Command Bit (W)
					1			Gate Command Bit
				1				Read Counter Control (W)
			1					Interrupt Error (R)
		1						Interrupt Pending (R)
	1							Interrupt Enable (R)
1								Interrupt Under Service (R)

WRITE COMMANDS			
0	0	0	Null Code
0	0	1	Clear IP and IUS
0	1	0	Set IUS
0	1	1	Clear IUS
1	0	0	Set IP
1	0	1	Clear IP
1	1	0	Set IE
1	1	1	Clear IE

ADDRESS	NAME	DEFAULT
22H-1CH	Mode Specification C/T 1	00H
22H-1DH	Mode Specification C/T 2	45H
22H-1EH	Mode Specification C/T 3	00H



ADDRESS	NAME		
22H-10H	Current Count	C/T 1	MSB
11H		C/T 1	LSB
12H		C/T 2	MSB
13H		C/T 2	LSB
14H		C/T 3	MSB
15H		C/T 3	LSB
16H	Time Constant	C/T 1	MSB
17H		C/T 1	LSB
18H		C/T 2	MSB
19H		C/T 2	LSB
1AH		C/T 3	MSB
1BH		C/T 3	LSB



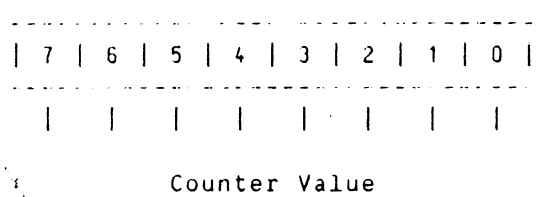
Binary value of 16 Bit Counter

2.5.2 Real Time Clock

The Real Time Clock generation is done by Counter/Timer 2 of Z8536-CIO.
It consists of a presettable 16 bit down counter.
The Z8536-CIO should be initialized according to section 2.5.1 before the timer can be programmed.

Time Constant Word:

ADDRESS	NAME			DEFAULT
22H-18H	Time Constant	C/T 2	MSB	C8H
22H-19H		C/T 2	LSB	64H



Note: Frequency= 3.072 MHz / counter value

60 Hz = 3.072 / 51200 (0C864H)

2.5.3 Serial Interfaces

The PMU 80-3 provides two serial interfaces:

Channel A, a full V24-interface
Channel B, a short distance interface

Channel A is a DTE Interface, used to connect the P3000 System to a communication link via standard Modems. Connection of peripherals to this interface should be done using the cross-wiring of Cable Type 6.

Channel B can be strapped as either a DCE Interface (as in PMU 80) or as a DTE Interface to provide the same interface type on both channels of the PMU 80, to minimize the number of cable types.

These interfaces are controlled via a dual-channel Z8530-SCC (Serial Communications Controller) and two control ports:
Input port 20H and Output port 20H.

The next procedure must be used to perform a serial data transmission:

- Program the Z8500-SCC mode of operation
- Program Output Port 20H to set the required V24 signals
- Check Input Port 20H for correct return signals
- Program the Z8500-SCC command (write and/or read)
- Wait for interrupts from Z8500-SCC

The interrupt routine should check the SCC status and react on this with either send or receive data actions.

A SCC Write or Read Register cannot be accessed directly.
Before any write or read action to the SCC Internal registers, the particular register has to be selected.

This is done by sending the address of the register to be selected to the Command Register.

The next ports are assigned to the Z8500-SCC:

PORT 00 H	DATA REGISTER	CHANNEL A
PORT 01 H	DATA REGISTER	CHANNEL B
PORT 02 H	COMMAND REGISTER	CHANNEL A
PORT 03 H	COMMAND REGISTER	CHANNEL B

2.5.3.1 Internal Registers SCC

The Z8530-SCC contains a number of Write and Read registers. A particular register is accessed in two steps:

First the register number to be accessed is written into the SCC Command Register (WR0)- , then the information to or from the register can be read or written.

WRITE REGISTER 0 - COMMAND REGISTER

```
          ---------------------------------
Port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
02H(ch.A) ---------------------------------
03H(ch.B)   |   |   |   |   |   |   |   |
            0   0   0   1   1   0   0   0     Default 18H
            |   |   |   |   |   |   |   |
            |   |   |   |   |   Next Byte Pointer
            |   |   |   |   |   0   0   0  - register 0/8
            |   |   |   |   |   0   0   1  - register 1/9
            |   |   |   |   |   0   1   0  - register 2/10
            |   |   |   |   |   0   1   1  - register 3/11
            |   |   |   |   |   1   0   0  - register 4/12
            |   |   |   |   |   1   0   1  - register 5/13
            |   |   |   |   |   1   1   0  - register 6/14
            |   |   |   |   |   1   1   1  - register 7/15
            |   |   command code
            |   |   0   0   0  - null code
            |   |   0   0   1  - high pointer (register 8-15 select)
            |   |   0   1   0  - reset ext.status interrupts
            |   |   0   1   1  - send abort (SDLC)
            |   |   1   0   0  - enable int. on next Rx char.
            |   |   1   0   1  - reset Tx int. pending
            |   |   1   1   0  - error reset
            |   |   1   1   1  - reset highest IUS
          reset code
          0   0  - null code
          0   1  - reset Rx CRC checker
          1   0  - reset Tx CRC generator
          1   1  - reset Tx underrun/ EOM latch
```

WRITE REGISTER 1 - INTERRUPT CONTROL

```
          ---------------------------------
port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
02H(ch.A) ---------------------------------
03H(ch.B)   |   |   |   |   |   |   |   |
            0   0   0   1   0   0   0   0    Default 10H
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 -- ext.interrupt enable
            |   |   |   |   |   |   1 ------ Tx interrupt enable
            |   |   |   |   |   1 ---------- parity is spec. cond.
            |   |   |   0   0 -- Rx int disable
            |   |   |   0   1 -- Rx int on first character or spec. cond.
            |   |   |   1   0 -- int on all Rx characters or spec. cond.
            |   |   |   1   1 -- Rx int on special condition only
            |   |   |
            |   |   1 - wait/ready on Rx/Tx-n
            |   1 ----- wait-n/ready function
            1 --------- wait/ready enable
```

WRITE REGISTER 2 - INTERRUPT VECTOR (COMMON FOR BOTH CHANNELS)

```
          ---------------------------------
Port 03H  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
          ---------------------------------
            |   |   |   |   |   |   |   |
            0   0   1   0   1   1   0   0     Default 2CH
```

Binary Value = Interrupt Vector

WRITE REGISTER 3 - RECEIVER CONTROL

```
          ---------------------------------
Port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
02H(ch.A) ---------------------------------
03H(ch.B)   |   |   |   |   |   |   |   |
            1   1   0   0   0   0   0   1    Default 0C1H
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 -- Receive Enable
            |   |   |   |   |   |   1 ------ Sync Char. Load Inhibit
            |   |   |   |   |   1 ---------- Address Search Mode(SDLC)
            |   |   |   |   1 -------------- Rx CRC Enable
            |   |   |   1 ------------------ Enter Hunt Phase
            |   |   1 ---------------------- Auto Enables
            0   0 -- Rx 5-bits/character
            0   1 -- Rx 7-bits/character
            1   0 -- Rx 6-bits/character
            1   1 -- Rx 8-bits/character
```

WRITE REGISTER 4 - RECEIVE/TRANSMIT CONTROL

```
          ---------------------------------
Port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
02H(ch.A) ---------------------------------
03H(ch.B)   |   |   |   |   |   |   |   |
            0   1   0   0   0   1   0   0    Default 44H
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 -- Parity Enable
            |   |   |   |   |   |   1 - --- Parity Even/Odd-N
            |   |   |   |   |   0   0 - Synchronous Mode
            |   |   |   |   |   0   1 - 1 stopbit/char
            |   |   |   |   |   1   0 - 1.5 stopbit/char
            |   |   |   |   |   1   1 - 2 stopbits/char
            |   |   |   0   0 - 8  bit sync character
            |   |   |   0   1 - 16 bit sync character
            |   |   |   1   0 - SDLC Mode
            |   |   |   1   1 - External Sync
            |   |   0   0 - x  1 Clock
            |   |   0   1 - x 16 Clock
            |   |   1   0 - x 32 Clock
            |   |   1   1 - x 64 Clock
```

WRITE REGISTER 5 - TRANSMITTER CONTROL

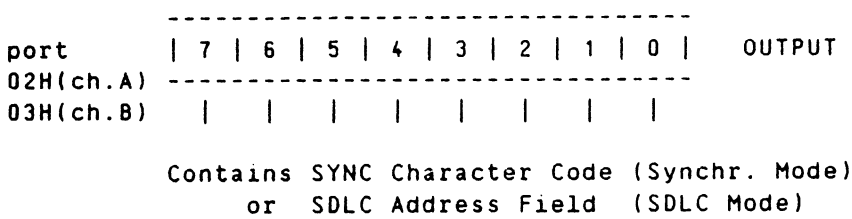
```
          ---------------------------------
port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
02H(ch.A) ---------------------------------
03H(ch.B)   |   |   |   |   |   |   |   |
            1   1   1   0   1   0   1   0    Default 0EAH
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 -- Tx CRC Enable
            |   |   |   |   |   |   1 ------ RTS
            |   |   |   |   |   1 ---------- SDLC-n/CRC16 Polynom.
            |   |   |   |   1 -------------- Tx Enable
            |   |   |   1 ------------------ Send Break
            |   0   0 - Tx 5 bits/character
            |   0   1 - Tx 7 bits/character
            |   1   0 - Tx 6 bits/character
            |   1   1 - Tx 8 bits/character
            |
            1 - DTR
```

WRITE REGISTER 6 - TRANSMIT SYNC CHARACTER

```
          ---------------------------------
port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
02H(ch.A) ---------------------------------
03H(ch.B)   |   |   |   |   |   |   |   |
```

Contains SYNC Character Code (Synchr. Mode)
or SDLC Address Field (SDLC Mode)

WRITE REGISTER 7 - RECEIVE SYNC CHARACTER

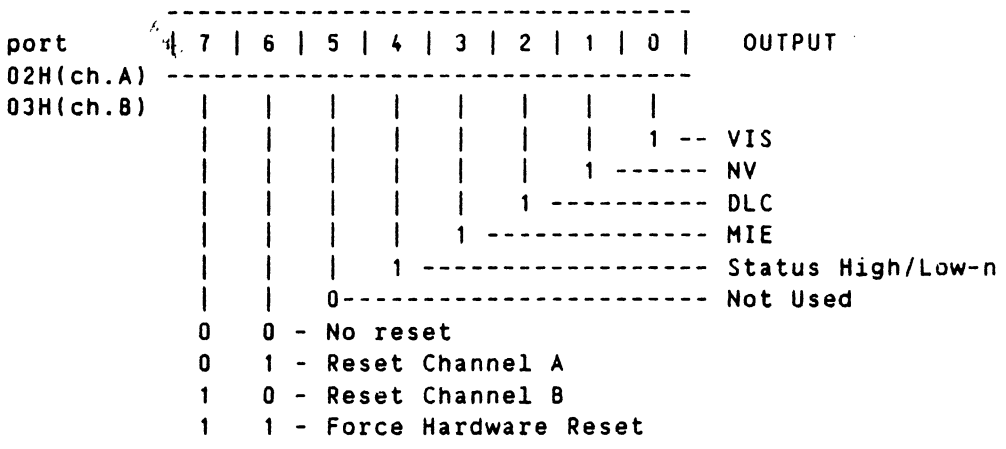


Contains SYNC Character Code (Synchr. Mode)
or SDLC Address Field (SDLC Mode)

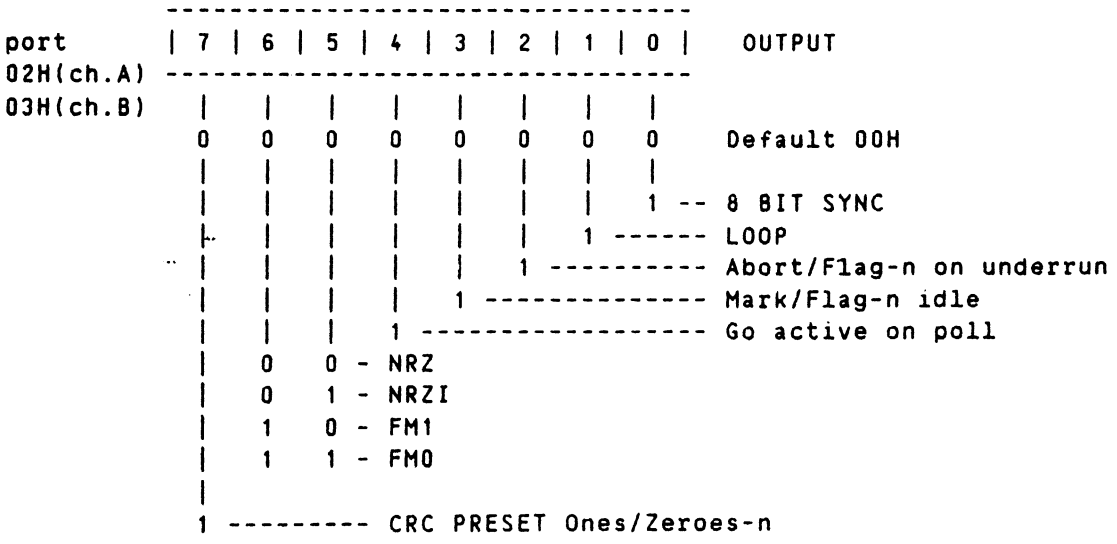
WRITE REGISTER 8 - TRANSMIT BUFFER

This buffer contains the character to be tansmitted, it is normally loaded via a write to port 00 or 01 (Data Buffer).

WRITE REGISTER 9 - MASTER INTERRUPT CONTROL / RESET
(COMMON FOR CHANNEL A/B)



WRITE REGISTER 10 - MISCELLANEOUS CONTROL BITS



WRITE REGISTER 12 - LSB BAUD RATE GENERATOR CONSTANT

WRITE REGISTER 13 - MSB BAUD RATE GENERATOR CONSTANT

For P3000 the next formular must be used to calculate the time constant value for a required baud rate in asynchronous mode:

Binary value = (3072000 / (32 * Baudrate))-2

WRITE REGISTER 14 - MISCELLANEOUS CONTROL BITS

port	7	6	5	4	3	2	1	0	OUTPUT
02H(ch.A) 03H(ch.B)									
	1	0	0	0	0	0	0	0	Default 80H
								1	-- BR Generator Enable
							1		------ BR Generator Source
						1			---------- DTR-n/Request Function
					1				-------------- Auto Echo
				1					---------------- Local Loop
	0	0	0	- Null Command					
	0	0	1	- Enter Search Mode					
	0	1	0	- Reset Missing Clock					
	0	1	1	- Disable PLL					
	1	0	0	- Set source = BR Generator					
	1	0	1	- Set source = RTxC					
	1	1	0	- Set FM Mode					
	1	1	1	- Set NRZI Mode					

WRITE REGISTER 15 - EXTERNAL / STATUS INTERRUPT CONTROL

port	7	6	5	4	3	2	1	0	OUTPUT
02H(ch.A) 03H(ch.B)									
	0	0	0	0	0	0	0	0	Default 00H
								0	-- Not Used
							1		------ Zero Count IE
						0			---------- Not Used
					1				---------- DCD IE
				1					---------------- SYNC/HUNT IE
			1						-------------- CTS IE
		1							------------------------ Tx Underrun IE
	1								------------------------ Break/Abort IE

READ REGISTER 0 - STATUS

```
          ---------------------------------
port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   INPUT
02H(ch.A) ---------------------------------
03H(ch.B)   |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 -- Rx Char. Available
            |   |   |   |   |   |   1 ------ Zero Count
            |   |   |   |   |   1 ---------- Tx Buffer Empty
            |   |   |   |   1 -------------- DCD
            |   |   |   1 ------------------ Sync/Hunt(Not Used)
            |   |   1 ---------------------- CTS
            |   1 ------------------------- Tx Underrun/EOM
            1 --------------------------- Break/Abort
```

READ REGISTER 1 - RECEIVE STATUS

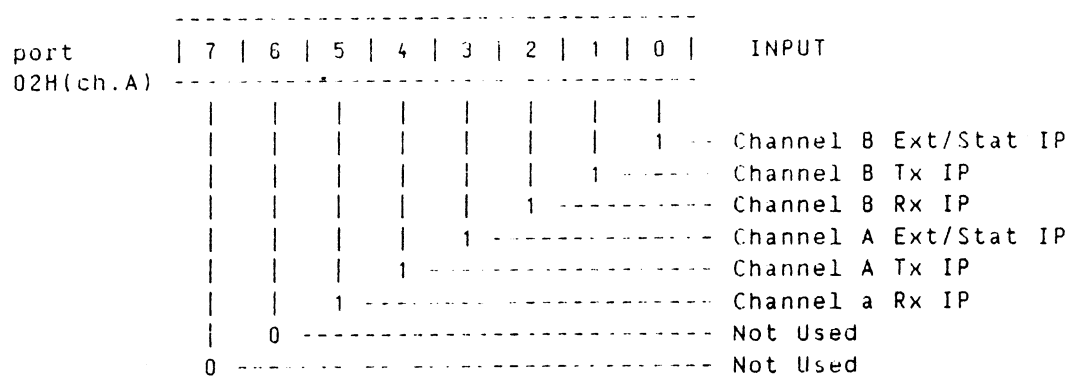
```
          ---------------------------------
port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   INPUT
02H(ch.A) ---------------------------------
03H(ch.B)   |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 -- All Sent (Tx Empty)
            |   |   |   |   SDLC-Residue
            |   |   |   |   1   0   0       3 bits left in last I-word
            |   |   |   |   0   1   0       4
            |   |   |   |   1   1   0       5
            |   |   |   |   0   0   1       6
            |   |   |   |   1   0   1       7
            |   |   |   |   0   1   1       8
            |   |   |   |   1   1   1       9
            |   |   |   |   0   0   0      10 bits left in last I-word
            |   |   |   |
            |   |   |   1-- Parity Error
            |   |   1------ Rx Overrun Error
            |   1---------- CRC/Framing Error
            1-------------- End Of Frame(SDLC)
```

READ REGISTER 2 - INTERRUPT VECTOR (COMMON FOR CHANNEL A/B)

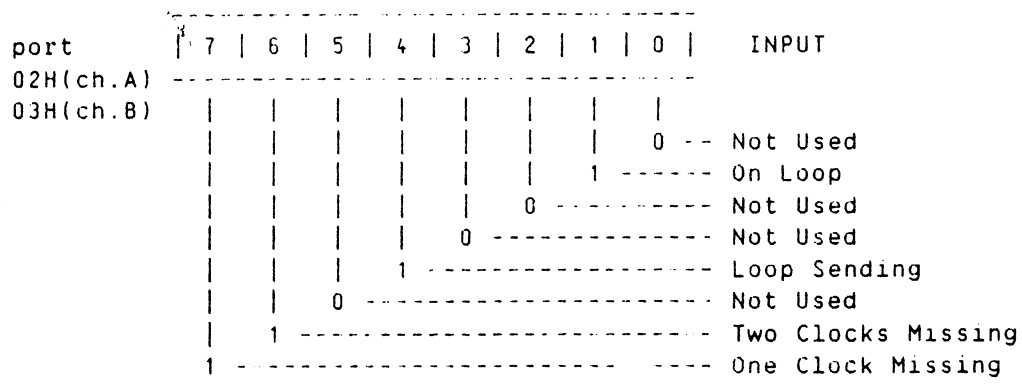
```
          ---------------------------------
Port 03H  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   INPUT
          ---------------------------------
            |   |   |   |   |   |   |   |
```

Contains Modified Interrupt Vector in Channel B

READ REGISTER 3 INTERRUPT PENDING BITS (Channel A only)



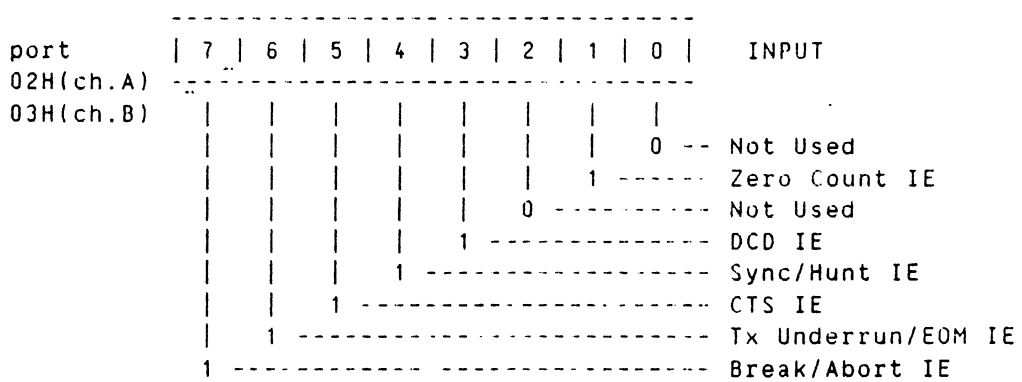
READ REGISTER 10 - MISCELLANEOUS STATUS



READ REGISTER 12 - LSB BAUD RATE CONSTANT
READ REGISTER 13 - MSB BAUD RATE CONSTANT

These registers contain the programmed value of the internal Baud Rate Generator time constant.

READ REGISTER 15 - EXTERNAL/STATUS INTERRUPT INFO



2.5.3.2 Programming the Baudrate

When used in asynchronous applications, so also for communication to workstations and printers, the System timing signal of 3.072 MHz is input to the SCC and supplied to an internal Baud Rate Generator.

Channel B of the SCC can only be used in asynchronous mode, Channel A can be strapped for Internal or External timing.

When strapped for External Timing, synchronous mode, the modem timing signals are used as Transmit and Receive Clock.

Thus the Z8500-SCC operates in P3000 systems in one of the next timing modes :

- SCC Supplies Receive/Transmit Clocks from internal Baud Rate Generator (Normal Mode)

- SCC receives Receive/Transmit Clock from external source (Synchronous Modem Connections on Channel A)

PROGRAMMING SCC FOR INTERNAL TIMING:

The next values must be send to the Control Port Address of Channel A and/or B :

00	10	Reset Channel
01	10	Interrupts on all Rx Characters or special conditions.
02	24	Interrupt vector set to 24H (Channel B)
03	C0	8-bit Characters
04	44	16 x Clock, Asynchronous, 1 Stopbit, No Parity Bit
05	EA	Transmit 8-bit characters, set DTR and RTS
09	09	Vector Includes Status, Master Interrupt Enable
0A	00	NRZ Mode
0B	55	RxC and TxC from Internal BR Generator, CT113 is TxC
0C	08	Speed LSB (9600 BpS)
0D	00	Speed MSB (9600 BpS)
0E	80	Set Source to BR Generator
0F	00	Disable Interrupts on DCD, CTS, Break etc.

PROGRAMMING SCC FOR EXTERNAL TIMING (CHANNEL A ONLY):

0B	08	RxC and TxC from Interface

2.5.3.3 Channel A Interface Control

The next interface signals are used at channel A, the list explains via which port the signals can be accessed.

PIN	CCITT	NAME	I/O PORT	BIT	DESCRIPTION
b1	101	GND	------		
b7	102	L	------		
b2	103	TMD	OUT 00H	0-7	DATA OUT
b3	104	RCD	IN 00H	0-7	DATA IN
b4	105	RTS	OUT WR5	1	REQUEST TO SEND
b5	106	CTS	IN RR0	5	CLEAR TO SEND
b6	107	DSR	IN 20H	7	DATA SET READY
a7	108.2	DTR	OUT WR5	7	DATA TERMINAL READY
b8	109	DCD	IN RR0	3	CARRIER DETECTED
a10	111	DRS	-------		HIGH
a11	113	TSET(M)	-------		INT.CLOCK TO MODEM)
a2	114	TSET	Strap		SYNCHR.TxCLOCK FROM MODEM
a4	115	RSET	Strap		SYNCHR.RxCLOCK FROM MODEM
a9	125	RIN	Strap		CALLING INDICATOR
a8	140	REML	OUT 20H	6	REMOTE LOOP SETTING
a5	141	LOCL	OUT 20H	5	LOCAL LOOP SETTING
a12	142	TIN	IN 20H	6	TEST INDICATOR
			IN 20H	3	RPON (CT109/CT125)

NOTE: CT109 and CT125 can be strapped to supply Remote Power ON (RPON).
CT109 or CT125 can be read at port 20H, bit 3.

2.5.3.4 Channel B Interface Control

SLAVE (P2711) MASTER (6P300L)

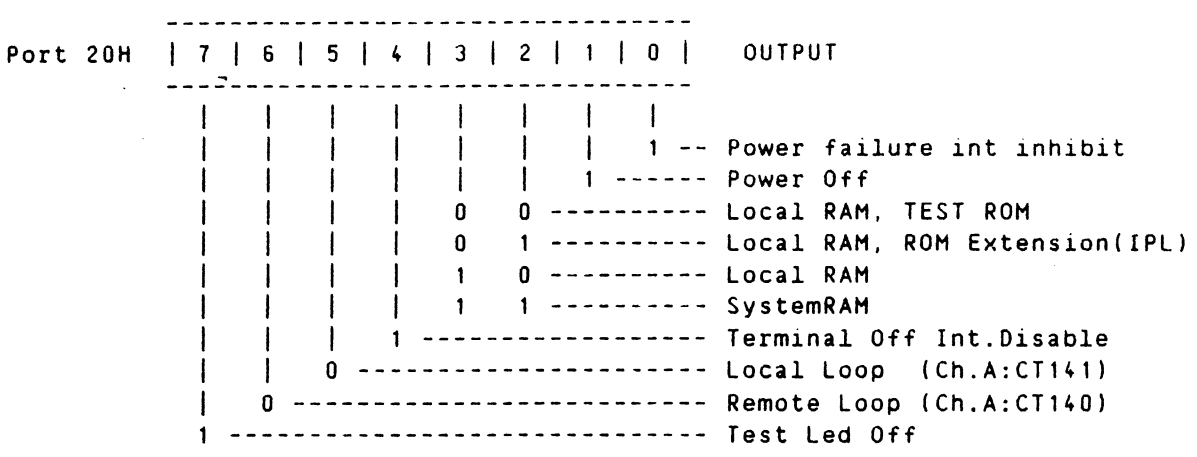
Channel B has limited control features . It is designed as Short Distance Interface, for direct connection of peripherals.
It can be strapped as DTE or DCE interface
The next interface signals are used at channel B, the list explains via which port the signals can be accessed.

STRAPPED AS :			DCE INTERFACE		DTE INTERFACE		
PIN	CCITT	NAME	I/O PORT	BIT	I/O PORT	BIT	
b1	101	GND	------		-------		
b7	102	L	------		-------		
b3	104	RCD	OUT 01H	0-7	IN 01H	0-7	
b2	103	TMD	IN 01H	0-7	OUT 01H	0-7	
b5	106	CTS	OUT WR5	7	IN RR0	5	
b6	107	DSR	IN RR0	5	IN 20H	5	
b7	108	DTR	IN 20H	5	OUT WR5	7	
b4	105	RTS	IN RR0	1	OUT WR5	1	*
b8	109	DCD	OUT WR5	1	IN RR0	1	*

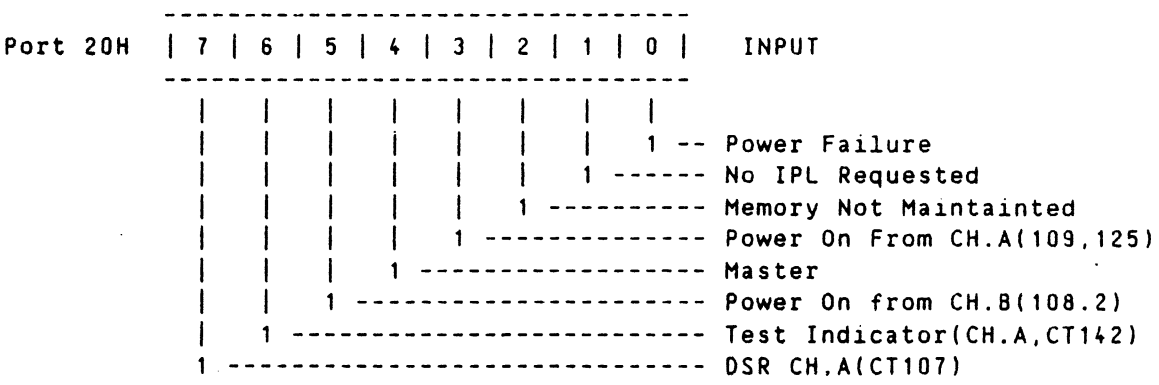
NOTE: CT108.2 can be strapped to give Remote Power ON (RPON).
RPON condition can be read at port 20H, bit 5.
* = Not used in protocol

2.5.4 Control Port Overview

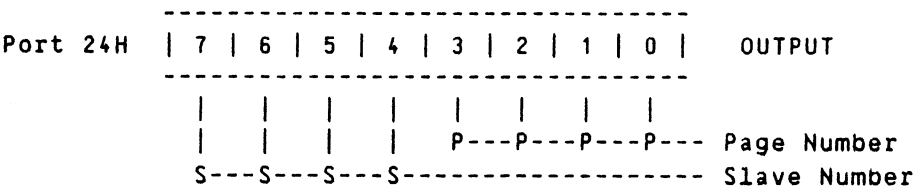
OUTPUT PORT 20H



INPUT PORT 20H



OUTPUT PORT 24H - MMU PORT



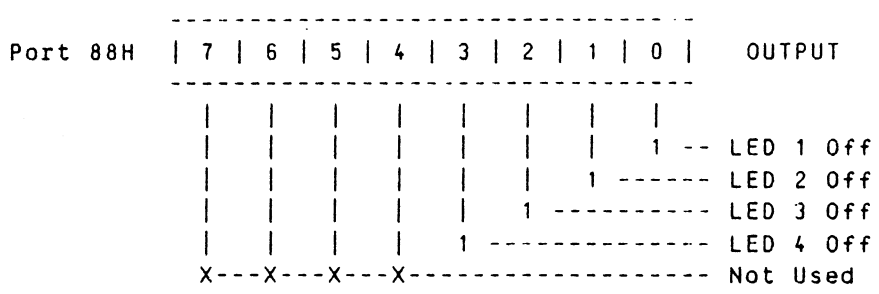
OUTPUT PORT 28H (CP3) - RESET M/S-COMMAND INTERRUPT

Any output to this port resets the Master/Slave Command interrupt. This interrupt can be set by the Master via the MSC- port (42H-5EH, bit 2).

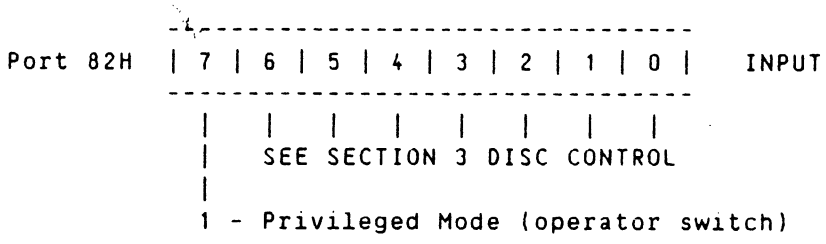
2.5.5 Operator Panel Control

Only the Master Processor has access to the operator panel.
The operator panel is connected to the SESCO board, accessable by the Master via the EMM-bus.

OPERATOR PANEL OUTPUT PORT (via SESCO)



OPERATOR PANEL INPUT (P3800 Only)



2.5.6 MASTER / SLAVE TRANSFERS

From Rel.3 onwards tne P3000 system can have three types of processors :

- A File Server (Master)
- DC-Node(s)
- Slave(s)

A DC-Node can be considered as a Slave for the File Server and as a Master for the Slaves.
Both the File Server and the DC-Node can access the bus.
A PMU80 or PMU80-1 can NOT act as DC-node.

PMU80-3 boards have additional facilities for bus transfer.
Between the EMM bus and the local bus is a FIFO buffer located which is used to communicate between the processors.
The FIFO processing is only used if all PMU boards are able to perform FIFO processing, so all PMU 80-3 or higher.

Thus, the communication between master and slave boards is executed via a polling mechanism of the Network Drivers (PMU 80-1) or via the FIFO mechanism (PMU 80-3).
Data transfers between master and slaves are allways done via the system memory mapping of the master.
A Master/Slave Control port is available on every board to allow interrupting of slave boards by the master processor.

2.5.6.1 Master/Slave Control Ports

The Master has access to the Slaves via an I/O- port located at every slave. This port is written to by the master, and cannot be accessed by the slave.
The port address depends on the slave number:

```
Port 42   Slave 1
     44   Slave 2
     46   Slave 3
     48   Slave 4
etc. till:
Port 5E   Slave 15
```

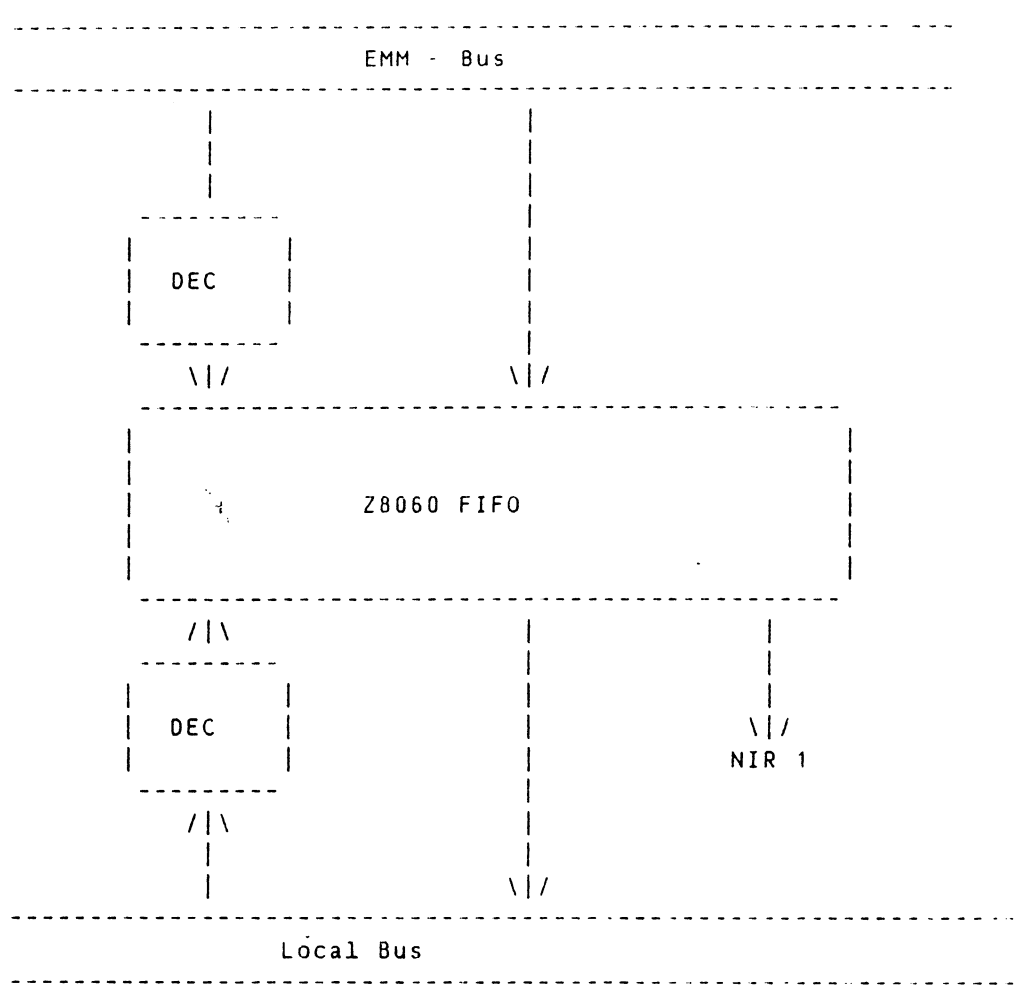
MASTER/SLAVE CONTROL PORT

```
          ---------------------------------
Port 42-  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
     5EH  ---------------------------------
            |   |   |   |   |   |   |   |
            X   X   X   X   X   |   |   0    Reset Slave
                                |   0 -----  IPL-request Slave
                                1 ---------  Interrupt Slave
```

Bit 0 gives a hardware reset of the slave, this port excluded.
Bit 1 is read by the slave at Port 20H (bit 1), to force the slave for a new IPL.
Bit 2 forces an MSC-interrupt at the slave, used to indicate a completed transfer.

2.5.6.2 FIFO Networking

The PMU 80-3 board is equipped with a Dual Channel 8-bit hardware FIFO, Z8060.
The FIFO is located between EMM-bus and Local-bus as follows:



The Internal FIFO Status " NOT EMPTY " causes an Interrupt (NIR1) to the processor.

The FIFO can be regarded as an output port at the EMM Bus (not readable). On the Local Bus it is available as an input port (readable only).

The port address to load the FIFO via the EMM Bus is as follows:

41H MASTER FIFO
43H SLAVE 1 FIFO
45H SLAVE 2 FIFO
47H SLAVE 3 FIFO
49H SLAVE 4 FIFO
5FH SLAVE 15 FIFO

The port address to read the FIFO via the Local Bus is 2CH.

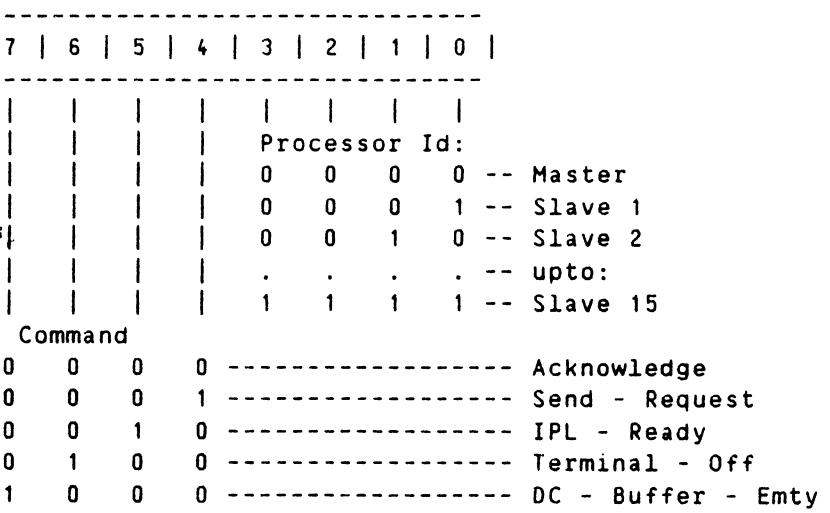
Note that the FIFO inverts the data between EMM and Local Bus

2.5.6.3 FIFO Bit Assignment

The Slave can inform the Master about a required action by sending a command into the FIFO of the Master.
After execution of this command the Master informs the Slave about this via the Master/Slave control port (see 2.5.4.1)

Note that this FIFO Command Processing is only used if all processor boards are PMU 80-3. In all other circumstances the Master should poll the slave at regular moments to check if the Slave requires service.

FIFO COMMAND LAYOUT



2.5.6.4 Master/Slave Communication Area

The next bytes in the System area of the RAM are used to communicate between Master and Slave:

```
0040H     MSCMD     MASTER-SLAVE COMMAND BYTE

Bit  7    ----------
     6    terminal off handling active          ;set by slave
     5    < Rel.2.1:receive-ready               ;set by master
     4    < Rel.2.1:send-ready                  ;set by master
     3    ------------
     2    intermediate-boot-code-available      ;set by master
     1    interrupt-acknowledge-request         ;set by master
     0    batch-processor,IPL-requested         ;set by master


0041H     SMSTA     SLAVE-MASTER STATUS

Bit  7    slave-terminal-on                     ;set by slave
     6    slave-terminal-off                    ;set by slave
     5    < Rel.2.1:slave-receive-request       ;set by slave
     4    < Rel.2.1:slave-send-request          ;set by slave
     3    slave-IPL-request                     ;set by slave
     2    IPL-ready                             ;set by slave
     1    slave-interrupt-acknowledge           ;answer to MSCMD /1
     0    ---------------


0042H     SLPRES    SLAVE PRESENT BYTE

Bit  0    Slave present                         ;set by slave

     3    DC-data-transmitted                   ;set by DC-node


0043H     SMSGLN    SLAVE MESSAGE LENGTH

0044/45H  SMSGAD    SLAVE MESSAGE BUFFER ADDRESS

0046H     SMSDID    SLAVE MESSAGE DESTINATION ADDRESS

0047/48H  TABADR    ADDRESS OF CIRCUIT TABLE

005AH     MSGINT    MESSAGE INTERFACE (FROM REL.2.1)

Bit  3    Slave-receive-request                 ;set by slave
     2    Slave-send-request                    ;set by slave
     1    Receive-ready                         ;set by master
     0    Send-ready                            ;set by master
```

CHAPTER 3 DISC CONTROL PAGE 3-1 tru 3-56

Continue next page.

3 DISC CONTROL

The P3000 System is supplied with two Disc interfaces to connect several types of Flexible and Fixed Disc Units.

The next interfaces are available:

- A Shugart Compatible Flexible Disc Interface (SA450), to connect several types of 5" Flexible Disc Drives.

- A SCSI Bus to connect a wide range of Controllers for Flexible or Hard Disc Units, Tape Units etc.

All Disc Devices are using DMA Data transfer. The DMA controller is described in section 3.1 .

Section 3.2 describes the control of the SA450 compatible Disc Drives.

Section 3.3 includes the SCSI Bus access and the Controllers available for P3000.

3.1 DMA Controller

3.1.1 General

The DMA Controller is able to control 4 independent data channels, two of them actually being used in P3000:

- Channel 2 for Flexible Disc (SA450)
- Channel 3 for Fixed Disc and Extensions(SCSI)

Programming of the DMA includes:

- Enabling of Controller (Set bit 6 of port 82H)
- Initialization of Controller
- Initialization of Address and Count Registers per Channel

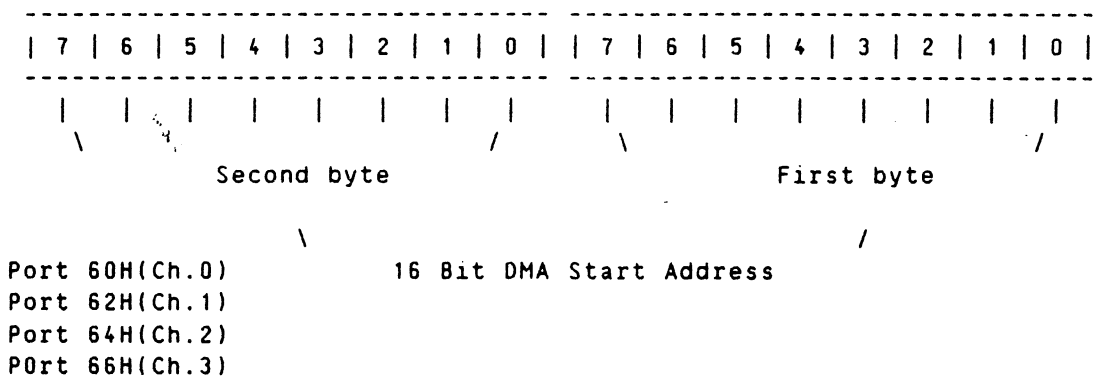
The next registers of the DMA Controller are accessable :

PORT	NAME	FUNCTION
60H	ADDRESS 0	
61H	COUNT 0	
62H	ADDRESS 1	
63H	COUNT 1	
64H	ADDRESS 2	Buffer Address for FDC Data
65H	COUNT 2	Length of Data Block for FDC
66H	ADDRESS 3	Buffer Address for SCSI Controller
67H	COUNT 3	Length of Data for SCSI Controller
68H	CMD/STATUS	
69H	REQUEST	
6AH	SINGLE MASK	
6BH	MODE	
6CH	CLEAR BYTE F/F	
6DH	M-CLEAR/READ TEMP	
6EH	--------	
6FH	ALL MASK	

3.1.2 Internal Registers DMA-Controller

3.1.2.1 Base and Current Address Register

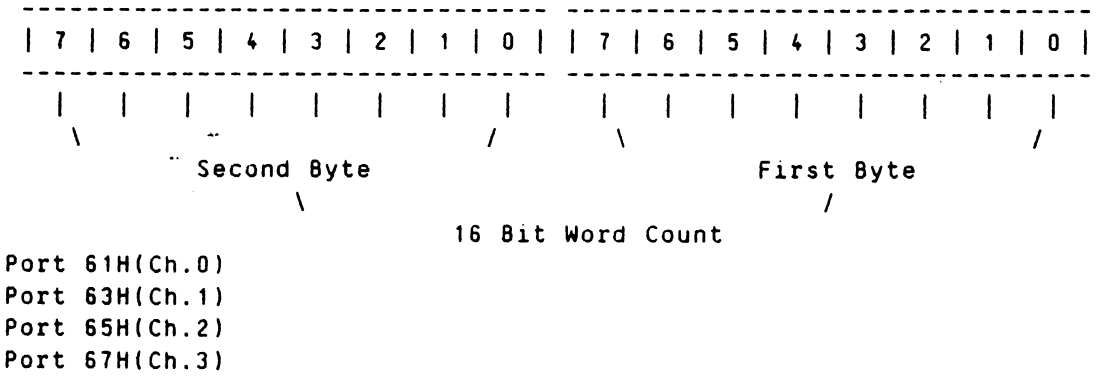
This is a register pair, specifying the start address of the DMA Buffer. It is loaded via two consecutive 8-bit I/O Write actions to the port number. The first byte must be the least significant part of the Address. Both the Base and Current Address is loaded via this I/O Write.
The Current Address Register is incremented for every transferred byte. When the auto-initialize bit is set in the Mode Register, the Current Address Register is automatically restored at the end of a DMA action.
There is one register pair for each channel.



Port 60H(Ch.0)
Port 62H(Ch.1)
Port 64H(Ch.2)
POrt 66H(Ch.3)

3.1.2.2 Base and Current Word Register

This register pair has to be loaded with the length of the data transfer.
The Current Word Register is decremented for every transferred byte. When Zero count is reached the action is terminated.
When the auto-initialize bit set this register is automatically restored at the end of the DMA action.



Port 61H(Ch.0)
Port 63H(Ch.1)
Port 65H(Ch.2)
Port 67H(Ch.3)

3.1.2.3 Status Register

This register contains two status bits for every channel.
One bit indicates whether the channel has a pending Data Request, the other bit indicates whether the channel has completed the DMA transfer.

```
          ---------------------------------
Port 68H  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   INPUT
          ---------------------------------
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 -- Channel 0 Terminated
            |   |   |   |   |   |   1 ------ Channel 1 Terminated
            |   |   |   |   |   1 ---------- Channel 2 Terminated
            |   |   |   |   1 -------------- Channel 3 Terminated
            |   |   |   1 ------------------ Channel 0 Request
            |   |   1 ---------------------- Channel 1 Request
            |   1 ------------------------- Channel 2 Request
            1 --------------------------- Channel 3 Request
```

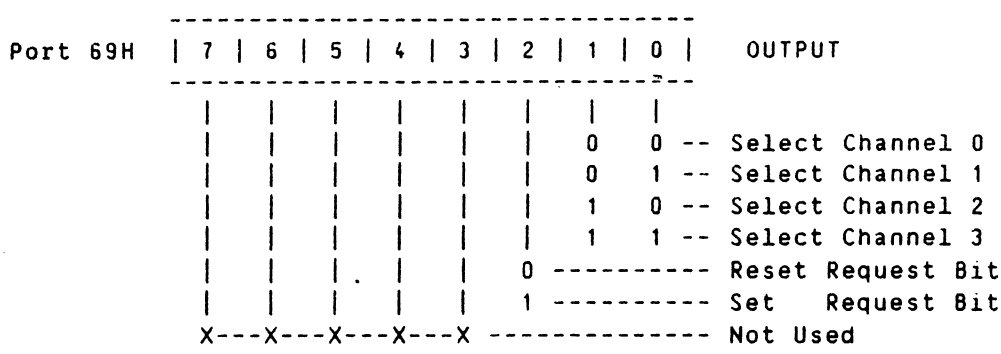
3.1.2.4 Command Register

This register is loaded with a number of parameters, specifying the general operation of the DMA Controller.

```
          ---------------------------------
Port 68H  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
          ---------------------------------
            |   |   |   |   |   |   |   |
            0   0   0   1   0   0   0   0     Default 10H
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   0 -- Memory to Memory Disable
            |   |   |   |   |   |   X ------ Not Used (P3000)
            |   |   |   |   |   0 ---------- Controller Enable
            |   |   |   |   |   1 ---------- Controller Disable
            |   |   |   |   0 -------------- Normal Timing(P3000)
            |   |   |   0 ------------------ Fixed Priority
            |   |   |   1 ------------------ Rotating Priority
            |   |   0 ---------------------- Late Write Selection
            |   0 ------------------------- DREQ Sense +
            0 --------------------------- DACK Sense -
```

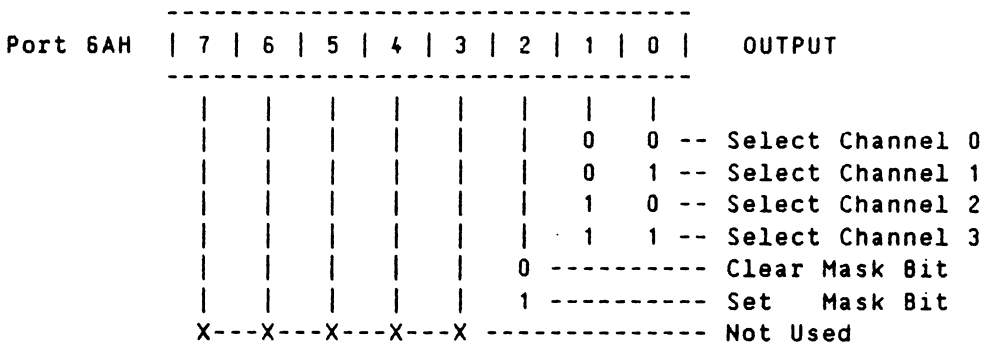
3.1.2.5 Request Register

This register can be used to generate a Software Data Request, mainly used for memory to memory transfers, which are not used in P3000.



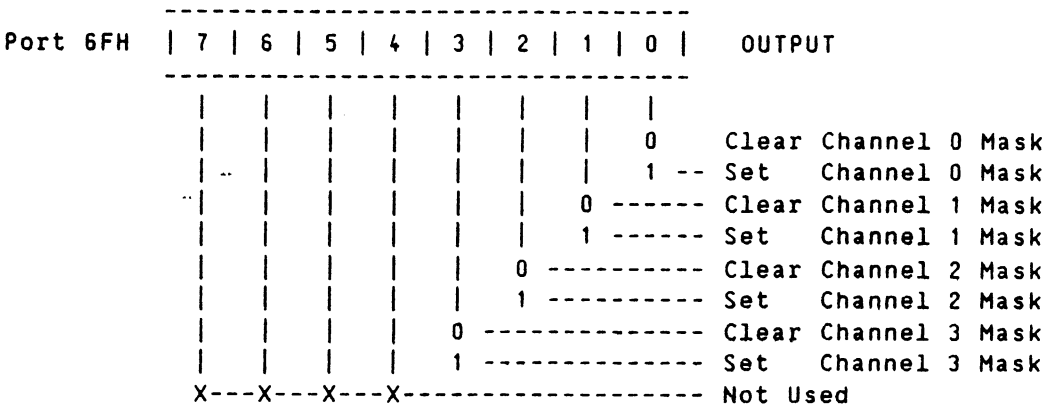
3.1.2.6 Write Single Mask Register

Via this register a single channel can be masked, to disable the hardware Data Request.



3.1.2.7 Write All Mask Register

All four channels can be masked, to disable the hardware Data Request, via one command to this port.



3.1.2.8 Mode Register

Each of the four DMA Channels can be set individually to a certain mode via the next output to port 68H :

```
          ---------------------------------
Port 68H  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
          ---------------------------------
            |   |   |   |   |   |   |   |
            0   1   0   1   r   w   c   c    Default 5XH
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   0   0 -- Select Channel 0
            |   |   |   |   |   |   0   1 -- Select Channel 1
            |   |   |   |   |   |   1   0 -- Select Channel 2
            |   |   |   |   |   |   1   1 -- Select Channel 3
            |   |   |   |   0   0 ---------- Verify
            |   |   |   |   0   1 ---------- Write (to Memory)
            |   |   |   |   1   0 ---------- Read (from Memory)
            |   |   |   |   1   1 ---------- Illegal
            |   |   |   0 ------------------ Auto Initialize Disable
            |   |   |   1 ------------------ Auto Initialize Enable
            |   |   0 ---------------------- Address Increment
            |   |   1 ---------------------- Address Decrement
            0   0 ------------------------- Demand  Mode
            0   1 ------------------------- Single  Mode
            1   0 ------------------------- Block   Mode
            1   1 ------------------------- Cascade Mode
```

3.1.2.9 Clear Byte Pointer

The Address and Word Count Registers are loaded in two steps with a 16 bit value. The Byte Pointer keeps track of this load action.
In case of doubt about command flow, this pointer can be reset to point to the LSB to be loaded.
Any value output to Port 6CH is sufficient.

3.1.2.10 Master Clear

Any output to Port 6DH forces the DMA Controller to initial state, only the Address and Word Registers are not reset.

3.2 Flexible Disc Control

A maximum of four Flexible Disk Drives, both single- and double sided, can be controlled via the FDC located at the SESCO Board.
The hardware however, supports only the connection of upto two Disc Drives.

3.2.1 General

The main circuit to control the Drives is the uPD 765, capable of performing 15 different commands. Each command is sent by a multiple byte transfer from the processor.
Apart from this some control ports are available at the SESCO Board, to control various signals e.g. Motor On. These ports should be set to the proper values before programming the FDC.

This results in the next procedure to access a Disc Drive:

INITIALIZATION

- Program the DMA-Controller (Channel 2)
- Program the FD Control Ports

COMMAND PHASE

- Program the FDC

EXECUTION PHASE

- Command is executed by the FDC, data exchange (if required) is performed by the DMAC.
- Command Completion gives a FDC Interrupt.

RESULT PHASE

- Status bytes must be read from FDC.

Any command or status transfer to and from the FDC has to be done by checking the Main Status Register of the FDC, this register is mainly used for handshaking between processor and FDC.

The next registers are available for Flexible Disc Control:

PORT	DIR	NAME	FUNCTION
A0H	IN	FDC-MSR	Main Status Register of FDC
A2H	I/O	FDC-DATA	All transfers to/from FDC
A8H	OUT	CP1	"Interface Control"
A8H	IN	CP3	"Test Status"
AAH	OUT	CP2	"Test Control"
64H	OUT	ADDRESS 2	DMA Address Register(see section 3.1)
66H	OUT	COUNT 2	DMA Count Register(see section 3.1)

3.2.2 Register Description

3.2.2.1 Control Port 1

This port is cleared to "0" after Master Reset.

```
          ---------------------------------
Port 0A8H | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
          ---------------------------------
            |   |   |   |   |   |   |   |
            1   1   1   1   X   1   X   1    Default 0F5H
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   0 -- FDC Reset(>4 ms)
            |   |   |   |   |   |   |   1 -- Enable FDC
            |   |   |   |   |   |   X ------ Not Used
            |   |   |   |   |   1 ---------- Enable  Interface
            |   |   |   |   |   0 ---------- Disable Interface
            |   |   |   |   X ---------------- Not Used
            |   |   |   1 ------------------- Motor  On  1
            |   |   1 --------------------------- Motor  On  2
            |   1 ----------------------------- In Use LED 1 On
            1 ------------------------------- In Use LED 2 On
```

3.2.2.2 Control Port 2

This port is cleared to "0" after Master Reset.

```
          ---------------------------------
Port 0AAH | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
          ---------------------------------
            |   |   |   |   |   |   |   |
            1   X   X   X   X   X   1   1    Default 83H
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 -- Read/Write test reset
            |   |   |   |   |   |   0 ------ Test LED On
            |   |   |   |   |   |   1 ------ Test LED Off
            |   X   X   X   X   X ---------- Not Used
            1 ------------------------------ Write Precom.Inhibit
```

3.2.2.3 Control Port 3

```
          ---------------------------------
Port 0A8H | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   INPUT
          ---------------------------------
            |   |   |   |   |   |   |   |
            0   0   I   D   0   S   0   R
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   0 -- Ready Test Drive
            |   |   |   |   |   |   0 ------ Not Used
            |   |   |   |   |   0 ---------- Step Command Inward
            |   |   |   |   |   1 ---------- Step Command Outward
            |   |   |   |   0 -------------- Read/Write operation
            |   |   |   0 ------------------ Read/Write Data Cont.
            |   |   0 ---------------------- Interrupt FDC
            0   0 ------------------------- Not Used
```

3.2.2.4 Main Status Register FDC

```
          ---------------------------------
Port 0A0H | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   INPUT
          ---------------------------------
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 -- Seek Mode Drive 0
            |   |   |   |   |   |   1 ------ Seek Mode Drive 1
            |   |   |   |   |   1 ---------- Seek Mode Drive 2
            |   |   |   |   1 -------------- Seek Mode Drive 3
            |   |   |   1 -- FDC Busy (Read/Write Cmd)
            |   |   1 -- FDC in Non-DMA Mode
           RQM DIO
            0   X -- FDC Not Ready For Transfer
            1   1 -- Data/Status from FDC into Processor
            1   0 -- Command/Data from Processor into FDC
```

3.2.2.5 Data Register FDC

Port 0A2H is the Data Register of the FDC. All Command Bytes, Status Information and Data are transferred via this register.
The transfer is to be synchronized via the two handshaking bits DIO and RQM of the Main Status Register.
The Command strings and possible Status bytes are explained in sect.3.2.3

COMMAND SUMMARY (MFM Codes)

C6	Read Data
C2	Read Track
C5	Write Data
D1	Scan Equal
4A	Read Identifier
4D	Format Track
07	Recalibrate
0F	Seek
03	Specify
08	Sense Interrupt Status
04	Sense Drive Status

3.2.3 FDC Instruction Set

3.2.3.1 Read Commands

The Read Data Command starts reading the disc from the specified sector number upto end of track. The command may be terminated if Terminal Count is activated (from DMAC).
The MT bit allows reading from both sides(Read sector 0, side 0 upto las sector, side 1).
The SK bit set causes the command to skip data marked as "deleted". If the bit is not set, an error bit is set when "deleted" data is found and the command is terminated.
The MF bit selects MFM (1) or FM (0) mode of operation.

The Read Deleted Data Command is the same as Read Data, except that "deleted" data is read and normal data is skipped if SK is set.

The Read Track Command reads an entire track as a continuous data stream.
Number of Sectors are read starting from the first sector after the Index hole. Even erroneous data is read.

COMMAND PHASE

BYTE 1	MT	MF	SK	0	0	1	1	0	READ DATA	0C6H
	MT	MF	SK	0	1	1	0	0	READ DELETED DATA	0CCH
	MT	MF	SK	0	0	0	1	0	READ TRACK	0C2H
	|	|	|						
	|	|	1	----------	----------	----------	----------	----------	Skip Deleted Address Mark	
	|	0	----------	----------	----------	----------	----------	FM Mode selected	
	|	1	----------	----------	----------	----------	----------	MFM Mode selected	
	1	----------	----------	----------	----------	----------	----------	----------	Multi-track	

BYTE 2	X	X	X	X	X	HD	US1	US0	
						|	|	|	
						|	0	0	-- Drive 0
						|	0	1	-- Drive 1
						0	----------	----------	Head 0
						1	----------	----------	Head 1

BYTE 3	CYLINDER NUMBER	0 - 79
BYTE 4	HEAD ADDRESS	0 or 1
BYTE 5	SECTOR NUMBER	1 - 16
BYTE 6	NUMBER OF BYTES / SECTOR	2**N*128(01H=256(Default))
BYTE 7	END OF TRACK	Final Sector(10H Default)
BYTE 8	GAP LENGTH	GAP 3 (0EH Default)
BYTE 9	DATA LENGTH	Sector length if Byte 5=00H

EXECUTION PHASE : Data transfer from FDC to Memory by DMAC

RESULT PHASE

BYTE 1	STATUS REGISTER 0
BYTE 2	STATUS REGISTER 1
BYTE 3	STATUS REGISTER 2
BYTE 4	CYLINDER NUMBER
BYTE 5	HEAD NUMBER
BYTE 6	SECTOR NUMBER
BYTE 7	NUMBER OF BYTES

3.2.3.2 Write commands

The Write Data Command starts writing to disc from the specified sector number upto end of track. The command may be terminated if Terminal Count is activated (from DMAC). The MT bit allows writing to both sides(Read sector 0, side 0 upto sector L, side 1). The MF bit selects MFM (1) or FM (0) mode of operation.

The Write Deleted Data Command is the same as Write Data, except that a Deleted Data Mark is written at the beginning of a data field.

COMMAND PHASE

BYTE 1	MT	MF	0	0	0	1	0	1	WRITE DATA	0C5H
	MT	MF	0	0	1	0	0	1	WRITE DELETED DATA	0C9H

MF: 0 ---------- FM Mode selected; 1 ---------- MFM Mode selected

MT: 1 ---------- Multi-track

BYTE 2	X	X	X	X	X	HD	US1	US0	

US1 | US0: 0 | 0 -- Drive 0; 0 | 1 -- Drive 1

HD: 0 ---------- Head 0; 1 ---------- Head 1

BYTE 3	CYLINDER NUMBER	0 - 79
BYTE 4	HEAD ADDRESS	0 or 1
BYTE 5	SECTOR NUMBER	1 - 16
BYTE 6	NUMBER OF BYTES / SECTOR	2**N*256 (01H = 256 (Default))
BYTE 7	END OF TRACK	Final Sector (10H Default)
BYTE 8	GAP LENGTH	GAP 3 (0EH Default)
BYTE 9	DATA LENGTH	Sector length if Byte 6 = 00H

EXECUTION PHASE

Data transfer from Memory to FDC by DMAC.

RESULT PHASE

BYTE 1	STATUS REGISTER 0
BYTE 2	STATUS REGISTER 1
BYTE 3	STATUS REGISTER 2
BYTE 4	CYLINDER NUMBER
BYTE 5	HEAD NUMBER
BYTE 6	SECTOR NUMBER
BYTE 7	NUMBER OF BYTES

3.2.3.3 Scan commands

The scan command allows data from disc to be compared with data in memory.
The data from disc is compared on byte-by-byte basis to meet the conditions =,<,> than data from processor. The scan starts at the Sectornumber and ends at either a Terminal Count or End Of Track.

COMMAND PHASE

```
BYTE 1    MT  MF  SK  1   0   0   0   1    SCAN EQUAL              0D1H
          MT  MF  SK  1   1   0   0   1    SCAN LOW OR EQUAL       0D9H
          MT  MF  SK  1   1   1   0   1    SCAN HIGH OR EQUAL      0DDH
          |   |   |
          |   |   1 ---------------------- Skip Deleted Address Mark
          |   0 ------------------------- FM  Mode selected
          |   1 ------------------------- MFM Mode selected
          1 ----------------------------- Multi-track

BYTE 2    X   X   X   X   X  HD  US1 US0
                             |   |   |
                             |   0   0 -- Drive 0
                             |   0   1 -- Drive 1
                             0 ---------- Head  0
                             1 ---------- Head  1

BYTE 3    CYLINDER NUMBER                 0 - 79
BYTE 4    HEAD ADDRESS                    0 or 1
BYTE 5    SECTOR NUMBER                   1 - 16
BYTE 6    NUMBER OF BYTES / SECTOR        2**N*256 (01H=256(Default))
BYTE 7    END OF TRACK                    Final Sector (10H Default)
BYTE 8    GAP LENGTH                      GAP 3 (0EH Default)
BYTE 9    SCANSTEP                        01H = >Continuos Sectors
                                          02H = >Alternate Sectors
```

EXECUTION PHASE

Data transfer between FDC and Processor

RESULT PHASE

```
BYTE 1    STATUS REGISTER 0
BYTE 2    STATUS REGISTER 1
BYTE 3    STATUS REGISTER 2
BYTE 4    CYLINDER NUMBER
BYTE 5    HEAD NUMBER
BYTE 6    SECTOR NUMBER
BYTE 7    NUMBER OF BYTES
```

3.2.3.4 Read Identifier

This Command is used to give the present position of the recording head.

COMMAND PHASE

```
BYTE 1    0   MF  0   0   1   0   1   0    4AH Default
              |
              0 -------------------------- FM  Mode selected
              1 -------------------------- MFM Mode selected

BYTE 2    X   X   X   X   X  HD  US1 US0
                               |   |   |
                               |   0   0 -- Drive 0
                               |   0   1 -- Drive 1
                              0 ---------- Head  0
                              1 ---------- Head  1
```

EXECUTION PHASE

The first correct ID is stored in the Data Register

RESULT PHASE

```
BYTE 1    STATUS REGISTER 0
BYTE 2    STATUS REGISTER 1
BYTE 3    STATUS REGISTER 2
BYTE 4    CYLINDER NUMBER
BYTE 5    HEAD NUMBER
BYTE 6    SECTOR NUMBER
BYTE 7    NUMBER OF BYTES
```

3.2.3.5 Format Track

The Format Commands allows an entire track to be formatted. After the Index Pulse the next Data are written to disc: Gaps, Address Marks, ID Fields and Data Fields. The formatting data is controlled by the values in the command. The ID Field for each sector is delivered during execution phase(four Data Requests/Sector).

Note: This format is the IBM System 34 (DD) or System 3740 (SD) standard and not according to ECMA 70 standard.
The Hardware does not allow execution of this command!

COMMAND PHASE

```
BYTE 1    0   MF  0   0   1   1   0   1    4DH Default
              |
              0 ------------------------- FM  Mode selected
              1 ------------------------- MFM Mode selected

BYTE 2    X   X   X   X   X  HD  US1 US0
                               |   |   |
                               |   0   0 -- Drive 0
                               |   0   1 -- Drive 1
                              0 ---------- Head  0
                              1 ---------- Head  1

BYTE 3    BYTES/SECTOR          (01)
BYTE 4    SECTORS/TRACK         (10)
BYTE 5    GAPLENGTH (GAP 3)     (32)
BYTE 6    FILLER BYTE           (E5)
```

EXECUTION PHASE

The FDC Formats an entire cylinder, the ID Information for each sector (Cylinder,Head,Sector,Bytes/sector) is requested from the processor.

RESULT PHASE

```
BYTE 1    STATUS REGISTER 0
BYTE 2    STATUS REGISTER 1
BYTE 3    STATUS REGISTER 2
BYTE 4    CYLINDER NUMBER
BYTE 5    HEAD NUMBER
BYTE 6    SECTOR NUMBER
BYTE 7    NUMBER OF BYTES
```

3.2.3.6 Recalibrate

This command positions the head to track 0.

COMMAND PHASE

BYTE 1	0	0	0	0	0	1	1	1	07H
BYTE 2	X	X	X	X	X	0	US1	US0	

US1 | US0
0 | 0 -- Drive 0
0 | 1 -- Drive 1

EXECUTION PHASE

Head retracted to Track 0(maximum 77 steps), terminated with Interrupt.
A Sense Interrupt Command must be executed to release the interrupt.

3.2.3.7 Seek

This command is used to position the head to a specified track.

COMMAND PHASE

BYTE 1	0	0	0	0	1	1	1	1	0FH
BYTE 2	X	X	X	X	X	0	US1	US0	

US1 | US0
0 | 0 -- Drive 0
0 | 1 -- Drive 1

BYTE 3 NEW CYLINDER NUMBER

EXECUTION PHASE

Head positioned to new cylinder, terminated with Interrupt.
A sense Interrupt Command must be given to release the interrupt.

3.2.3.8 Specify

This command sets the value of some internal timers.

COMMAND PHASE

```
BYTE 1    0   0   0   0   0   0   1   1    03H

BYTE 2    s3  s2  s1  s0  h3  h2  h1  h0   DFH Default
           \          /    \          /
            \        /      \        /
             \      /          ---------- Head Unload Time (N * 32ms)
               --------- Step Rate Time ((16-N) * 2ms)


BYTE 3    h6  h5  h4  h3  h2  h1  h0  nd   02H Default

           \                      /   |
            \                    /    1 -- Non-DMA Mode
             \                  /     0 -- DMA Mode
               ---------------------- Head Load Time ((N+1) * 4ms)
```

EXECUTION PHASE

The FDC Controller loads his internal timers with the specified values.

3.2.3.9 Sense Interrupt Status

An Interrupt is generated for one of the following reasons:

1. At the result phase of Read, Write,Format and Scan Commands
2. If the Drive Ready line changes
3. At End of Seek or Recalibrate
4. During Execution Phase in Non-DMA Mode

Interrupts caused by reason 2 and 3 may be uniquely defined by this Sense Interrupt Status Command.

COMMAND PHASE

```
BYTE 1    0   0   0   0   1   0   0   0    08H


BYTE 2    X   X   X   X   X  HD  US1 US0
                             |   |   |
                             |   0   0 -- Drive 0
                             |   0   1 -- Drive 1
                            0 ---------- Head  0
                            1 ---------- Head  1
```

RESULT PHASE

```
BYTE 1    STATUS REGISTER 0
BYTE 2    PRESENT CYLINDER
```

3.2.3.10 Sense Drive Status

This command may be used to obtain the status of the Disc Drives.

COMMAND PHASE

BYTE 1	0	0	0	0	0	1	0	0	04H

BYTE 2	X	X	X	X	X	HD	US1	US0

HD: 0 ---------- Head 0; 1 ---------- Head 1

US1 US0: 0 0 -- Drive 0; 0 1 -- Drive 1

RESULT PHASE

BYTE 1 STATUS REGISTER 3

7	6	5	4	3	2	1	0

- 7 --- Fault
- 6 --- Write Protect
- 5 --- Ready
- 4 ---- Track 0
- 3 ---- Two Side
- 2 --- Head 1
- 1 0 -- Drive 0; 1 -- Drive 1

3.2.4 Status Description

The next status bytes are to be read in the result phase of most of the commands.

```
          ---------------------------------
REGISTER  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
   0      ---------------------------------
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   0   0 -- Drive 0 Interrupt
            |   |   |   |   |   |   0   1 -- Drive 1 Interrupt
            |   |   |   |   |   1 ----- Head  1 Interrupt
            |   |   |   |   1 ----- Drive Not Ready
            |   |   |   1 ----- Fault
            |   |   1 ---- Seek End
            0   0 --- Normal Termination
            0   1 --- Abnormal Termination
            1   0 --- Invalid Command Issue
            1   1 --- Abnormal Termination(Ready signal changed)
```

```
          ---------------------------------
REGISTER  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
   1      ---------------------------------
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 --- Missing Address Mark
            |   |   |   |   |   |   1 ---- Write Protect
            |   |   |   |   |   1 ---- No Data
            |   |   |   |   1 ----- Not Used
            |   |   |   1 ----- Overrun
            |   |   1 ---- Data Error
            |   1 ---- Not Used
            1 ---- End Of Cylinder
```

```
          ---------------------------------
REGISTER  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
   2      ---------------------------------
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 --- Missing Address Mark
            |   |   |   |   |   |   1 ---- Bad Cylinder
            |   |   |   |   |   1 ---- Scan Not Satisfied
            |   |   |   |   1 ----- Scan Equal Hit
            |   |   |   1 ----- Wrong Cylinder
            |   |   1 ---- Data Error(Data Field)
            |   1 ---- Control Mark(Deleted Mark Found)
            1 ---- Not Used
```

3.3 SCSI DEVICE CONTROL

This section describes the control of the SCSI Bus and the devices connected.

3.3.1 SCSI Control

Control of the SCSI-Bus is realized via some control ports,located at the SESCO Board. These ports can be considered as the adaption between the EMM System Bus and the SCSI-Bus.

3.3.1.1 Transfer Phases

Communication via the SCSI Bus is performed in a number of Phases, using the handshaking signals REQuest, C/D,and I/O.

SELECTION PHASE

The processor selects one of the controllers connected to the bus. It sets the SELect bit and writes the controller address to the bus. It then waits for either signal BuSY and REQuest or an interrupt to start the Command phase. The selected controller is now autonomous. The signal SELect should be released again.
Selection of a controller is done in the next sequence:

1. Output the controller address to the databus.
2. Raise the SELect line.
The selected controller raises the BuSY line
3. Wait for BuSY line
4. Release the SELect line

COMMAND PHASE

The controller requests for a Command Descriptor Block. Each command byte is transferred via a Command REQuest - ACKnowledge handshaking. Reception of the last command byte starts the Execution phase. Transfer can be done either on Interrupt or in Polling Mode.
The interrupt routine on Command Request should send one byte of the command to the controller.
The next handshaking sequence should be used in Polling Mode:

1. Wait for REQuest
2. Check for Command Request(C/D=0,I/O=1)
3. Send Command Byte
4. Continue 1,2,3 untill all command bytes are sent

Note 1: The first command after a power-on will not be executed in each controller, but is sometimes used to inform the host about the status of the controller.

Note 2: During execution of a Backup/Restore command the ATtentioN line is used in special way by the host (see Backup/Restore).

EXECUTION PHASE

The command is executed by the controller. If Data Transfer is included in the command this will be performed either by the Processor or by the DMA Controller. Data REQuest - ACKnowledge handshaking is used for each byte to be transferred.
The next handshaking should be used in Non-DMA Mode:
1. Wait for REQuest
2. Check for Data Request(C/D=1)
3. Read Data Byte(I/O=0) or Write Data Byte(I/O=1)
4. Continue 1,2,3 untill all data is transferred

In DMA Mode a DMA Request for Channel 3 is given for every Data Request from the controller .

STATUS PHASE

Two bytes of status information must be transferred in this phase. Each byte is transferred via a Command REQuest - ACKnowledge handshaking.
At the end of the Status phase the SCSI Bus is released by the controller (deactivation of BuSY signal).
The status bytes of the controller can be returned either in interrupt mode or in non-interrupt mode.

A REQuest to send Status (REQ=1,C/D=0,I/O=0) generates an SCSI interrupt. The interrupt routine has to read one status byte from the controller.

In Polling Mode the next handshaking should be used:
1. Wait For REQuest
2. Check for Status Request (C/D=0,I/O=0)
3. Read Status byte
4. continue 1,2,3 for second Status Byte

RESET

In the initialization phase the controllers must be forced to an initial state.
This is realised by activating the ReSeT line , accessible via port 82: bit 6, for a period of minimal 100 nS.
After this reset action most of the controllers must be initialised again via a command, to inform the controller about the Drive characteristics etc..

The ReSeT signal is also used in the Extension Cabinets to control Remote Power On of these Cabinets.
An inactive ReSeT signal forces the Extension Cabinet to switch Power-On.
Activating the ReSeT signal for a period longer than 250 mS forces the Extension Cabinet to switch Power Off.

The ReSeT signal is also used as an input signal from the SCSI Bus. Switching off the Mains of the Extension Cabinet forces the signal ReSeT to Active. In this case the System is informed about a Controller Reset via input port 82,Bit6 (SCSI Reset condition).
In practice this means that all the connected controllers should be initialised again. After this the reset condition must be cleared with an output to port 82H, Bit 0 (Clear Reset Condition).

3.3.1.2 SCSI Ports

There is a minor difference in the assignment of signals to the SCSI Ports between the SESCO and SASI-AD Boards.

3.3.1.2.1 SCSI Ports SESCO

SCSI DATA PORT

```
          ---------------------------------
Port 80H  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   IN/OUTPUT
          ---------------------------------
            \                           /
             \                         /
              Command, Data, and Status
```

SCSI CONTROL PORT

```
          ---------------------------------
Port 82H  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
          ---------------------------------
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   0 -- Clear Reset Condition
            |   |   |   |   |   |   1 ------ Select SCSI Controller
            |   |   |   |   |   X ---------- Not Used
            |   |   |   |   0 -------------- Clear Interrupt
            |   |   |   0 ------------------ Clear DMA Request
            |   |   0 -------------------- Reset DMA Controller
            |   1 ---------------------------- Reset SCSI Controllers
            1 ------------------------------ Set ATTention Condition
```

SCSI STATUS PORT

```
          ---------------------------------
Port 82H  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   INPUT
          ---------------------------------
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   0 -- Controller Sends
            |   |   |   |   |   |   |   1 -- Controller Receives
            |   |   |   |   |   |   0 -- Command
            |   |   |   |   |   |   1 -- Data
            |   |   |   |   |   0 -- Message
            |   |   |   |   0 -- SESCO (No Flexco/Sasi-ad)
            |   |   |   0 -- REQuest
            |   |   0 -- BuSY
            |   1 -- SCSI Reset Condition
            1 -- Privileged Mode (P3800)
```

3.3.1.2.2 SCSI Ports SASI-AD

SCSI DATA PORT

```
            ---------------------------------
Port 80H    | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   IN/OUTPUT
            ---------------------------------
              \                             /
               \                           /
                 Command, Data, and Status
```

SCSI CONTROL PORT

```
            ---------------------------------
Port 82H    | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
            ---------------------------------
              |   |   |   |   |   |   |   |
              |   |   |   |   |   |   |   1 -- Select Int. SCSI Controller
              |   |   |   |   |   |   1 ------ Select Ext. SCSI Controller
              |   |   |   |   |   0 ---------- Reset Int.  SCSI Controller
              |   |   |   |   0 -------------- Clear Interrupt
              |   |   |   0 ------------------ Clear DMA Request
              |   |   0 -------------------- Reset DMA Controller
              |   1 ---------------------------- Reset Ext.  SCSI Controller
              1 ------------------------------ Not Used
```

SCSI STATUS PORT

```
            ---------------------------------
Port 82H    | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   INPUT
            ---------------------------------
              |   |   |   |   |   |   |   |
              |   |   |   |   |   |   |   0 -- Controller Sends
              |   |   |   |   |   |   |   1 -- Controller Receives
              |   |   |   |   |   |   0 -- Command
              |   |   |   |   |   |   1 -- Data
              |   |   |   |   |   0 -- Message
              |   |   |   |   0 -- BuSY Internal Controller
              |   |   |   0 -- REQuest
              |   |   0 -- BuSY External Controller
              |   1 -- Not Used
              1 -- Not Used
```

3.3.1.3 SCSI Controller Addressing

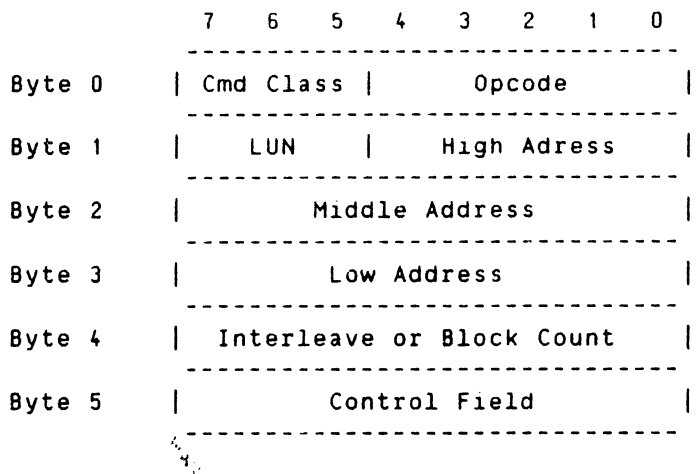
During the selection phase the controller address is offered to the SCSI Bus. The default address of the P3000 Controllers is as follows:

CUA	ADR	DEVICE	CONTROLLER	REMARKS
7	80H	First FXD	FIXCO-5/XEBEC-S1410	Internal
6	40H	Second FXD	FIXCO-5/XEBEC-S1410	P3012
5	20H	---------		
4	10H	---------		
3	08H	BACKUP	TAPCO-Q	P3013
2	04H	8"FDD	XEBEC-S1401	P2621
1	02H	---------		Reserved for 5"FD/S1401
0	01H	HOST	SESCO	

3.3.2 Fixed Disc Commands (XEBEC S1410/FIXCO 5)

The Controller commands in this section are used to access the SEAGATE 406/412 or RODIME 202 Fixed Discs (5M or 10M).

All commands are formed by a six-byte control block as follows



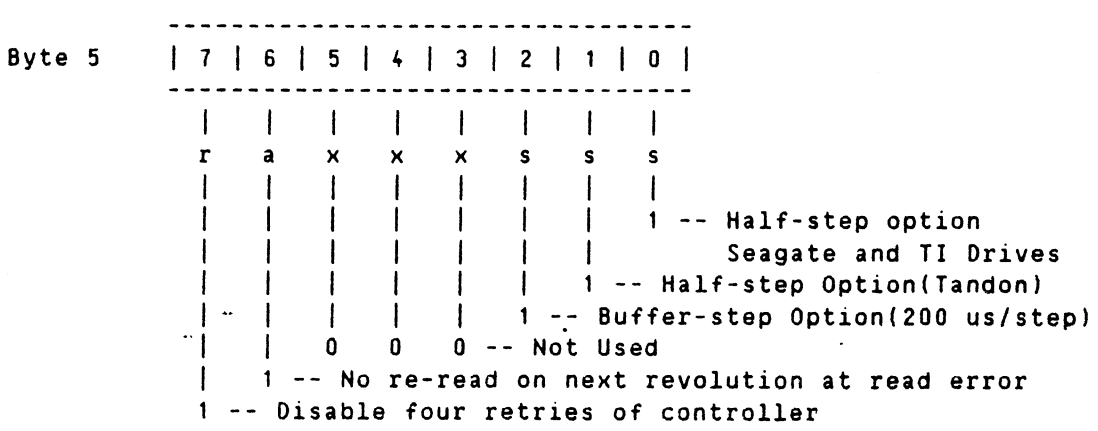
LUN is the Drive Number

Byte 1,2 and 3 specify a 21-bit logical data address, calculated as follows:

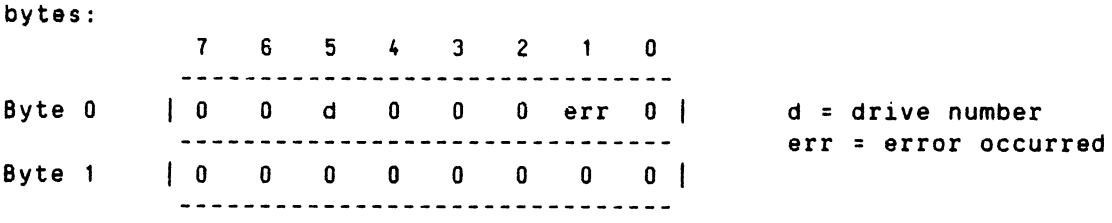
Logical Address=(CYADR*HDCYL+HDADR)*SETRK+SEADR

Where: CYADR = Cylinder Address
HDADR = Head Address
SEADR = Sector Address
HDCYL = Number of Heads/Cylinder
SETRK = Number of Sectors/Track

Byte 5 allows for the selection of several options as follows:



At the end of a command the controller returns the next two status bytes:



COMMAND SUMMARY SEAGATE/RODIME FXD

CODE	FUNCTION
00	Test Drive Ready
01	Recalibrate
03	Request Sense Status
04	Format Drive
05	Check Track Format
06	Format Track
07	Format Bad Track
08	Read
0A	Write
0B	Seek
0C	Initialize Drive Charateristics
0D	Read ECC Error Burst
E0	RAM Diagnostic
E3	Drive Diagnostic
E4	Controller Diagnostic
E5	Read Long
E6	Write Long

3.3.2.1 Test Drive Ready

This command selects the drive and verifies that the drive is ready.

	7	6	5	4	3	2	1	0	
Byte 0	0	0	0	0	0	0	0	0	00H
Byte 1	0	0	d	x	x	x	x	x	
Byte 2	x	x	x	x	x	x	x	x	
Byte 3	x	x	x	x	x	x	x	x	
Byte 4	x	x	x	x	x	x	x	x	
Byte 5	x	x	x	x	x	x	x	x	

3.3.2.2 Recalibrate

This command positions the head to track 0.

	7	6	5	4	3	2	1	0	
Byte 0	0	0	0	0	0	0	0	1	01H
Byte 1	0	0	d	x	x	x	x	x	
Byte 2	x	x	x	x	x	x	x	x	
Byte 3	x	x	x	x	x	x	x	x	
Byte 4	x	x	x	x	x	x	x	x	
Byte 5	r	0	0	0	0	s	s	s	Default 04H

3.3.2.3 Request Sense Status

This command must be issued immediately after an error is detected. The controller reurns four bytes of drive and controller status.

	7	6	5	4	3	2	1	0	
Byte 0	0	0	0	0	0	0	1	1	03H
Byte 1	0	0	d	x	x	x	x	x	
Byte 2	x	x	x	x	x	x	x	x	
Byte 3	x	x	x	x	x	x	x	x	
Byte 4	x	x	x	x	x	x	x	x	
Byte 5	x	x	x	x	x	x	x	x	

The next status bytes are returned at the DMA Address:

	7	6	5	4	3	2	1	0
Byte 0	av	Error Code						
Byte 1	LUN			High Adress				
Byte 2	Middle Address							
Byte 3	Low Address							

Byte 0 (bit 7) indicates if the address in the next 3 bytes is valid.

List of Error Codes

00	80	No Error
01	81	No Index
02	82	No Seek Completed
03	83	Write Fault
04	84	Drive Not Ready
06	86	No Track 00
10	90	ID Read Error
11	91	Data Error
12	92	Address Mark Not Found
14	94	Sector Not Found
15	95	Seek Error
18	98	Correctable Data Error
19	99	Bad Track
1A	9A	Format Error
20	A0	Invalid Command
21	A1	Illegal Disk Address
30	B0	RAM Diagnostic Failure
31	B1	ROM Checksum Error
32	B2	ECC Diagnostic Failure

3.3.2.4 Format Commands

Format Drive formats all sectors with ID and Data information , from the start address in the command to the end of the Disc.
Check Track Format checks the specified track for correct ID and Interleave.
Format Track formats the specified track.
Format Bad Track sets the bad-sector bit in the ID field.

	7	6	5	4	3	2	1	0		
Byte 0	0	0	0	0	0	1	0	0	04H	Format Drive
Byte 0	0	0	0	0	0	1	0	1	05H	Check Track Format
Byte 0	0	0	0	0	0	1	1	0	06H	Format Track
Byte 0	0	0	0	0	0	1	1	1	07H	Format Bad Track
Byte 1	0	0	d	High Adress						
Byte 2	Middle Address									
Byte 3	Low Address									
Byte 4	0	0	0	Interleave(1 to 16)						
Byte 5	r	0	0	0	0	s	s	s		

3.3.2.5 Read/Write Commands

READ reads the specified number of sectors starting with the address in the command block.
The WRITE Command writes the specified number of sectors to the Disc,starting with the Disc Address in the command block.
Read Long and WRite Long transfer the Data and four bytes of ECC data to the system, to be used in recovery and diagnostic operations.

	7	6	5	4	3	2	1	0	
Byte 0	0	0	0	0	1	0	0	0	08H Read
Byte 0	0	0	0	0	1	0	1	0	0AH Write
Byte 0	1	1	1	0	0	1	0	1	E5H Read Long
Byte 0	1	1	1	0	0	1	1	0	E6H Write Long
Byte 1	0	0	d	High Adress					
Byte 2	Middle Address								
Byte 3	Low Address								
Byte 4	Block Count								
Byte 5	r	a	0	0	0	s	s	s	

3.3.2.6 Seek Command

This Command initiates a seek to the specified track

	7	6	5	4	3	2	1	0	
Byte 0	0	0	0	0	1	0	1	1	0BH
Byte 1	0	0	d	High Adress					
Byte 2	Middle Address								
Byte 3	Low Address								
Byte 4	x	x	x	x	x	x	x	x	
Byte 5	r	0	0	0	0	s	s	s	

3.3.2.7 Initialize Drive Characteristics

This command is used to configure the controller to work with a certain Drive Type. After the command is sent, the controller expects an 8 byte block of data as listed below.

	7	6	5	4	3	2	1	0	
Byte 0	0	0	0	0	1	1	0	0	0CH
Byte 1	0	0	d	x	x	x	x	x	
Byte 2	x	x	x	x	x	x	x	x	
Byte 3	x	x	x	x	x	x	x	x	
Byte 4	x	x	x	x	x	x	x	x	
Byte 5	x	x	x	x	x	x	x	x	

DATA

	7	6	5	4	3	2	1	0	
Byte 0	c	c	c	c	c	c	c	c	c= Number of Cylinders
Byte 1	c	c	c	c	c	c	c	c	
Byte 2	0	0	0	0	h	h	h	h	h= Number of Heads
Byte 3	w	w	w	w	w	w	w	w	w= Starting cylinder Reduced Write Current
Byte 4	w	w	w	w	w	w	w	w	
Byte 5	p	p	p	p	p	p	p	p	p= Starting cylinder Write Precompensation
Byte 6	p	p	p	p	p	p	p	p	
Byte 7	0	0	0	0	e	e	e	e	e= Maximum ECC data burst length (08H Default)

3.3.2.8 Read ECC Burst Error Length

This command transfers one byte, containing the value of the ECC burst length detected at the last Read command. The byte is only valid after a correctable Ecc data error (Error Code 18H).

	7	6	5	4	3	2	1	0	
Byte 0	0	0	0	0	1	1	0	1	0DH
Byte 1	x	x	x	x	x	x	x	x	
Byte 2	x	x	x	x	x	x	x	x	
Byte 3	x	x	x	x	x	x	x	x	
Byte 4	x	x	x	x	x	x	x	x	
Byte 5	x	x	x	x	x	x	x	x	

3.3.2.9 Diagnostic Commands

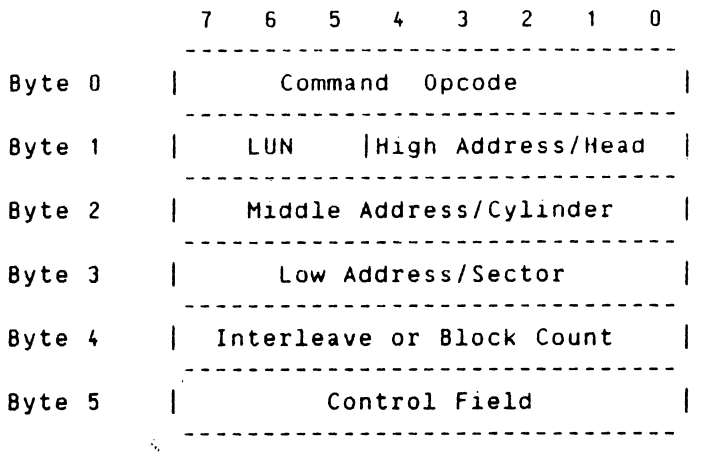
The RAM Diagnostic performs a data pattern test of the RAM Buffer.
The Drive Diagnostic performs a test of the Drive and Drive Interface. The controller sends recalibrate and seek commands and verify sector 0 of all the tracks.
The Controller Internal Diagnostics performs a self-test of the controller(Processor,Buffers,ROM and ECC circuitry)

	7	6	5	4	3	2	1	0		
Byte 0	1	1	1	0	0	0	0	0	E0H	RAM Diagnostic
Byte 0	1	1	1	0	0	0	1	1	E3H	Drive Diagnostic
Byte 0	1	1	1	0	0	1	0	0	E4H	Controller Diagnostic
Byte 1	0	0	d	x	x	x	x	x		
Byte 2	x	x	x	x	x	x	x	x		
Byte 3	x	x	x	x	x	x	x	x		
Byte 4	x	x	x	x	x	x	x	x		
Byte 5	x	x	x	x	x	x	x	x		

3.3.3 8" Flexible Disc Commands (P2621)

The commands in this Section are used to access the Flexible Disc Drive CDC 9406 via the XEBEC S1401 Controller.

All commands are formed by a six-byte control block as follows:



LUN is the Drive Number , allways unit 0 in P3000

If Control Field Bit 6 is Reset then Byte 1,2 and 3 specify a 21-bit logical data address, calculated as follows:

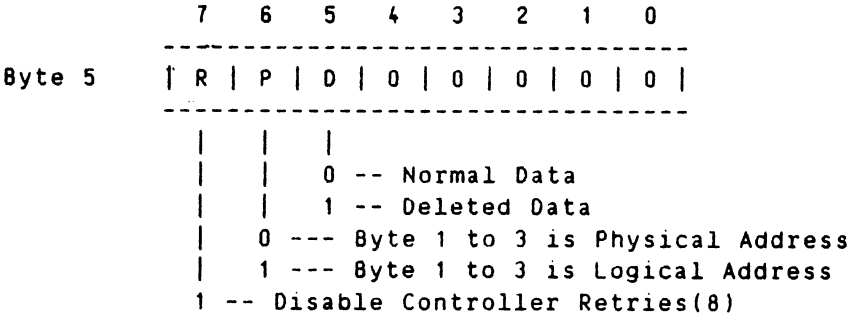
Logical Address=(CYADR*HDCYL+HDADR)*SETRK+SEADR

Where: CYADR = Cylinder Address
HDADR = Head Address
SEADR = Sector Address
HDCYL = Number of Heads/Cylinder
SETRK = Number of Sectors/Track

If Control Field Bit 6 is set then Byte 1,2 and 3 specify a physical address as follows:
Byte 1 is the Head Number(0 or 1)
Byte 2 is the Cylinder Number(0 to 76
Byte 3 is the Sector Number(0 to 25)

CONTROL FIELD

Byte 5 allows for the selection of several options as follows:



At the end of a command the controller returns the next two status bytes:

	7	6	5	4	3	2	1	0
Byte 0	0	0	d	0	0	0	err	0
Byte 1	0	0	0	0	0	0	0	0

d = drive number
err = when set: error occurred

COMMAND SUMMARY P2621

CODE	FUNCTION
00	Test Drive Ready
01	Recalibrate
03	Request Sense Status
04	Format Drive
06	Format Track
08	Read
0A	Write
0B	Seek
0C	Initialize Drive Charateristics
0D	Read ECC Error Burst
C1	Copy from Floppy Disc
C2	Copy to Floppy Disc
E0	RAM Diagnostic
E3	Drive Diagnostic
E4	Controller Diagnostic

3.3.3.1 Test Drive Ready

This command selects a drive and verifies that the drive is ready.

	7	6	5	4	3	2	1	0	
Byte 0	0	0	0	0	0	0	0	0	00H
Byte 1	0	0	0	x	x	x	x	x	
Byte 2	x	x	x	x	x	x	x	x	
Byte 3	x	x	x	x	x	x	x	x	
Byte 4	x	x	x	x	x	x	x	x	
Byte 5	x	x	x	x	x	x	x	x	

3.3.3.2 Recalibrate

This command positions the head to track 0.

	7	6	5	4	3	2	1	0	
Byte 0	0	0	0	0	0	0	0	1	01H
Byte 1	0	0	0	x	x	x	x	x	
Byte 2	x	x	x	x	x	x	x	x	
Byte 3	x	x	x	x	x	x	x	x	
Byte 4	x	x	x	x	x	x	x	x	
Byte 5	R	x	x	x	x	x	x	x	

3.3.3.3 Request Sense Status

This command must be issued immediately after an error is detected.

	7	6	5	4	3	2	1	0	
Byte 0	0	0	0	0	0	0	1	1	03H
Byte 1	0	0	0	x	x	x	x	x	
Byte 2	x	x	x	x	x	x	x	x	
Byte 3	x	x	x	x	x	x	x	x	
Byte 4	x	x	x	x	x	x	x	x	
Byte 5	x	x	x	x	x	x	x	x	

The controller returns the next four bytes at the DMA Address:

	7	6	5	4	3	2	1	0
Byte 0	av	0	Error Code					
Byte 1	LUN		High Adress					
Byte 2	Middle Address							
Byte 3	Low Address							

List of Error Codes (bit 7(av) indicates if the Address Bytes are valid.)

00	80	No Error
02	82	No Seek Completed
04	84	Drive Not Ready
06	86	No Track 00
07	87	Door Open
08	88	No Head Loaded
10	90	ID Read Error
11	91	Write Fault
12	92	Write Protected
14	94	Sector Not Found
15	95	Seek Error
16	96	Format Track Timeout
17	97	Format Track Not Complete
19	99	Two Sided Error
1A	9A	Wrong Data Mark
1B	9B	Pad Error: Wrong Sector in copy command
1D	9D	Last Data
1E	9E	Data Error
1F	9F	FDC Busy Error
20	A0	Invalid Command
21	A1	Illegal Disk Address
22	A2	Wrong Initialize Command
23	A3	Invalid Interleave
30	B0	Ram Diagnostic Failure
31	B1	Rom Checksum Error
32	B2	ECC Diagnostic Failure

3.3.3.4 Format Commands

Format Drive formats all sectors with ID and Data information , from the start address in the command to the end of the Disc.
Format Track formats the specified track.

	7	6	5	4	3	2	1	0	
Byte 0	0	0	0	0	0	1	0	0	04H Format Drive
Byte 0	0	0	0	0	0	1	1	0	06H Format Track
Byte 1	0	0	0	High Address/Head					
Byte 2	Middle Address/Cylinder								
Byte 3	Low Address/Don't care								
Byte 4	0	0	0	Interleave					
Byte 5	R	P	D	0	0	0	0	0	

3.3.3.5 Read/Write Commands

Read reads the specified number of sectors starting with the address in the command block.
The Write Command writes the specified number of sectors to the Disc,starting with the Disc Address in the command block.

	7	6	5	4	3	2	1	0	
Byte 0	0	0	0	0	1	0	0	0	08H Read
Byte 0	0	0	0	0	1	0	1	0	0AH Write
Byte 1	0	0	0	High Adress/Head					
Byte 2	Middle Address/Cylinder								
Byte 3	Low Address/Sector								
Byte 4	Sector Count								
Byte 5	R	P	D	0	0	0	0	0	

3.3.3.6 Seek Command

This Command initiates a seek to the specified track.

	7	6	5	4	3	2	1	0	
Byte 0	0	0	0	0	1	0	1	1	08H
Byte 1	0	0	0	High Address/Head					
Byte 2	Middle Address/Cylinder								
Byte 3	Low Address/Don't care								
Byte 4	x	x	x	x	x	x	x	x	
Byte 5	R	P	0	0	0	0	0	0	

3.3.3.7 Initialize Drive Characteristics

This command is used to configure the controller to work with a certain Drive Type. After the command is send, the controller expects an 8 byte block of data as listed below.

	7	6	5	4	3	2	1	0	
Byte 0	0	0	0	0	1	1	0	0	0CH
Byte 1	0	0	0	x	x	x	x	x	
Byte 2	x	x	x	x	x	x	x	x	
Byte 3	x	x	x	x	x	x	x	x	
Byte 4	x	x	x	x	x	x	x	x	
Byte 5	x	x	x	x	x	x	x	x	

DATA	7	6	5	4	3	2	1	0	Default	
Byte 0	c	c	c	c	c	c	c	c	48H	c= Number of Cyl.
Byte 1	0	0	r	r	t	t	t	t	00H	r= Track Switch Rate 3,6,10,15 ms
Byte 2	t	t	t	t	t	t	t	t	20H	t= Head Load Time(ms)
Byte 3	1	0	0	0	h	h	h	h	82H	h= Number of Heads
Byte 4	m	m	m	m	m	m	m	m	01H	m= MSB Bytes/Sector
Byte 5	l	l	l	l	l	l	l	l	00H	l= LSB Bytes/Sector
Byte 6	s	s	s	s	s	s	s	s	1AH	s= Sectors/Track
Byte 7	f	f	0	0	0	0	0	0	40H	f= Recording Format 00=FM,01=MFM(Tr.1-N) 11= MFM

3.3.3.8 Copy Commands

These Commands can be used to copy data directly from/to another SCSI Controller on the same bus. There is no status return after this command. Status may be obtained by executing the Request Sense Status Command.
First issue the Copy Command, then issue the Write or Read Commmand to the other controller. As soon as the other controller goes to data mode the data is transferred. The transfer stops when the other controller goes to result phase.

	7	6	5	4	3	2	1	0		
Byte 0	1	1	0	0	0	0	0	1	C1H	Copy From Flex.Disc
Byte 0	1	1	0	0	0	0	1	0	C2H	Copy To Flex. Disc
Byte 1	0	0	0	High Address/Head						
Byte 2	Middle Address/Cylinder									
Byte 3	Low Address/Sector									
Byte 4	Sector Count									
Byte 5	R	P	D	0	0	0	0	0		

3.3.3.9 Diagnostic Commands

The RAM Diagnostic performs a data pattern test of the RAM Buffer.

The Drive Diagnostic performs a test of the Drive and Drive Interface. The controller sends recalibrate and seek commands and verifies sector 0 of all the tracks.

The Controller Internal Diagnostics performs a self-test of the controller(Processor,Buffers,ROM and ECC circuitry)

	7	6	5	4	3	2	1	0		
Byte 0	1	1	1	0	0	0	0	0	E0H	RAM Diagnostic
Byte 0	1	1	1	0	0	0	1	1	E3H	Drive Diagnostic
Byte 0	1	1	1	0	0	1	0	0	E4H	Controller Diagnostic
Byte 1	0	0	0	x	x	x	x	x		
Byte 2	x	x	x	x	x	x	x	x		
Byte 3	x	x	x	x	x	x	x	x		
Byte 4	x	x	x	x	x	x	x	x		
Byte 5	R	x	x	x	x	x	x	x		

3.3.4 STREAMER TAPE COMMANDS (TAPCO)

The commands in this section are used to access the ARCHIVE Streamer Tape used as Backup Medium for P3800 or the P3013 Backup Option of P3500.

All commands are formed by a six-byte control block as follows:

	7	6	5	4	3	2	1	0
Byte 0	Cmd Class			Opcode				
Byte 1	LUN							
Byte 2				Block Count(High)				
Byte 3	Block Count (Medium)							
Byte 4	Block Count (Low)							
Byte 5	Control Field							

LUN is the Drive Number (Only Unit 0 and 1 accepted)

Byte 2,3 and 4 specify a 21-bit Number of Blocks

Byte 5 allows for the selection of several options as follows:

	7	6	5	4	3	2	1	0	
Byte 5	p	f	0	0	x	x	x	x	-- Not Used

f:
- 1 -- During Write: A File Mark Block is appended to the last block
- 1 -- During Read : Continue reading independent of File Mark Blocks

p:
- 0 -- Stop tape after command for further access
- 1 -- Go to Begin of Tape after command execution

At the end of a command the controller returns the next two bytes:

	7	6	5	4	3	2	1	0
Byte 0	0	0	d	0	0	c	e	0
Byte 1	0	0	0	0	0	0	0	0

d = drive number
e = 1: Error Occurred; Issue Request Command
c = 1: More then 8 retries needed

COMMAND SUMMARY STREAMER

CODE	FUNCTION
00	Test Drive Ready
01	Rewind
02	Retension
03	Request Sense Status
04	Format Drive
05	Check Track Format
06	Request Drive Status
08	Read
09	Fill
0A	Write
10	Write File Mark
11	Space
13	Verify
19	Erase
C8	Restore
CA	Backup
E0	RAM Diagnostic
E1	Send FW Revision
E3	Drive Diagnostic
E4	Controller Diagnostic

3.3.4.1 Test Unit Ready

This command selects the drive and verifies that the drive is ready.

	7	6	5	4	3	2	1	0	
Byte 0	0	0	0	0	0	0	0	0	00H
Byte 1	0	0	d	x	x	x	x	x	
Byte 2	x	x	x	x	x	x	x	x	
Byte 3	x	x	x	x	x	x	x	x	
Byte 4	x	x	x	x	x	x	x	x	
Byte 5	x	x	x	x	x	x	x	x	

3.3.4.2 Rewind/Retension/Erase

The Rewind command moves the tape to "Begin Of Tape"(BOT).

The Retension command moves the tape to "Begin Of Tape"(BOT), then moves to "End of Tape" and from EOT back to BOT.

The Erase Command moves the selected drive to BOT. Then the Tape will be completely erased and rewinded to BOT.

	7	6	5	4	3	2	1	0	
Byte 0	0	0	0	0	0	0	0	1	01H Rewind
	0	0	0	0	0	0	1	0	02H Retension
	0	0	0	1	1	0	0	1	19H Erase
Byte 1	0	0	d	x	x	x	x	x	
Byte 2	x	x	x	x	x	x	x	x	
Byte 3	x	x	x	x	x	x	x	x	
Byte 4	x	x	x	x	x	x	x	x	
Byte 5	x	x	x	x	x	x	x	x	

Status Information is immediately returned after receiving the command. Further commands are rejected untill the operation is finished. Possible error information is returned at the next command. In case of Bus Arbitration is used the bus is released after receiving the command and status is made available after a SCSI Reselection phase.

3.3.4.3 Request Sense Status

This command must be issued immediately after an error is detected. The controller returns four bytes of drive and controller status.

	7	6	5	4	3	2	1	0	
Byte 0	0	0	0	0	0	0	1	1	03H
Byte 1	0	0	d	x	x	x	x	x	
Byte 2	x	x	x	x	x	x	x	x	
Byte 3	x	x	x	x	x	x	x	x	
Byte 4	x	x	x	x	x	x	x	x	
Byte 5	x	x	x	x	x	x	x	x	

The next status bytes are returned at the DMA Address:

	7	6	5	4	3	2	1	0
Byte 0	v	Error Code						
Byte 1	0	0	d	Remining Blocks(H)				
Byte 2	Remaining Blocks(M)							
Byte 3	Remaining Blocks(L)							

Byte 0 (bit 7) indicates if the address in the next 3 bytes is valid.

List of Error Codes

00	80	No Error
04	84	Drive Not Ready
09	89	Media Not Loaded
0D	8D	End of Media
11	91	Uncorrectable Data Error
17	97	Write Protected
18	98	Correctable Data Error
1C	9C	Bad Block Not Located
1E	9E	No Data Detected
1F	9F	Controller Error
20	A0	Invalid Command
22	A2	File Mark Found
23	A3	Command Rejected
30	B0	Ram Diagnostic Failure
31	B1	Rom Checksum Error
34	B4	DMA Diagnostic Failure
35	B5	Drive Error

3.3.4.4 Request Drive Status

This command causes the controller to send six bytes of drive status to the DMA Address.

	7	6	5	4	3	2	1	0	
Byte 0	0	0	0	0	0	1	1	0	06H
Byte 1	0	0	d	x	x	x	x	x	
Byte 2	x	x	x	x	x	x	x	x	
Byte 3	x	x	x	x	x	x	x	x	
Byte 4	x	x	x	x	x	x	x	x	
Byte 5	x	x	x	x	x	x	x	x	

The next status Bytes are returned:

	7	6	5	4	3	2	1	0	
Byte 0	Tape Drive Status 0								Error Class
Byte 1	Tape Drive Status 1								Error Type
Byte 2	Data Error Count (High)								Write: Number of Rewritten Blocks
Byte 3	Data Error Count (Low)								Read .: Number of Read Errors
Byte 4	Underrun Count (High)								Number of Interruptions in Data Flow
Byte 5	Underrun Count (Low)								

3.3.4.5 Read/Write/Fill/Verify Commands

READ reads the specified number of blocks starting from the current Tape position.

The Fill command demands for 512 data bytes(one block). As many blocks as indicated in No. of Blocks will be filled with this data pattern.

The Write Command writes the specified number of Blocks to Tape, starting from the current Tape position.

The Verify Command selects the Tape and will check No. of Blocks from the current Tape position for correct CRC.

	7	6	5	4	3	2	1	0		
Byte 0	0	0	0	0	1	0	0	0	08H	Read
Byte 0	0	0	0	0	1	0	0	1	09H	Fill
Byte 0	0	0	0	0	1	0	1	0	0AH	Write
Byte 0	0	0	0	1	0	0	1	1	13H	Verify
Byte 1	0	0	d	0	0	0	0	0		
Byte 2	0	0	0	No. of Blocks (H)						
Byte 3	No. of Blocks (M)									
Byte 4	No. of Blocks (L)									
Byte 5	p	f	0	0	x	x	x	x		

3.3.4.6 Write File Marks Command

This Command selects the drive and writes No. of File Marks to tape, starting from the current Tape position.

	7	6	5	4	3	2	1	0		
Byte 0	0	0	0	1	0	0	0	0	10H	Write File Marks
Byte 1	0	0	d	0	0	0	0	0		
Byte 2	0	0	0	0	0	0	0	0		
Byte 3	0	0	0	0	0	0	0	0		
Byte 4	No. of File Marks									
Byte 5	x	x	x	x	x	x	x	x		

3.3.4.7 Space Command

This command is used to move the Tape in the direction from BOT to EOT. The "code" field defines how the Space command is used.
Code 00 moves as many blocks as indicated n "count", untill a File Mark is Found. Code 01 skips as many File Marks as indicated in "Count". Code 11 moves the tape behind the last block.

	7	6	5	4	3	2	1	0	
Byte 0	0	0	0	1	0	0	0	1	11H Space
Byte 1	0	0	d	0	0	0	c	c	cc=00 : Skip blocks cc=01 : Skip File Marks
Byte 2	0	0	0	Count (High)					cc=11 : End of Data
Byte 3	Count (Medium)								
Byte 4	Count (Low)								
Byte 5	x	x	x	x	x	x	x	x	

3.3.4.8 Backup/Restore Commands

These commands provide for transfers between this controller and another controller which is also connected to the SCSI Bus. The Backup command copies to Tape, the Restore command copies from tape.
After having received the command the bus is immediately released by sending the status information. This allows the system to supply a Read/Write Command to the other controller,e.g. disc.
The Tape Controller remains active and observes the SCSI Bus for Data Requests. If so, the controller will handle the data rather then the Host Processor.
The command is terminated if either the No. of Blocks are transferred or the Host aborts the command by issueing a Request Sense or Request Drive Command.

	7	6	5	4	3	2	1	0	
Byte 0	1	1	0	0	1	0	0	0	0C8H Restore
	1	1	0	0	1	0	1	0	0CAH Backup
Byte 1	0	0	d	0	0	0	0	0	
Byte 2	0	0	0	No. of Blocks (H)					
Byte 3	No. of Blocks (M)								
Byte 4	No. of Blocks (L)								
Byte 5	0	f	0	0	x	x	x	x	

To get the status information about these commands a Request Sense or Request Drive Status must be issued.

3.3.4.9 Diagnostic Commands

The RAM Diagnostic performs a data pattern test of the RAM Buffer.

The Drive Diagnostic performs a test of the Drive and Drive Interface. The controller sends recalibrate and seek commands and verify sector 0 of all the tracks.

The Controller Internal Diagnostics performs a self-test of the controller(Processor,Buffers,ROM and ECC circuitry)

The Send FW Revision command is used to obtain the current Firmware Revision Number of the Tape Controller (0-F).
The next data byte is send to the Host for this command.

7	6	5	4	3	2	1	0	
f	f	f	f	0	0	1	1	f= Revision number

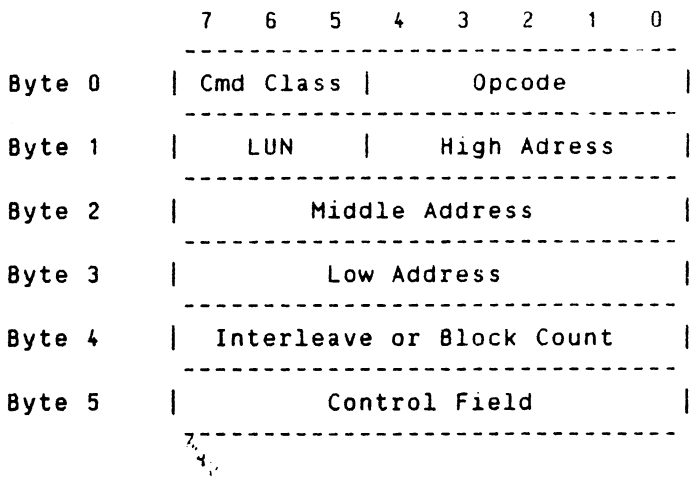
The CDB for this Commands is structured as follows:

	7	6	5	4	3	2	1	0	
Byte 0	1	1	1	0	0	0	0	0	E0H RAM Diagnostic
Byte 0	1	1	1	0	0	0	0	1	E1H Send FW Revision
Byte 0	1	1	1	0	0	0	1	1	E3H Drive Diagnostic
Byte 0	1	1	1	0	0	1	0	0	E4H Controller Diagnostic
Byte 1	0	0	0	x	x	x	x	x	
Byte 2	x	x	x	x	x	x	x	x	
Byte 3	x	x	x	x	x	x	x	x	
Byte 4	x	x	x	x	x	x	x	x	
Byte 5	x	x	x	x	x	x	x	x	

3.3.5 Fixed Disc Commands PRIAM (FIXCO 8)

The commands in this section are used to access the PRIAM Fixed Disc (60M) of the P3800 System.

All commands are formed by a six-byte control block as follows



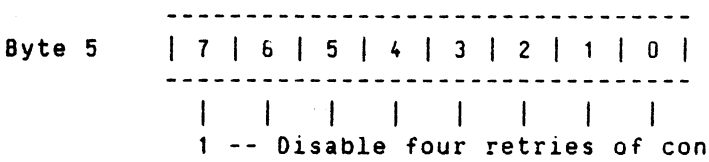
LUN is the Drive Number (Only Unit 0 and 1 are accepted)

Byte 1,2 and 3 specify a 21-bit logical data address, calculated as follows:

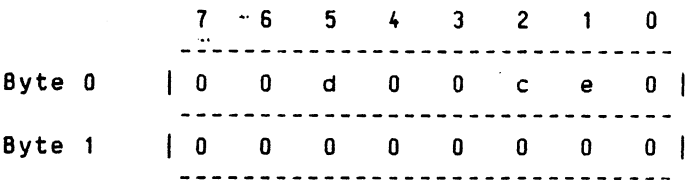
Logical Address=(CYADR*HDCYL+HDADR)*SETRK+SEADR

Where: CYADR = Cylinder Address
HDADR = Head Address
SEADR = Sector Address
HDCYL = Number of Heads/Cylinder
SETRK = Number of Sectors/Track

Byte 5 allows for the selection of several options as follows:



At the end of a command the controller returns the next two status bytes:



d = drive number
c = CRC Error has been corrected succesfully
e = error occurred during command, use Request Sense command to obtain more information.

COMMAND SUMMARY PRIAM FXD

CODE	FUNCTION
00	Test Drive Ready
01	Recalibrate
03	Request Sense Status
04	Format Drive
05	Check Track Format
06	Format Track
07	Format Bad Track
08	Read
0A	Write
E5	Read Long
E6	Write Long
0B	Seek
0C	Initialize Drive Charateristics
0D	Read ECC Error Burst
E0	RAM Diagnostic
E3	Drive Diagnostic
E4	Controller Diagnostic

3.3.5.1 Test Drive Ready

This command selects the drive and verifies that the drive is ready. If the motor is off the drive spindle motor is started and the controller waits 30 seconds for the maximum motor start time.

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	0	0	0
Byte 1	0	0	d	x	x	x	x	x
Byte 2	x	x	x	x	x	x	x	x
Byte 3	x	x	x	x	x	x	x	x
Byte 4	x	x	x	x	x	x	x	x
Byte 5	x	x	x	x	x	x	x	x

3.3.5.2 Recalibrate

This command positions the head to cylinder 0.

	7	6	5	4	3	2	1	0	
Byte 0	0	0	0	0	0	0	0	1	01H
Byte 1	0	0	d	x	x	x	x	x	
Byte 2	x	x	x	x	x	x	x	x	
Byte 3	x	x	x	x	x	x	x	x	
Byte 4	x	x	x	x	x	x	x	x	
Byte 5	r	0	0	0	x	x	x	x	

3.3.5.3 Request Sense Status

This command must be issued immediately after an error is detected. The controller reurns four bytes of drive and controller status, belonging to the previous command.

	7	6	5	4	3	2	1	0	
Byte 0	0	0	0	0	0	0	1	1	03H
Byte 1	0	0	d	x	x	x	x	x	
Byte 2	x	x	x	x	x	x	x	x	
Byte 3	x	x	x	x	x	x	x	x	
Byte 4	x	x	x	x	x	x	x	x	
Byte 5	x	x	x	x	x	x	x	x	

The next status bytes are returned at the DMA Address:

	7	6	5	4	3	2	1	0
Byte 0	av	Error Code						
Byte 1	0	0	d	High Adress				
Byte 2	Middle Address							
Byte 3	Low Address							

Byte 0(bit 7) indicates if the address in the next 3 bytes is valid.

List of Error Codes

00	80	No Error
04	84	Drive Not Ready
0F	8F	Controller Reset
10	90	ID Read Error
11	91	Uncorrectable Data Error
13	93	Data Address Mark Not Found
14	94	Sector Not Found
15	95	Seek Error
17	97	Write Protected
18	98	Correctable Data Error
1C	9C	Defective Track
1D	9D	Wrong Head
1E	9E	No ID Synchronization
1F	9F	Controller Error
20	A0	Invalid Command
21	A1	Illegal Disk Address
30	B0	RAM Diagnostic Failure
31	B1	ROM Checksum Error
32	B2	ECC Diagnostic Failure
34	B4	Interface Error at Device Connector
35	B5	Drive Error

3.3.5.4 Identifier Commands

Format Identifiers Writes and Checks Number of sectors of a Track with ID information , from the start address in the command.
Format Defective Track marks the addressed track as defective (Flag/Head field=2).
Read Identifiers reads the ID Information from the specified disk address to the DMA Address.

	7	6	5	4	3	2	1	0	
Byte 0	1	1	0	0	0	1	0	1	C5H Read Identifiers
Byte 0	1	1	0	0	0	1	1	0	C6H Format Identifiers
Byte 0	1	1	0	0	0	1	1	1	C7H Format Defective Track
Byte 1	0	0	d	High Adress					
Byte 2	Middle Address								
Byte 3	Low Address								
Byte 4	Number of Sectors/Track								x for Read Identifiers
Byte 5	x	0	0	0	x	x	x	x	

SECTOR LAYOUT

Number	Value	Function	Supplied by Host/Controller
23	00	Preamble	Controller
1	FB	Sync Byte	Controller
4	00	Sync Extension	Host
3	xx	Sector Number (3x)	Host
3	xx	Flag/Head Number (3x)	Host
3	xx	Cylinder Number High(3x)	Host
3	xx	Cylinder Number Low (3x)	Host
4	xx	ID CRC	Controller
2	00	Postamble	Controller
1	FF	Gap 1	Controller
11	00	Preamble	Controller
1	FB	Sync Byte	Controller
N	xx	Data	Host
4	xx	Data CRC	Controller
2	00	Postamble	Controller
1	00	Gap 2	Controller

The 16 bytes of ID Information to be supplied by the host are requested by the controller before execution of the format command.

The Read ID command transfers for every sector 24 bytes to the system, being these 16 bytes, followed by the ID CRC and 4 Dummy bytes.

3.3.5.5 Read/Write Commands

The Read Command reads the specified number of sectors of a track starting with the address in the command block.
The Write Command writes the specified number of sectors of a track to the Disc,starting with the Disc Address in the command block.
There must not be any Head or Cylinder change during command execution.

	7	6	5	4	3	2	1	0	
Byte 0	0	0	0	0	1	0	0	0	08H Read
Byte 0	0	0	0	0	1	0	1	0	0AH Write
Byte 1	0	0	d	High Adress					
Byte 2	Middle Address								
Byte 3	Low Address								
Byte 4	Block Count								
Byte 5	r	0	0	0	x	x	x	x	

3.3.5.6 Seek Command

This Command initiates a seek to the specified track.

	7	6	5	4	3	2	1	0	
Byte 0	0	0	0	0	1	0	1	1	0BH Seek
Byte 1	0	0	d	High Adress					
Byte 2	Middle Address								
Byte 3	Low Address								
Byte 4	x	x	x	x	x	x	x	x	
Byte 5	r	0	0	0	x	x	x	x	

3.3.5.7 Initialize Drive Characteristics

The Initialize command is used to configure the controller to work with a certain Drive Type. After the command is sent, the controller expects an 8 byte block of data as listed below.
The Send Drive Characteristics Command asks the controller to send some bytes of Drive information to the system.

	7	6	5	4	3	2	1	0	
Byte 0	0	0	0	0	1	1	0	0	0CH Initialize
Byte 0	1	1	0	0	0	0	1	0	C2H Send Drive Characteristics
Byte 1	x	x	x	x	x	x	x	x	
Byte 2	x	x	x	x	x	x	x	x	
Byte 3	x	x	x	x	x	x	x	x	
Byte 4	x	x	x	x	x	x	x	x	
Byte 5	x	x	x	x	x	x	x	x	

INITIALIZATION DATA

	7	6	5	4	3	2	1	0	
Byte 0-6	To Be Fixed								
Byte 7	0	0	0	0	e	e	e	e	e= Maximum ECC data burst length (08H Default)

DRIVE DATA

Byte 0 : Drive ID (04H=DISKOS 3450, 05H=DISKOS 7050)
Byte 1 : Bytes/Sector High
Byte 2 : Bytes/Sector Low

Bytes/Sector	Bytes/Datafield	Sectors/Track
01 46	256	41
02 46	512	23
04 5D	1024	12

3.3.5.8 Read Bad Spot Info

This Command Reads a table of 8 Bytes from the addressed track, containing the byte position relative to index of up to three bad spots on the track.

	7	6	5	4	3	2	1	0	
Byte 0	1	1	0	0	0	1	0	0	C4H Read Bad Spot Info
Byte 1	0	0	d	High Adress					
Byte 2	Middle Address								
Byte 3	Low Address								
Byte 4	x	x	x	x	x	x	x	x	
Byte 5	x	0	0	0	x	x	x	x	

BAD SPOT INFO

Byte 0 : Defect 1 Position High
Byte 1 : Defect 1 Position Low
Byte 2 : Defect 2 Position High
Byte 3 : Defect 2 Position Low
Byte 4 : Defect 3 Position High
Byte 5 : Defect 3 Position Low
Byte 6 : Checksum Byte 0-7 High
Byte 7 : Checksum Byte 0-7 Low

The table is read correctly if the sum of this four words equals zero.

3.3.5.9 Motor Off

This command forces a "Seuence Down" procedure (position to landing zone and stop spindle motor) at the selected drive.

	7	6	5	4	3	2	1	0	
Byte 0	1	1	0	0	1	0	0	1	C9H Motor Off
Byte 1	0	0	d	x	x	x	x	x	
Byte 2	x	x	x	x	x	x	x	x	
Byte 3	x	x	x	x	x	x	x	x	
Byte 4	x	x	x	x	x	x	x	x	
Byte 5	x	x	x	x	x	x	x	x	

3.3.5.10 Diagnostic Commands

The Drive Diagnostic performs a test of the Drive and Drive Interface. The controller sends recalibrate and seek commands and verify sector 0 of all the tracks.
The Controller Diagnostics performs a self-test of the controller (Processor,Buffers,ROM and ECC circuitry)
The Send FW Revision Command sends the firmware level of the controller to the system (Value X1, X=Revision 0-F).
The Read Test CRC performs a read without data transfer.

	7	6	5	4	3	2	1	0		
Byte 0	1	1	1	0	0	0	0	1	E1H	Send FW Revision
Byte 0	1	1	1	0	0	0	1	0	E2H	Test Controller/Drive
Byte 0	1	1	1	0	0	0	1	1	E3H	Test Drive
Byte 0	1	1	1	0	0	1	0	0	E4H	Test Controller
Byte 0	1	1	1	0	0	1	1	1	E7H	Read Test CRC
Byte 1	0	0	d	x	x	x	x	x		
Byte 2	x	x	x	x	x	x	x	x		
Byte 3	x	x	x	x	x	x	x	x		
Byte 4	x	x	x	x	x	x	x	x		
Byte 5	x	x	x	x	x	x	x	x		

4 PROCESSOR PMU 186

4.1 80186 MICROPROCESSOR

For a description of the instruction set as well as all other relevant information refer to:
Intel's IAPX 86/88,186/188 User's Manual.

4.1.1 Timing

The frequency applied to the microprocessor is 16 MHz.
The processor clock is 8 MHz.

The next timing states are required:

- Local Memory Access Fetch : 4 clock cycles
  Read : 4 clock cycles
  Write : 4 clock cycles
- I/O Access : 7 clock cycles (incl. wait states)
- Interrupt Acknowledge : 7 clock cycles (incl. wait states)

For System Bus Access additional clock cycles are required due to bus arbitration.

4.1.2 Interrupt system

The interrupt handling is done by the integrated interrupt controller of the 80186. For a detailed description can be referred to the data sheets. However in section 4.3.1.5 all of the internal registers are shown and the default value is given (if possible).

The interrupt controller is operating in NON-IRMX mode and the cascade mode is selected.
The INT0/INTA0 lines are connected to the SCC while INT1/INTA1 are connected to the PIC.

The interrupt priority (high to low) is:

Interrupt	Source
NMI	Time Out/Hand Held Panel
INT0	SCC Channel A SCC Channel B
INT1	PIC Power Failure Line PIC Networking Fifo PIC Networking Control Port PIC Planned Power Off PIC SCSI Port PIC reserved PIC reserved PIC Flexible Disc Controller
IRT2	Counter/Timer 2 (Internal)

4.2 MEMORY SYSTEM

4.2.1 Local and System memory

The local memory on a PMU186 board consists of:

- 16 k8 ROM

- 160 or 256 k8 RAM

A master can also access the system memory. This is formed by 16 pages. Each page is 64 k8 wide and is located on another slave processor board.

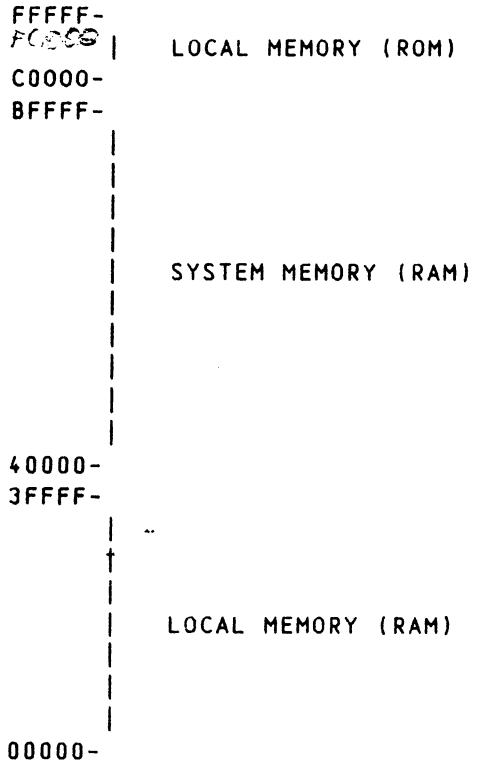
2.2 Memory Mapping

The PMU186 supports two different memory mapping schemes.
The version is indicated by a strap.

4.2.2.1 Version A

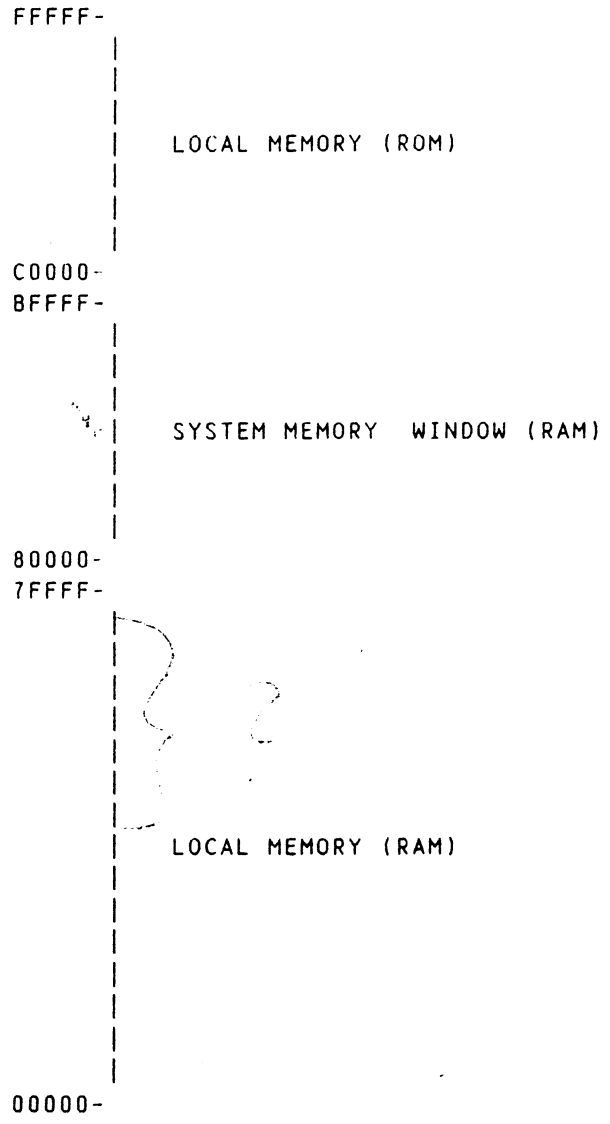
- 256 k8 mapped to local memory (RAM).
- up to 752 k8 mapped to memory on the EMM-bus (RAM). } 1 MByte
- minimal 16 k8 mapped to local memory (ROM).

The memory address space on the EMM-bus is a 1:1 mapping of the local address area.



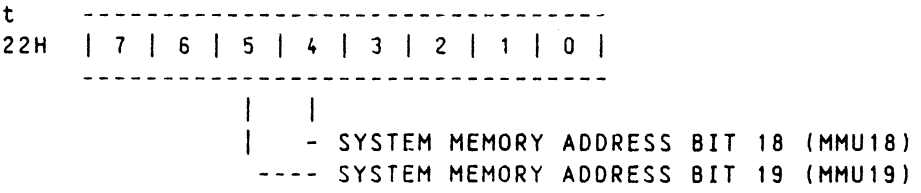
4.2.2.2 Version B

- 512 k8 local memory (RAM).
- 256 k8 window to access 1 M8 system memory (RAM).
- 256 k8 local memory (ROM).

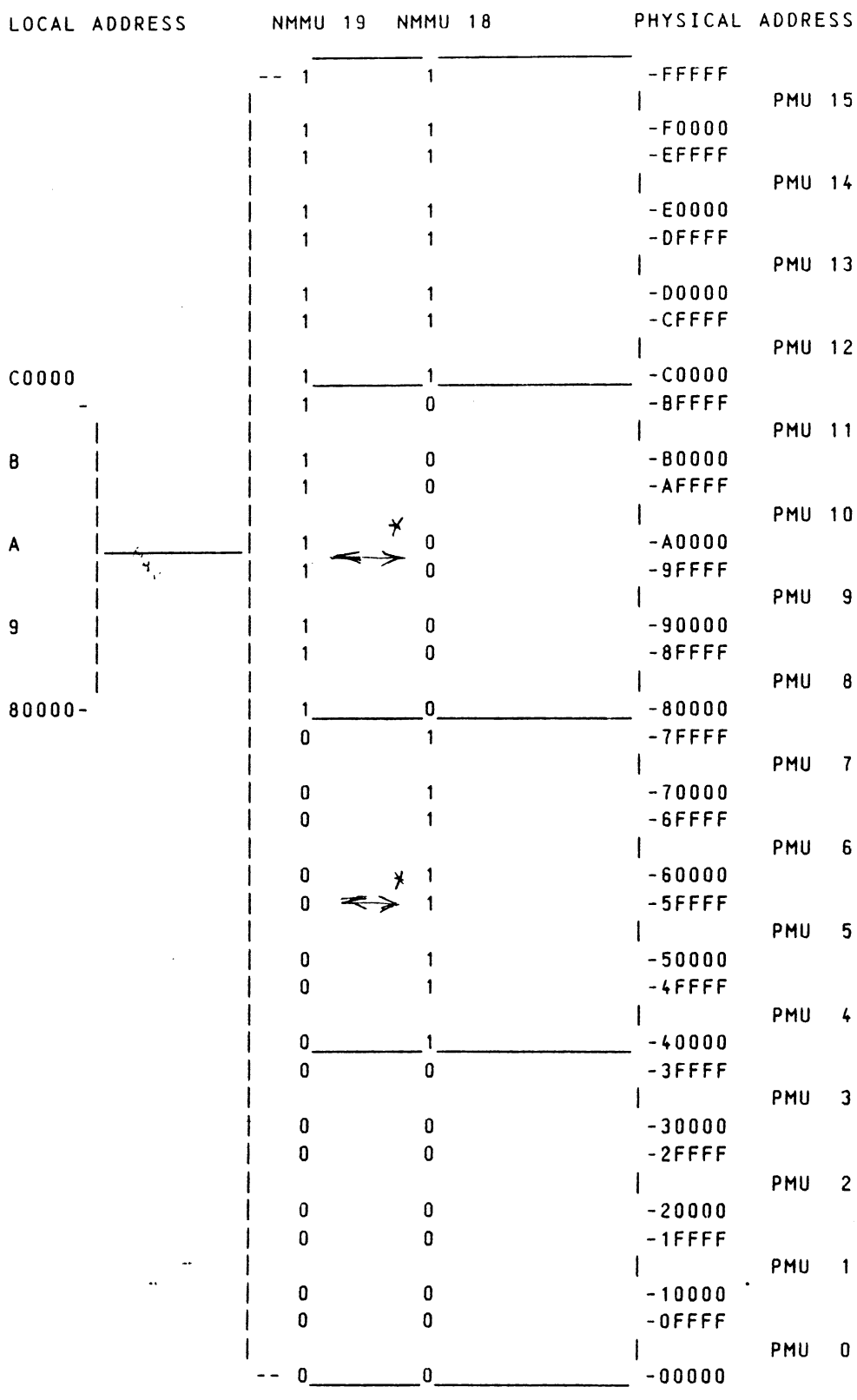


4.2.2.3 System Memory Mapping

When the processor is adressing the system memory window then the local memory address is translated into a system memory address. For this purpose two bits of output port 22H are used.



The lines NMMU 19 and NMMU 18 become the two most significant bits of the 20 bits system memory address.

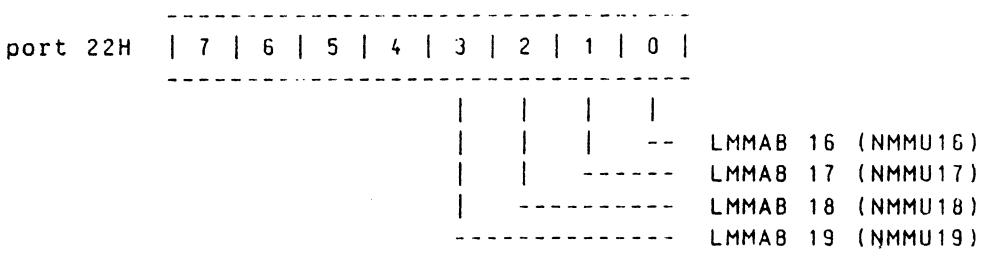


* Die Werte müssen genau umgekehrt sein

4.2.2.4 Local Memory Mapping

Each processor board has a page of 64 kB in the system memory. The local address area of the PMU 186 is however 1 MB. By means of 4 bits of output port 22H the local processor can indicate on which part of the local memory the system memory page must be mapped.

Output

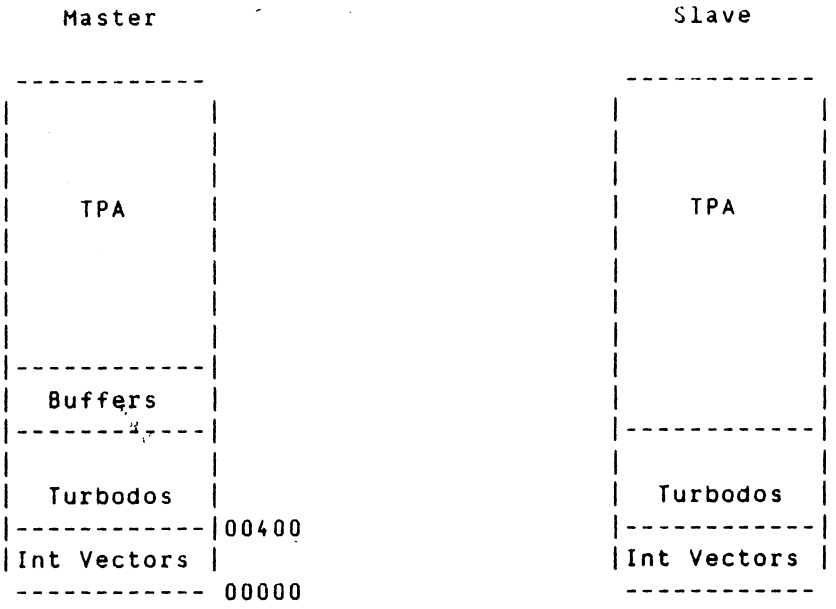


LMMAB = LOCAL MEMORY MAP ADDRESS BIT

The four most significant bits of the system memory address, which hold the PMU number, are replaced on the accessed processor board by the lines LMMAB 19-16.
These lines are the most significant four local addresslines.

4.2.3 Memory Layout

4.2.3.1 Turbodos Memory Occupation



4.2.3.2 System Memory Area

A number of system dependent parameters are stored in the interrupt vector area (00000-00402). This section will list these parameters.

```
0000DH          IPLFLG      :IPL/Power off flags

0004C-0004FH    RTCIV       :real time clock isr

000A3H          CONP2A      :copy of control port 2 (22H)
000A4H          CONP3A      :copy of control port 3 (28H)
000A5H          CONP4A      :copy of control port 4 (2AH)
000A6H          SASCP2      :copy of SASI control port 2
000A7H          CONCHA      :copy of Turbodos console assignment channel
000A8H          LAMPS       :copy of lampsfield

00120-00123H    PFLIV       :power failure isr
00124-00127H    FIFOIV      :fifo isr
00128-0012BH    MSCIV       :master slave control isr
0012C-0012FH    TOFIV       :terminal off isr
00130-00133H    SASIV       :SASI port (SCSI) isr
00134-00137H    reserved
00138-0013BH    reserved
0013C-0013FH    FDCIV       :flexible disc controller isr

* 00140-00143H  SBTIV       :SCC Channel B transmit buffer empty isr
  00144-00147H  SBEIV       :SCC Channel B external status isr
  00148-0014BH  SBRIV       :SCC Channel B received character isr
  0014C-0014FH  SBSIV       :SCC Channel B special condition isr
  00150-00153H  SATIV       :SCC Channel A transmit buffer empty isr
  00154-00157H  SAEIV       :SCC Channel A external status isr
  00158-0015BH  SARIV       :SCC Channel A received character isr
  0015C-0015FH  SASIV       :SCC Channel A special condition isr
```

4.2.3.3 Memory Layout TurboDOS

The base page is the 256-byte memory region from DS:0000 to DS:00FF. The base page is initialized by turbodos whenever a transient program is loaded, and is used for communication between TURBODOS and the transient program.

0000-0002H	Length of Code group (LSB first).
0003-0004H	Base address Code group.
0005H	8080 model flag (set if 8080 model).
0006-0008H	Length of Data group (LSB first).
0009-000AH	Base address Data group.
0008H	not used.
000C-000EH	Length of Extra group (LSB first).
000F-0010H	Base address of Extra group.
0011H	not used.
0012-0014H	Length of Stack group (LSB first).
0015-0016H	Base address of Stack group.
0017H	not used.
0018-001AH	Length of Auxiliary-1 group (LSB first).
0018-001CH	Base address of Auxiliary-1 group.
001DH	not used.
001E-0020H	Length of Auxiliary-2 group (LSB first).
0021-0022H	Base address of Auxiliary-2 group.
0023H	not used.
0024-0026H	Length of Auxiliary-3 group (LSB first).
0027-0028H	Base address of Auxiliary-3 group.
0029H	not used.
002A-002CH	Length of Auxiliary-4 group (LSB first).
002D-002EH	Base address of Auxiliary-4 group.
002F-0058H	not used.
005C-006BH	Default file control block (part 1).
006C-007BH	Default file control block (part 2).
007CH	Default file control block current record.
007D-007FH	Default file control block random record.
0080-00FFH	Default 128-byte buffer.

4.3 INPUT/OUTPUT SYSTEM

This section gives the programming information for the PMU 186 on HSI-level. First a complete map of the I/O adresses is given. In the following sections each port is described seperately.

The 80186 offers an I/O address area of 64k. Of this complete area only three blocks of 256 addresses each are used.

- block 1 :FF00-FFFFH 80186 integrated peripherals
- block 2 :0100-01FFH reserved
- block 3 :0000-00FFH local and system I/O area

Block 3 can be subdivided in:

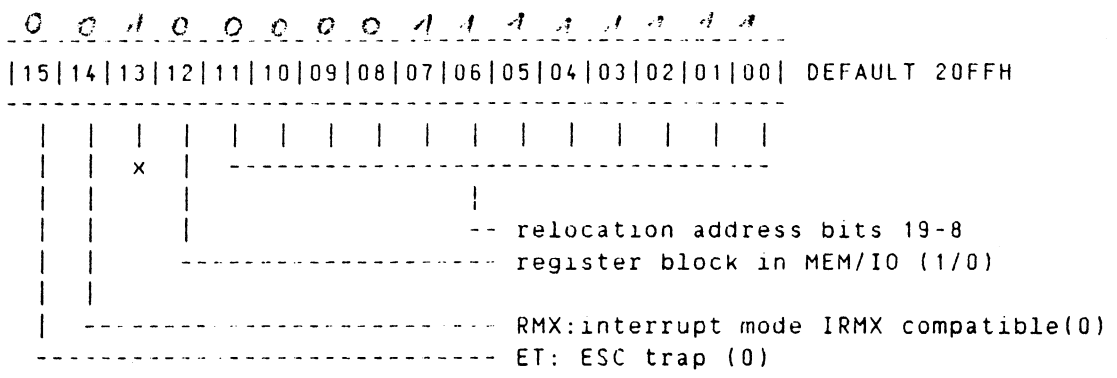
- local I/O area (local CPU) :0000-003FH
- system I/O area part 1 (PMU 0,PMU 1-15) :0040-005FH
- system I/O area part 2 (PMU 0) :0060-00FFH

4.3.1 80186 Integrated Peripherals

Port nr	Assignment
FFFEH	relocation register
	DMA channel 1
FFDAH	control word
FFD8H	transfer count
FFD6H	destination pointer (most significant 4 bits)
FFD4H	destination pointer
FFD2H	source pointer (most significant 4 bits)
FFD0H	source pointer
	DMA channel 2
FFCAH	control word
FFC8H	transfer count
FFC6H	destination pointer (most significant 4 bits)
FFC4H	destination pointer
FFC2H	source pointer (most significant 4 bits)
FFC0H	source pointer
	Chip select unit
FFA8H	MPCS register
FFA6H	MMCS register
FFA2H	LMCS register
FFA4H	PACS register (not used)
FFA0H	UMCS register
	Timer 2
FF66H	mode/control word
FF64H	not present
FF62H	max count A
FF60H	count register
	Timer 1
FF5EH	mode/control word
FF5CH	max count B
FF5AH	max count A
FF58H	count register
	Timer 0
FF56H	mode/control register
FF54H	max count B
FF52H	max count A
FF50H	count register
	Interrupt controller
FF3AH	control register Timer 2
FF38H	control register Timer 1
FF36H	control register DMA 1
FF34H	control register DMA 2
FF32H	control register Timer 0
FF2EH	interrupt-request register
FF2CH	in-service register
FF2AH	priority-level mask register
FF28H	mask register
FF22H	specific eoi register
FF20H	interrupt vector register

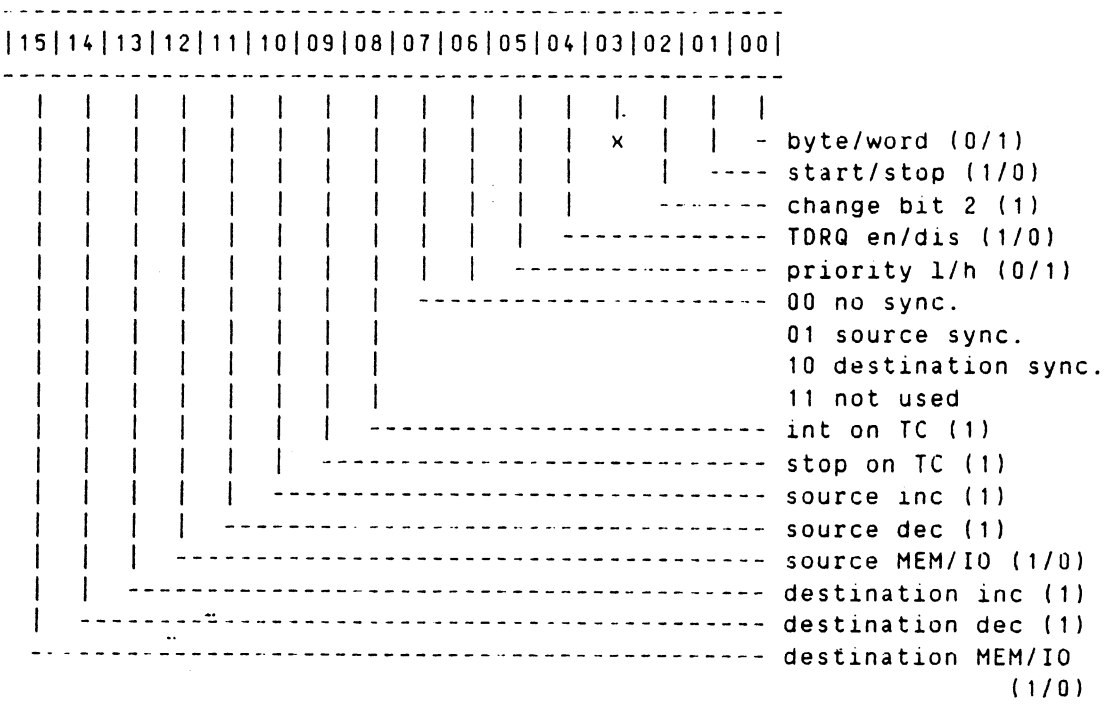
4.3.1.1 80186 Relocation Register

Output Port : FFFEH - relocation register

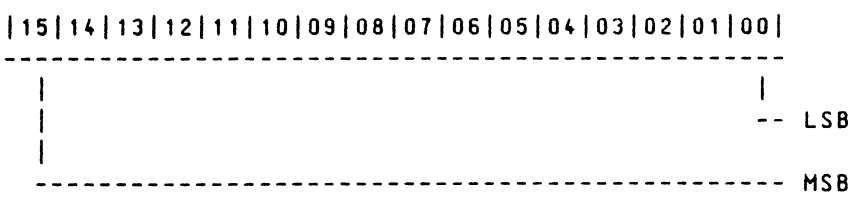


4.3.1.2 80186 DMA Controllers

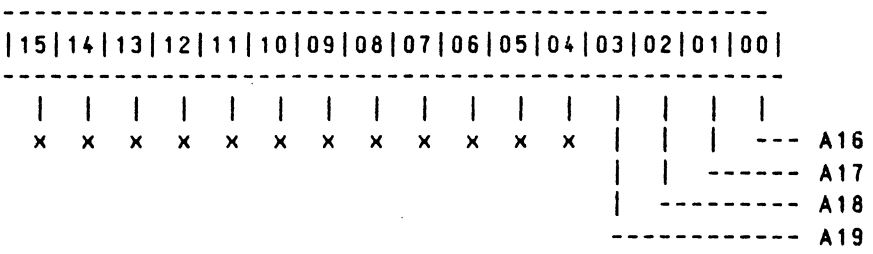
Output Port : FFDAH - control word DMA channel 1
FFCAH - control word DMA channel 2



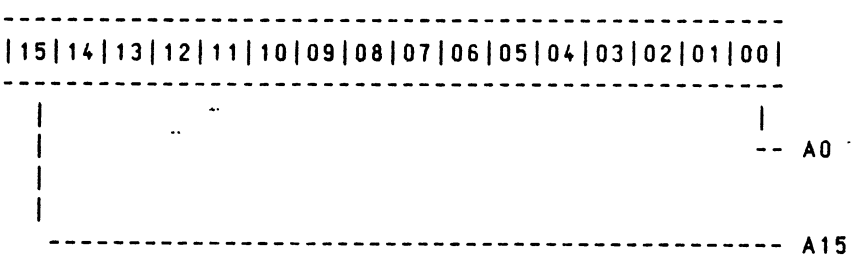
Output Port : FFD8H - transfer count DMA channel 1
FFC8H - transfer count DMA channel 2



Output Port : FFD6H - destination pointer DMA channel 1 (4 bits)
FFD2H - source pointer DMA channel 1 (4 bits)
FFC6H - destination pointer DMA channel 2 (4 bits)
FFC2H - source pointer DMA channel 2 (4 bits)



Output Port : FFD4H - destination pointer DMA channel 1
FFD0H - source pointer DMA channel 1
FFC4H - destination pointer DMA channel 2
FFC0H - source pointer DMA channel 2



4.3.1.3 80186 Memory Chip Select

Output Port : FFA8H - MPCS

```
 1  0  1  0  0  0  0  0  0  0  1  1  1  0  0  0
-----------------------------------------------
|15|14|13|12|11|10|09|08|07|06|05|04|03|02|01|00| DEFAULT A038H
-----------------------------------------------
  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
  1  |  |  |  |  |  |  |  |  |  1  1  1  |  |  -- R0 \
     |  |  |  |  |  |  |  |  |              |  ----- R1  |-  wait states
     |  |  |  |  |  |  |  |  |              |  -------- R2 /
     |  |  |  |  |  |  |  |  |  ------------------------ MS: I/O in I/O area
     |  |  |  |  |  |  |  |  ------------------------- EX: 7/5 pcs lines (1/0)
    M6 M5 M4 M3 M2 M1 M0 -------------------------- Mid-range Memory Size:
```

M6	M5	M4	M3	M2	M1	M0	total block size	individual size	
0	0	0	0	0	0	1	8k	2k	
0	0	0	0	0	1	0	16k	4k	
0	0	0	0	1	0	0	32k	8k	
0	0	0	1	0	0	0	64k	16k	
0	0	1	0	0	0	0	128k	32k	
0	1	0	0	0	0	0	256k	64k	* DEFAULT
1	0	0	0	0	0	0	512k	128k	

Output Port: FFA6H - MMCS Mid-range Memory Chip Select

```
 1  0  0  0  0  0  0  1  1  1  1  1  1  0  0  0
-----------------------------------------------
|15|14|13|12|11|10|09|08|07|06|05|04|03|02|01|00|  DEFAULT 81F8H
-----------------------------------------------
  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
  |  |  |  |  |  |  |  1  1  1  1  1  1  |  |  -- R0 \
  |  |  |  |  |  |  |                    |  ----- R1  | wait states
  |  |  |  |  |  |  |                    |  -------- R2 /
A19 18 17 16 15 14 13 ------------------------- A13-A19 :
```

MSB Address of the mid-range memory block.
Bits A12-A0 always 0.

Output Port : FFA2H - LMCS Lower Memory Chip Select

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	DEFAULT 3FF8H
0	0									1	1	1				--- R0 \
																------ R1 |- wait states
																--------- R2 /
A19	18	17	16	15	14	13	12	11	A10							---------- A10-A19

The Legal Addresses for A10-A19 are shown in the next table:

Upper Address	Memory Block Size	
003FFH	1k	
007FFH	2k	
00FFFH	4k	
01FFFH	8k	
03FFFH	16k	
07FFFH	32k	
0FFFFH	64k	
1FFFFH	128k	
3FFFFH	256k	* DEFAULT

Output Port :FFA0H - UMCS - Upper Memory Chip Select

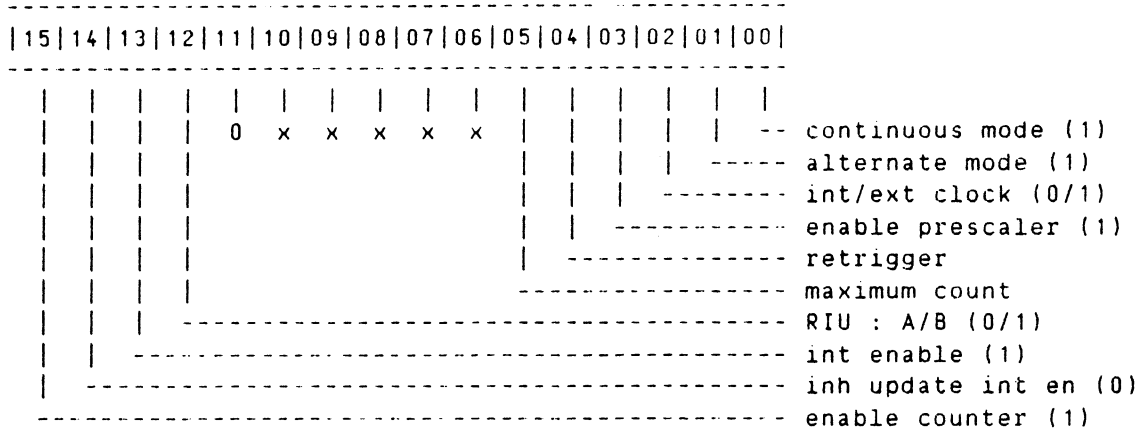
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	DEFAULT FC38H
1	1									1	1	1				--- R0 \
																------ R1 |- wait state
																--------- R2 /
A19	18	17	16	15	14	13	12	11	A10							---------- A10-A19

The legal addresses for A19-A10 are shown in the next table.

starting address	memory size	
FFC00H	1k	
FF800H	2k	
FF000H	4k	
FE000H	8k	
FC000H	16k	* default
F8000H	32k	
F0000H	64k	
E0000H	128k	
C0000H	256k	

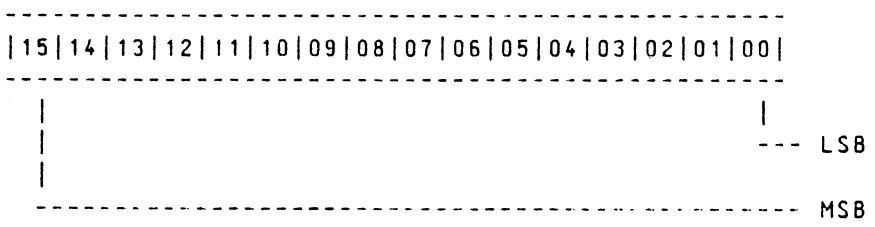
4.3.1.4 80186 Timers

Output Port : FF66H - mode/control word timer 2
FF5EH - mode/control word timer 1
FF56H - mode control word timer 0



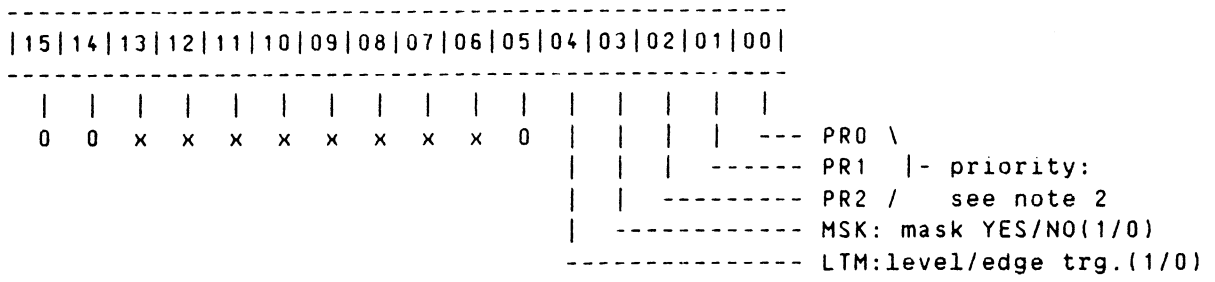
Output Port : FF62H - max count A timer 2
FF5CH - max count B timer 1
FF5AH - max count A timer 1
FF54H - max count B timer 0
FF52H - max count B timer 0

I / O Port : FF60H - current count timer 2
FF58H - current count timer 1
FF50H - current count timer 0



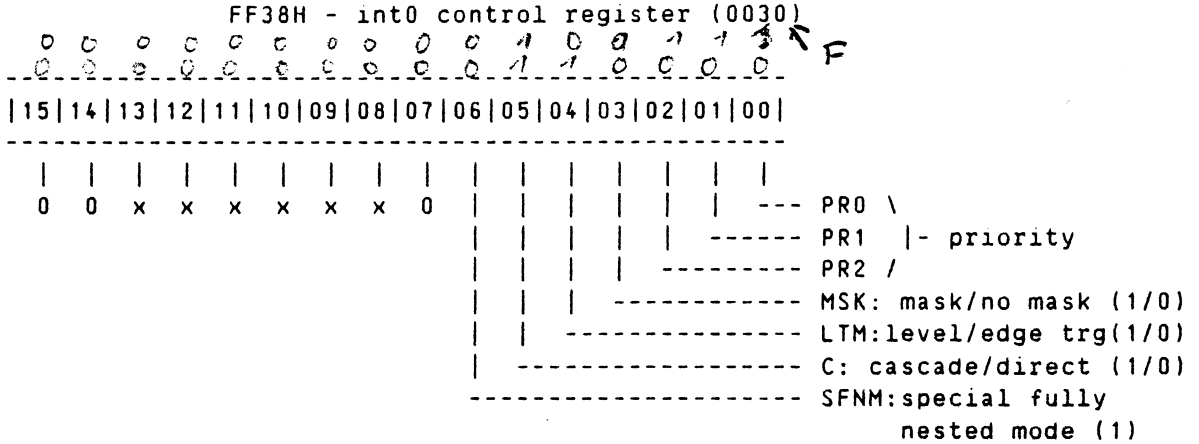
4.3.1.5 80186 Interrupt Control

Output Port : FF3EH - int3 control register (see note 1)
FF3CH - int2 control register (see note 1)



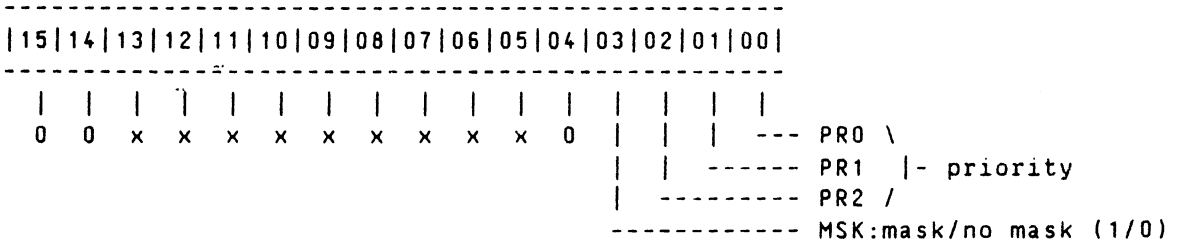
Note 1: in cascade or fully nested mode int3 and int2 are not used.
Note 2: priority levels 000=highest, 111=lowest

Output Port : FF3AH - int1 control register (0027)
FF38H - int0 control register (0030)



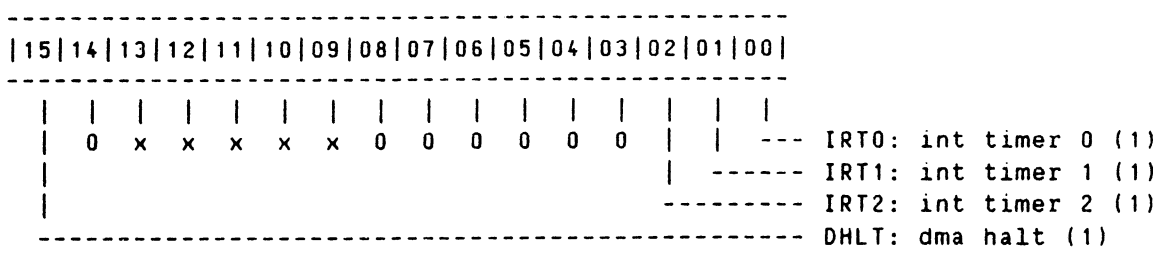
Note : priority levels 000=highest, 111=lowest

Output Port : FF36H : control register DMA 1
FF34H : control register DMA 0
FF32H : control register timer

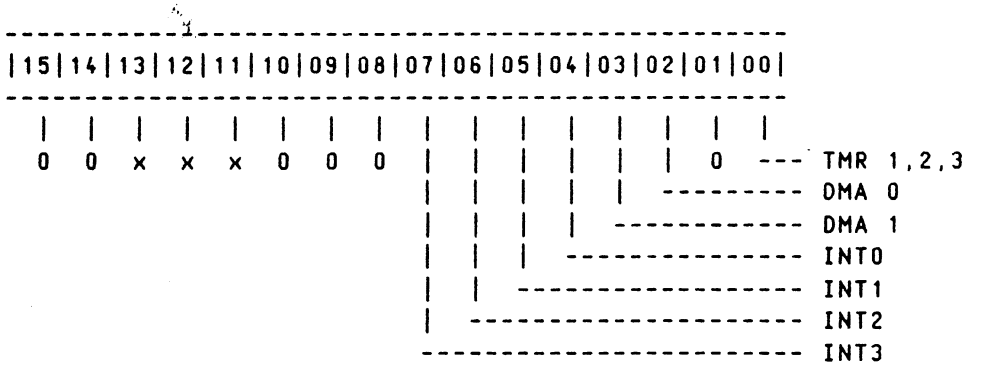


Note : priority levels 000=highest,111=lowest

I / O Port : FF30H : interrupt status register

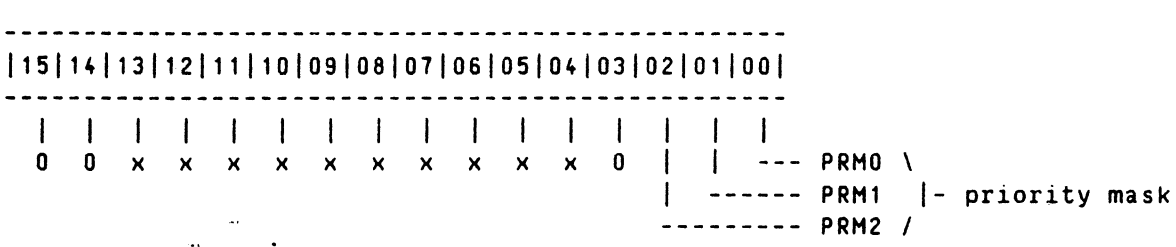


I / O Port : FF2EH - interrupt request register (see note 1)
FF2CH - in-service register (see note 2)
FF28H - mask register (see note 3)



Note 1: 1 means interrupt source has a request. Bits 6-4 are read-only.
Note 2: 1 means interrupt source is being serviced
Note 3: 1 means interrupt source is masked

I / O Port : FF2AH - priority mask register



Note : The code in PRM2-0 inhibits interrupts of lower priority
(lower priority means higher binary value!).

Input Port : FF26H - poll status register
FF24H - poll register

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
x	0	0	x	x	x	x	x	x	x	0	S4	S3	S2	S1	S0	Interrupt Vector (See Table)

Output Port : FF22H - EOI register - end of interrupt register

1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 default 8000

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
	0	0	x	x	x	x	x	x	x	0	S4	S3	S2	S1	S0	Vector Type (See Table)
																EOI command specific Y/N (0/1)

80186 Interrupt Vector Table

Interrupt Name	S4	S3	S2	S1	S0	
divide error	0	0	0	0	0	0
single step	0	0	0	0	1	1
NMI	0	0	0	1	0	2
breakpoint	0	0	0	1	1	3
INT0	0	0	1	0	0	4
array bounds	0	0	1	0	1	5
unused-opcodes	0	0	1	1	0	6
ESC opcode	0	0	1	1	1	7
int timer 0	0	1	0	0	0	8
int timer 1	1	0	0	1	0	12
int timer 2	1	0	0	1	1	13
reserved	0	1	0	0	1	9
int DMA 0	0	1	0	1	0	A
int DMA 1	0	1	0	1	1	B
int INT0	0	1	1	0	0	C
int INT1	0	1	1	0	1	D
int INT2	0	1	1	1	0	E
int INT3	0	1	1	1	1	F

4.3.2 Local and System I/O

Port nr	Assignment
	SCC
0000H	Channel B control/status register
0002H	Channel A control/status register
0004H	Channel B data register
0006H	Channel A data register
0022H	Control Port 1 input
0022H	Control Port 2 output
0028H	Control Port 3
002AH	Control Port 4
002CH	FIFO Input
0040H	Networking Control Port PMU 0
0041H	Networking FIFO PMU 0
0042H	Networking Control Port PMU 1
0043H	Networking FIFO PMU 1
"	
"	
005EH	Networking Control Port PMU 15
005FH	Networking FIFO 15

0060-00FFH For information about these ports refer to chapter 3 (Disc Control)

PIC
0008
0009
000A
000B

4.3.2.1 Serial Interfaces

The PMU 186 provides two serial interfaces:

Channel A, a full V24-interface
Channel B, a short distance interface

Channel A is a DTE Interface, used to connect the P3000 System to a communication link via standard Modems. Connection of peripherals to this interface should be done using the cross-wiring of Cable Type 6.

Channel B can be strapped as either a DCE Interface (as in PMU 80) or as a DTE Interface to provide the same interface type on both channels of the PMU , to minimize the number of cable types.

These interfaces are controlled via a dual-channel Z8530-SCC (Serial Communications Controller) and two control ports:
Input port 2 (22H) and Output port 2 (22H).

The next procedure must be used to perform a serial data transmission:

- Program the Z8500-SCC mode of operation
- Program Output Port 2 to set the required V24 signals
- Check Input Port 2 for correct return signals
- Program the Z8500-SCC command (write and/or read)
- Wait for interrupts from Z8500-SCC

The interrupt routine should check the SCC status and react on this with either send or receive data actions.

A SCC Write or Read Register cannot be accessed directly.
Before any write or read action to the SCC Internal registers, the particular register has to be selected.

This is done by sending the address of the register to be selected to the Command Register.

The Z8530-SCC contains a number of Write and Read registers. A particular register is accessed in two steps:

First the register number to be accessed is written into the SCC - Command Register (WR0)- , then the information to or from the register can be read or written.

When used in asynchronous applications, so also for communication to workstations and printers, the System timing signal of 3.072 MHz is input to the SCC and supplied to an internal Baud Rate Generator.

Channel B of the SCC can only be used in asynchronous mode, Channel A can be strapped for Internal or External timing.

When strapped for External Timing, synchronous mode, the modem timing signals are used as Transmit and Receive Clock.

Thus the Z8500-SCC operates in P3000 systems in one of the next timing modes :

- SCC Supplies Receive/Transmit Clocks from internal Baud Rate Generator (Normal Mode)

- SCC receives Receive/Transmit Clock from external source (Synchronous Modem Connections on Channel A)

PROGRAMMING SCC FOR INTERNAL TIMING:

The next values must be send to the Control Port Address of Channel A and/or B :

00	10	Reset Channel
01	10	Interrupts on all Rx Characters or special conditions.
02	50	Interrupt vector set to 50H (Channel B)
03	C0	8-bit Characters
04	44	16 x Clock, Asynchronous, 1 Stopbit, No Parity Bit
05	EA	Transmit 8-bit characters, set DTR and RTS
09	09	Vector Includes Status, Master Interrupt Enable
0A	00	NRZ Mode
0B	55	RxC and TxC from Internal BR Generator, CT113 is TxC
0C	08	Speed LSB (9600 BpS)
0D	00	Speed MSB (9600 BpS)
0E	80	Set Source to BR Generator
0F	00	Disable Interrupts on DCD, CTS, Break etc.

PROGRAMMING SCC FOR EXTERNAL TIMING (CHANNEL A ONLY):

0B	08	RxC and TxC from Interface

4.3.2.1.1 SCC Internal Registers

WRITE REGISTER 0 - COMMAND REGISTER

```
          ---------------------------------
Port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
02H(ch.A) ---------------------------------
00H(ch.B)   |   |   |   |   |   |   |   |
            0   0   0   1   1   0   0   0     Default 18H
            |   |   |   |   |   |   |   |
            |   |   |   |   |   Next Byte Pointer
            |   |   |   |   |   0   0   0  - register 0/8
            |   |   |   |   |   0   0   1  - register 1/9
            |   |   |   |   |   0   1   0  - register 2/10
            |   |   |   |   |   0   1   1  - register 3/11
            |   |   |   |   |   1   0   0  - register 4/12
            |   |   |   |   |   1   0   1  - register 5/13
            |   |   |   |   |   1   1   0  - register 6/14
            |   |   |   |   |   1   1   1  - register 7/15
            |   |   command code
            |   |   0   0   0  - null code
            |   |   0   0   1  - high pointer (register 8-15 select)
            |   |   0   1   0  - reset ext.status interrupts
            |   |   0   1   1  - send abort (SDLC)
            |   |   1   0   0  - enable int. on next Rx char.
            |   |   1   0   1  - reset Tx int. pending
            |   |   1   1   0  - error reset
            |   |   1   1   1  - reset highest IUS
            reset code
            0   0  - null code
            0   1  - reset Rx CRC checker
            1   0  - reset Tx CRC generator
            1   1  - reset Tx underrun/ EOM latch
```

WRITE REGISTER 1 - INTERRUPT CONTROL

```
          ---------------------------------
port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
02H(ch.A) ---------------------------------
00H(ch.B)   |   |   |   |   |   |   |   |
            0   0   0   1   0   0   0   0    Default 10H
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 -- ext.interrupt enable
            |   |   |   |   |   |   1 ------ Tx interrupt enable
            |   |   |   |   |   1 ---------- parity is special condition
            |   |   |   |   0   0 -- Rx int disable
            |   |   |   |   0   1 -- Rx int on first character or special condition
            |   |   |   |   1   0 -- int on all Rx characters or special condition
            |   |   |   |   1   1 -- Rx int on special condition only
            |   |   |
            |   |   1 - wait/ready on Rx/Tx-n
            |   1 ----- wait-n/ready function
            1 --------- wait/ready enable
```

4.3.2.1.1 SCC Internal Registers (continued).

WRITE REGISTER 2 - INTERRUPT VECTOR (COMMON FOR BOTH CHANNELS)

```
          ---------------------------------
Port 00H  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
          ---------------------------------
            |   |   |   |   |   |   |   |
            0   0   1   0   1   1   0   0     Default 50H

          Binary Value = Interrupt Vector
```

WRITE REGISTER 3 - RECEIVER CONTROL

```
          ---------------------------------
Port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
02H(ch.A) ---------------------------------
00H(ch.B)   |   |   |   |   |   |   |   |
            1   1   0   0   0   0   0   1     Default C1H
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 -- Receive Enable
            |   |   |   |   |   |   1 ------ Sync Char. Load Inhibit
            |   |   |   |   |   1 ---------- Address Search Mode(SDLC)
            |   |   |   |   1 -------------- Rx CRC Enable
            |   |   |   1 ------------------ Enter Hunt Phase
            |   |   1 -------------------- Auto Enables
            0   0 -- Rx 5-bits/character
            0   1 -- Rx 7-bits/character
            1   0 -- Rx 6-bits/character
            1   1 -- Rx 8-bits/character
```

WRITE REGISTER 4 - RECEIVE/TRANSMIT CONTROL

```
          ---------------------------------
Port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
02H(ch.A) ---------------------------------
00H(ch.B)   |   |   |   |   |   |   |   |
            0   1   0   0   0   1   0   0     Default 44H
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 -- Parity Enable
            |   |   |   |   |   |   1 ------ Parity Even/Odd-N
            |   |   |   |   |   0   0 - Synchronous Mode
            |   |   |   |   |   0   1 - 1 stopbit/char
            |   |   |   |   |   1   0 - 1.5 stopbit/char
            |   |   |   |   |   1   1 - 2 stopbits/char
            |   |   |   |   0   0 - 8  bit sync character
            |   |   |   |   0   1 - 16 bit sync character
            |   |   |   |   1   0 - SDLC Mode
            |   |   |   |   1   1 - External Sync
            0   0 - x  1 Clock
            0   1 - x 16 Clock
            1   0 - x 32 Clock
            1   1 - x 64 Clock
```

WRITE REGISTER 5 - TRANSMITTER CONTROL

```
          ---------------------------------
port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
02H(ch.A) ---------------------------------
00H(ch.B)   |   |   |   |   |   |   |   |
            1   1   1   0   1   0   1   0    Default EAH
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 -- Tx CRC Enable
            |   |   |   |   |   |   1 ------ RTS
            |   |   |   |   |   1 ---------- SDLC-n/CRC16 Polynom.
            |   |   |   |   1 -------------- Tx Enable
            |   |   |   1 ------------------ Send Break
            |   0   0 - Tx 5 bits/character
            |   0   1 - Tx 7 bits/character
            |   1   0 - Tx 6 bits/character
            |   1   1 - Tx 8 bits/character
            |
            1 - DTR
```

WRITE REGISTER 6 - TRANSMIT SYNC CHARACTER

```
          ---------------------------------
port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
02H(ch.A) ---------------------------------
00H(ch.B)   |   |   |   |   |   |   |   |
```

Contains SYNC Character Code (Synchr. Mode)
or SDLC Address Field (SDLC Mode)

WRITE REGISTER 7 - RECEIVE SYNC CHARACTER

```
          ---------------------------------
port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
02H(ch.A) ---------------------------------
00H(ch.B)   |   |   |   |   |   |   |   |
```

Contains SYNC Character Code (Synchr. Mode)
or SDLC Address Field (SDLC Mode)

WRITE REGISTER 8 - TRANSMIT BUFFER

This buffer contains the character to be tansmitted, it is normally loaded via a write to port 06 or 04 (Data Buffer).

WRITE REGISTER 9 - MASTER INTERRUPT CONTROL / RESET

```
          ---------------------------------
port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
02H(ch.A) ---------------------------------
00H(ch.B)   |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 -- VIS (Ch.A and B)
            |   |   |   |   |   |   1 ------ NV  (Ch.A and B)
            |   |   |   |   |   1 ---------- DLC (Ch.A and B)
            |   |   |   |   1 -------------- MIE (Ch.A and B)
            |   |   |   1 ------------------ Status High/Low-n
            |   |   0---------------------- Not Used
            0   0 - No reset
            0   1 - Reset Channel A
            1   0 - Reset Channel B
            1   1 - Force Hardware Reset
```

WRITE REGISTER 10 - MISCELLANEOUS CONTROL BITS

```
          ---------------------------------
port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
02H(ch.A) ---------------------------------
00H(ch.B)   |   |   |   |   |   |   |   |
            0   0   0   0   0   0   0   0    Default 00H
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 -- 8 BIT SYNC
            |   |   |   |   |   |   1 ------ LOOP
            |   |   |   |   |   1 ---------- Abort/Flag-n on underrun
            |   |   |   |   1 -------------- Mark/Flag-n idle
            |   |   |   1 ------------------ Go active on poll
            |   0   0 - NRZ
            |   0   1 - NRZI
            |   1   0 - FM1
            |   1   1 - FM0
             ---------- CRC Preset Ones/Zeroes-n
```

WRITE REGISTER 11 - CLOCK MODE CONTROL

```
    ---------------------------------
    | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |      OUTPUT
    ---------------------------------
      0   1   0   1   0   1   0   1        DEFAULT 55H
      |   |   |   |   |   |   |   |
      |   |   |   |   |   |   0   0  - TRxC out = xtal output
      |   |   |   |   |   |   0   1  - TRxC out = transmit clock
      |   |   |   |   |   |   1   0  - TRxC out = br generator
      |   |   |   |   |   |   1   1  - TRxC out = dpll output
      |   |   |   |   |    ----------- TRxC on
      |   |   |   0   0 -------------- RTxC pin = transmit clock
      |   |   |   0   1 -------------- TRxC pin = transmit clock
      |   |   |   1   0 -------------- BR gen = transmit clock
      |   |   |   1   1 -------------- DPLL output = transmit clock
      |   0   0 ---------------------- RTxC pin = receive clock
      |   0   1 ---------------------- TRxC pin = receive clock
      |   1   0 ---------------------- BR gen = receive clock
      |   1   1 ---------------------- DPLL output = receive clock
      ------------------------------- RTxC xtal
```

WRITE REGISTER 12 - LSB BAUD RATE GENERATOR CONSTANT

WRITE REGISTER 13 - MSB BAUD RATE GENERATOR CONSTANT

For P3000 the next formular must be used to calculate the time constant value for a required baud rate in asynchronous mode:

Binary value = (3072000 / (32 * Baudrate))-2

WRITE REGISTER 14 - MISCELLANEOUS CONTROL BITS

```
          ---------------------------------
port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
02H(ch.A) ---------------------------------
00H(ch.B)   |   |   |   |   |   |   |   |
            1   0   0   0   0   0   0   0    Default 80H
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 -- BR Generator Enable
            |   |   |   |   |   |   1 ------ BR Generator Source
            |   |   |   |   |   1 ---------- DTR-n/Request Function
            |   |   |   |   1 -------------- Auto Echo
            |   |   |   1 ------------------ Local Loop
            |   |   |
            0   0   0 - Null Command
            0   0   1 - Enter Search Mode
            0   1   0 - Reset Missing Clock
            0   1   1 - Disable PLL
            1   0   0 - Set source = BR Generator
            1   0   1 - Set source = RTxC
            1   1   0 - Set FM Mode
            1   1   1 - Set NRZI Mode
```

WRITE REGISTER 15 - EXTERNAL / STATUS INTERRUPT CONTROL

```
          ---------------------------------
port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   OUTPUT
02H(ch.A) ---------------------------------
00H(ch.B)   |   |   |   |   |   |   |   |
            0   0   0   0   0   0   0   0    Default 00H
            |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   0 -- Not Used
            |   |   |   |   |   |   1 ------ Zero Count IE
            |   |   |   |   |   0 ---------- Not Used
            |   |   |   |   1 -------------- DCD IE
            |   |   |   1 ------------------ SYNC/HUNT IE
            |   |   1 -------------------- CTS IE
            |   1 ---------------------- Tx Underrun IE
            1 ------------------------ Break/Abort IE
```

4.3.2.1.1 SCC Internal Registers (continued).

READ REGISTER 0 - STATUS

```
          ---------------------------------
port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   INPUT
02H(ch.A) ---------------------------------
00H(ch.B)   |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 -- Rx Char. Available
            |   |   |   |   |   |   1 ------ Zero Count
            |   |   |   |   |   1 ---------- Tx Buffer Empty
            |   |   |   |   1 -------------- DCD
            |   |   |   1 ------------------ Sync/Hunt(Not Used)
            |   |   1 ---------------------- CTS
            |   1 ------------------------- Tx Underrun/EOM
            1 ----------------------------- Break/Abort
```

READ REGISTER 1 - RECEIVE STATUS

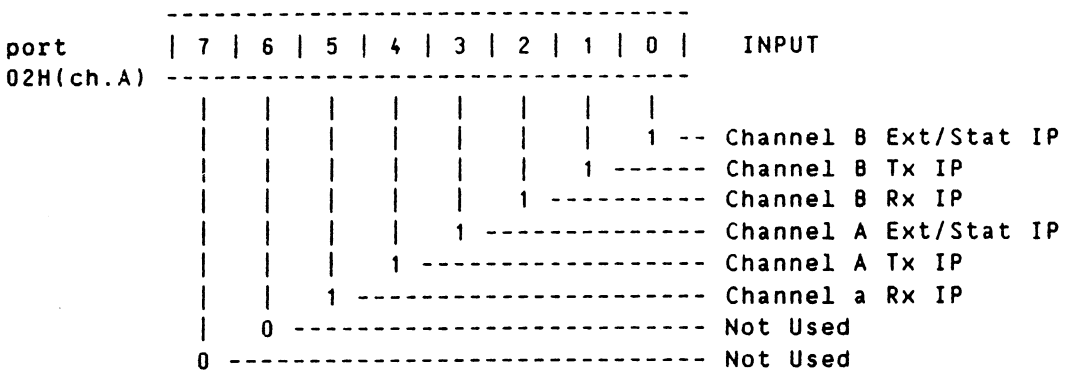
```
          ---------------------------------
port      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   INPUT
02H(ch.A)  ---------------------------------
00H(ch.B)   |   |   |   |   |   |   |   |
            |   |   |   |   |   |   |   1 -- All Sent (Tx Empty)
            |   |   |   |   SDLC-Residue
            |   |   |   |   1   0   0       3 bits left in last I-word
            |   |   |   |   0   1   0       4
            |   |   |   |   1   1   0       5
            |   |   |   |   0   0   1       6
            |   |   |   |   1   0   1       7
            |   |   |   |   0   1   1       8
            |   |   |   |   1   1   1       9
            |   |   |   |   0   0   0      10 bits left in last I-word
            |   |   |   |
            |   |   |   1-- Parity Error
            |   |   1------ Rx Overrun Error
            |   1---------- CRC/Framing Error
            1-------------- End Of Frame(SDLC)
```

READ REGISTER 2 - INTERRUPT VECTOR (COMMON FOR CHANNEL A/B)

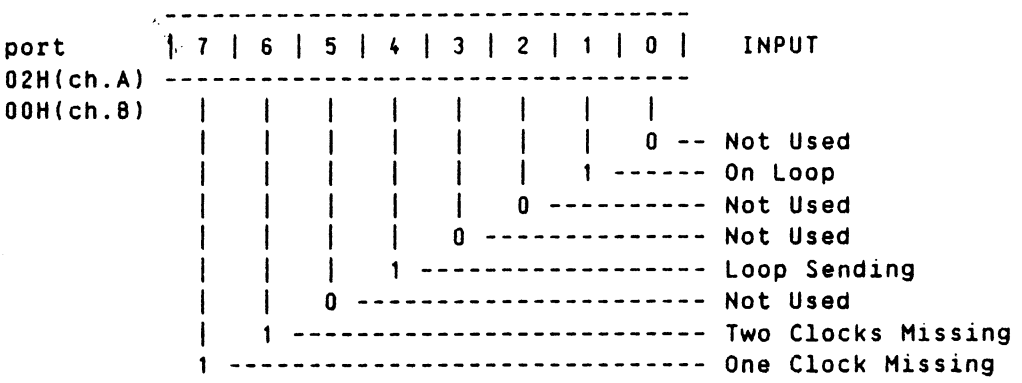
```
          ---------------------------------
Port 00H  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   INPUT
          ---------------------------------
            |   |   |   |   |   |   |   |
```

Contains Modified Interrupt Vector in Channel B

READ REGISTER 3 - INTERRUPT PENDING BITS (Channel A only)



READ REGISTER 10 - MISCELLANEOUS STATUS

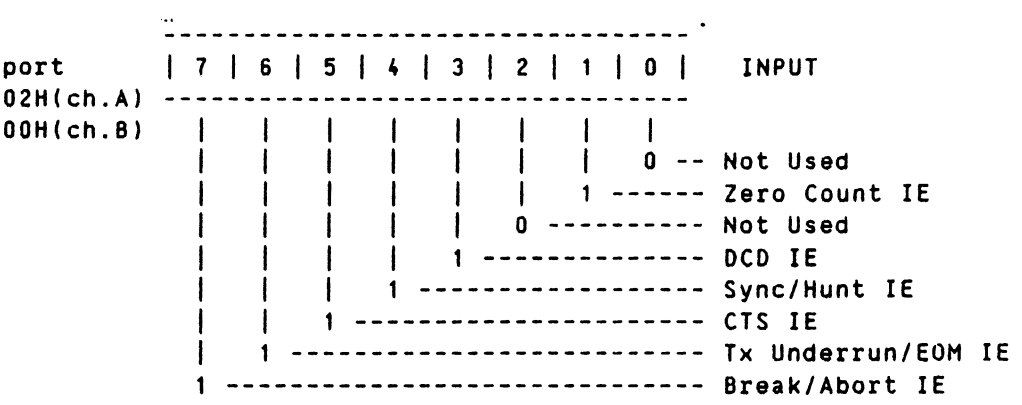


READ REGISTER 12 - LSB BAUD RATE CONSTANT

READ REGISTER 13 - MSB BAUD RATE CONSTANT

These registers contain the programmed value of the internal Baud Rate Generator time constant.

READ REGISTER 15 - EXTERNAL/STATUS INTERRUPT INFO



4.3.2.1.2 Channel A Interface Control

The next interface signals are used at channel A, the list explains via which port the signals can be accessed.

PIN	CCITT	NAME	I/O	PORT	BIT	DESCRIPTION
b1	101	GND	------			
b7	102	L	------			
b2	103	TMD	OUT	06H	0-7	DATA OUT
b3	104	RCD	IN	06H	0-7	DATA IN
b4	105	RTS	OUT	WR5	1	REQUEST TO SEND
b5	106	CTS	IN	RR0	5	CLEAR TO SEND
b6	107	DSR	IN	RR0	3	DATA SET READY
a7	108.2	DTR	OUT	28H	4	DATA TERMINAL READY
b8	109	DCD	IN	22H	6	CARRIER DETECTED
a10	111	DRS	-------			HIGH
a11	113	TSET(M)	-------			INT.CLOCK TO MODEM)
a2	114	TSET	Strap			SYNCHR.TxCLOCK FROM MODEM
a4	115	RSET	Strap			SYNCHR.RxCLOCK FROM MODEM
a9	125	RIN	IN	22H	6	CALLING INDICATOR
a8	140	REML	OUT	28H	5	REMOTE LOOP SETTING
a5	141	LOCL	OUT	28H	6	LOCAL LOOP SETTING
a12	142	TIN	IN	22H	5	TEST INDICATOR
			IN	20H	3	RPON (CT109/CT125)

NOTE: CT109 and CT125 can be strapped to supply Remote Power ON (RPON). CT109 or CT125 can be read at port 22H, bit 6 (or-ed).

4.3.2.1.3 Channel B Interface Control

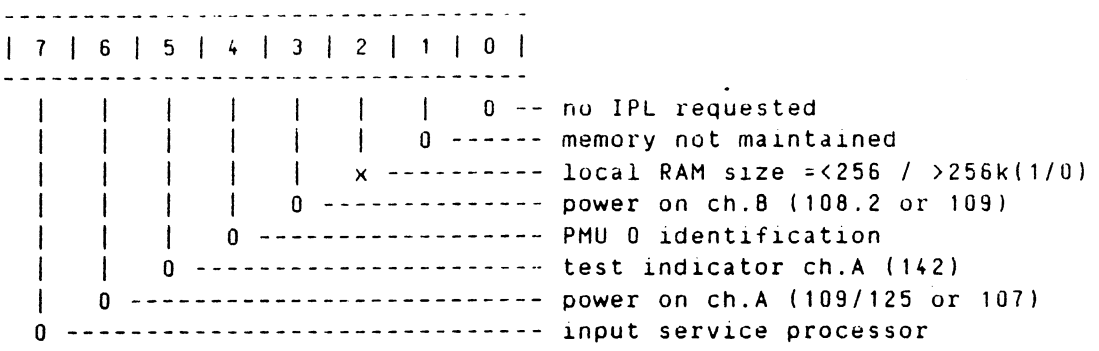
Channel B has limited control features . It is designed as Short Distance Interface, for direct connection of peripherals.
It can be strapped as DTE or DCE interface.
The next interface signals are used at channel B, the list explains via which port the signals can be accessed.

STRAPPED AS :			DCE INTERFACE			DTE INTERFACE		
			-------------			-------------		
PIN	CCITT	NAME	I/O	PORT	BIT	I/O	PORT	BIT
b1	101	GND	------			-------		
b7	102	L	------			-------		
b3	104	RCD	OUT	04H	0-7	IN	04H	0-7
b2	103	TMD	IN	04H	0-7	OUT	04H	0-7
b5	106	CTS	OUT	WR5	7	IN	RR0	5
b6	107	DSR	IN	RR0	5	IN	RR0	4
b7	108	DTR	IN	RR0	5	OUT	WR5	7
b4	105	RTS	IN	RR0	3	OUT	WR5	1 *
b8	109	DCD	OUT	WR5	1	IN	RR0	3 *

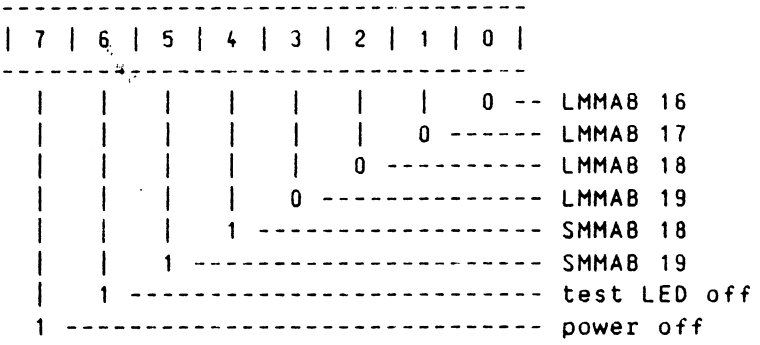
NOTE: CT108.2 can be strapped to give Remote Power ON (RPON).
RPON condition can be read at control port 1 (22H), bit 3.
* = Not used in protocol

4.3.3 Control Port Overview

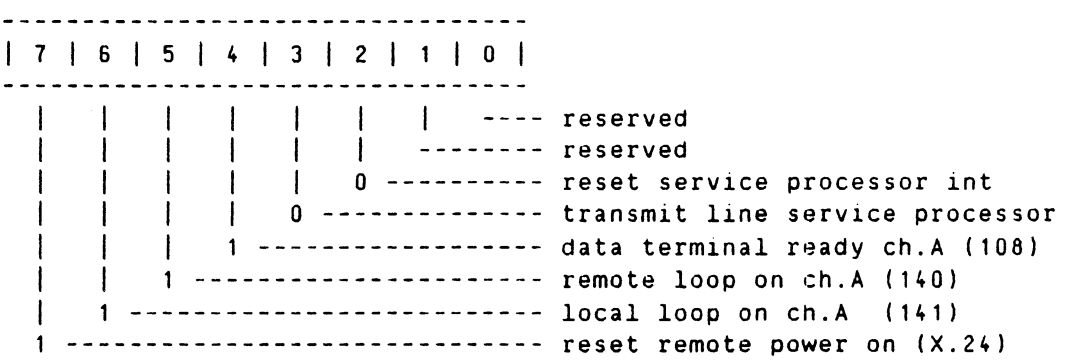
CONTROL PORT 1 (0022H - Input Port)



CONTROL PORT 2 (0022H - Output Port)



CONTROL PORT 3 (FF28H - Output Port)



CONTROL PORT 4 (FF2AH - Output Port)

This is a virtual output port. Accessing of this port causes a reset signal on the interprocessor communication flipflop.
An output to this port should typically be done within an interprocessor communication interrupt service routine.

4.3.4 Networking

From Rel.3 onwards the P3000 system can have three types of processors :

- A File Server (Master)
- DC-Node(s)
- Slave(s)

A DC-Node can be seen as a Slave for the File Server and as a Master for the Slaves.
Both the File Server and the DC-Node can access the bus.
A PMU80 or PMU80-1 can NOT act as DC-node.

PMU80-3 and PMU 186 boards have additional facilities for bus transfer.
Between the EMM bus and the local bus is a FIFO buffer located which is used to communicate between the processors.
The FIFO processing is only used if all PMU boards are able to perform FIFO processing (all PMU 80-3 and/or PMU 186).

Thus, the communication is executed via a polling mechanism of the Network Drivers (PMU 80-1) or via the FIFO mechanism (PMU 80-3,PMU 186).

Data transfers are always done via the system memory mapping.

A Networking Control port is available on every board to allow some interrupting of slave boards by the master processor.

4.3.4.1 Networking Control Port

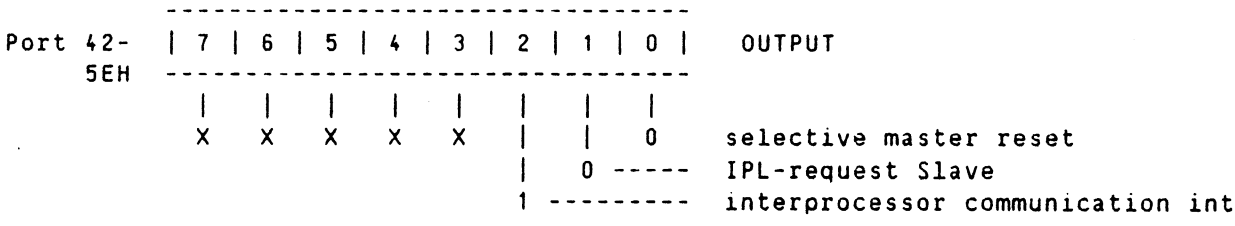
The networking control port is represented as a destination on the EMM-bus and can be directly accessed by output operations on the bus. Any type of PMU can set up special control lines to another PMU.

```
Port 40   PMU 0
     42   PMU 1
     44   PMU 2
     46   PMU 3
     48   PMU 4

etc. till:

Port 5E   PMU 15
```

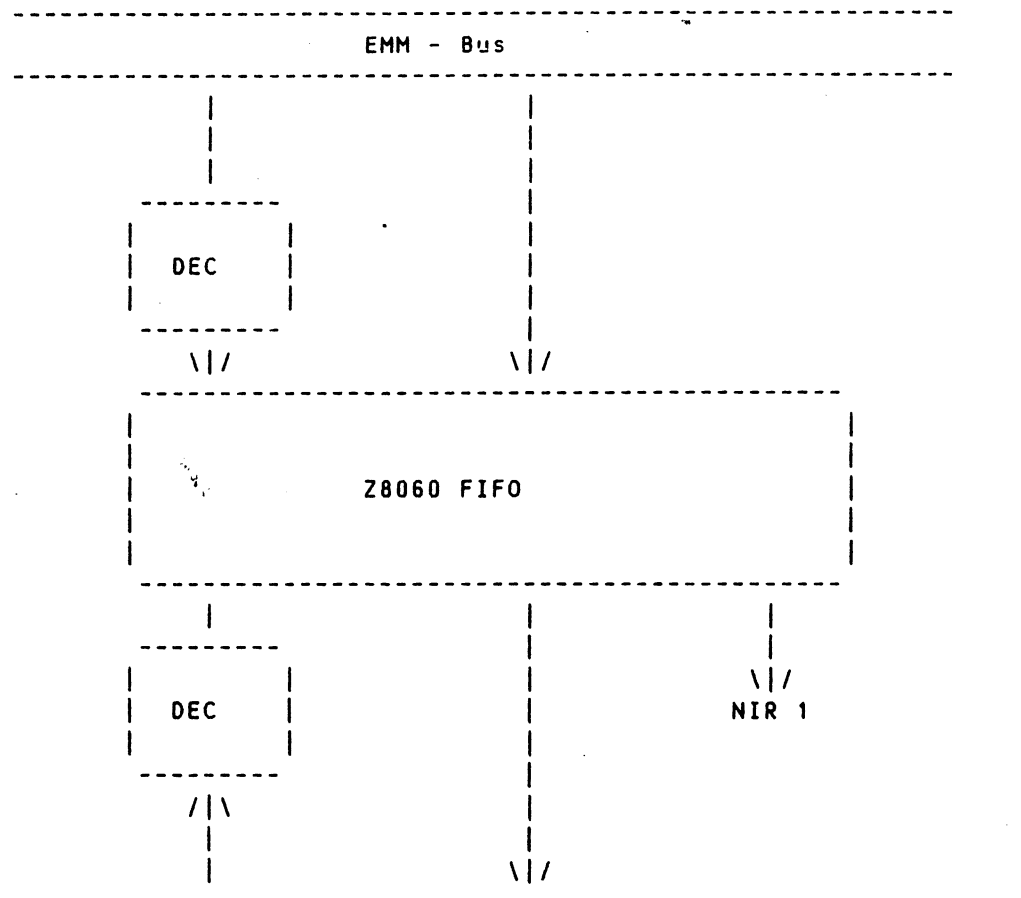
NETWORKING CONTROL PORT



Bit 0 gives a hardware reset of the PMU, this port excluded.
Bit 1 is read by the slave at Port 1 (bit 0), used to force the slave for a new IPL.
Bit 2 forces an interprocessor communication interrupt.

4.3.4.2 FIFO Networking

The PMU 186 board is equipped with a Dual Channel 8-bit hardware FIFO, Z8060.
The FIFO is located between EMM-bus and Local-bus as follows:



The Internal FIFO Status " NOT EMPTY " causes an Interrupt (NIR1) to the processor.

The FIFO can be regarded as an output port at the EMM Bus (not readable).
On the Local Bus it is available as an input port (readable only).

The port address to load the FIFO via the EMM Bus is as follows:

41H PMU 0 FIFO
43H PMU 1 FIFO
45H PMU 2 FIFO
47H PMU 3 FIFO
49H PMU 4 FIFO
5FH PMU 15 FIFO

The port address to read the FIFO via the Local Bus is 002CH.

Note that the FIFO inverts the data between EMM and Local Bus.

4.3.4.3 FIFO Bit Assignment

The Slave can inform the Master about a required action by sending a command into the FIFO of the Master.
After execution of this command the Master informs the Slave about this via the Networking Control Port (see 5.3.4.1)

Note that this FIFO Command Processing is only used if all processor boards are PMU 80-3 or PMU 186. In all other circumstances the Master should poll the slave at regular moments to check if the Slave requires service.

FIFO COMMAND LAYOUT

```
 -------------------------------
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
 -------------------------------
  |   |   |   |   |   |   |   |
  |   |   |   |   Processor Id:
  |   |   |   |   0   0   0   0 -- PMU 0
  |   |   |   |   0   0   0   1 -- PMU 1
  |   |   |   |   0   0   1   0 -- PMU 2
  |   |   |   |   .   .   .   . -- upto:
  |   |   |   |   1   1   1   1 -- PMU 15
   Command
  0   0   0   0 ------------------ Acknowledge
  0   0   0   1 ------------------ Send - Request
  0   0   1   0 ------------------ IPL - Ready
  0   1   0   0 ------------------ Terminal - Off
  1   0   0   0 ------------------ DC - Buffer - Empty
```