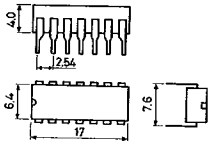
DIGITAL MONOLITHIC INTEGRATED CIRCUITS

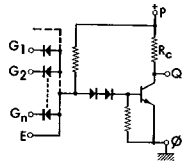
FC family (Diode-Transistor Logic)
Standard temperature range

Supply voltage	V_P	6.0 V
Operating ambient temperature	T_{amb}	0 to 75°C

* collector resistor R_c omitted



Package D1 (dual in-line)
Dimensions in mm



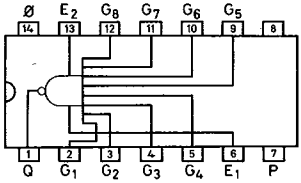
Basic gate circuit

CHARACTERISTICS at T_{amb} = 25°C (each gate)

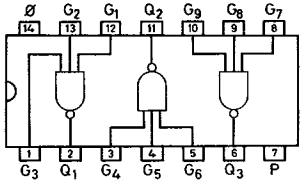
Type number	*Description (positive logic)*	*Propagation delay time typ. (ns)*	*Available fan-out min.*	*Noise margin min (V)*	*Noise margin typ.(V)**	*Power consumption typ.(mW)*	*Package*
FCH101*	Single 8-input	31	8	0.60	1.2	7.0	D1
FCH111	NAND gate	31	8	0.60	1.2	11.0	D1
FCH121*	Dual 4-input	31	8	0.60	1.2	7.0	D1
FCH131	NAND gate	31	8	0.60	1.2	11.0	D1
FCH141*	Triple 3-3-2 input	31	8	0.60	1.2	7.0	D1
FCH161	NAND gate	31	8	0.60	1.2	11.0	D1
FCH151*	Triple 3-input	31	8	0.60	1.2	7.0	D1
FCH171	NAND gate	31	8	0.60	1.2	11.0	D1
FCH181*	Quadruple 2-input	31	8	0.60	1.2	7.0	D1
FCH191	NAND gate	31	8	0.60	1.2	11.0	D1
FCH201*	Sextuple	31	8	0.60	1.2	7.0	D1
FCH211	inverter	31	8	0.60	1.2	11.0	D1

Terminal connections (top view)

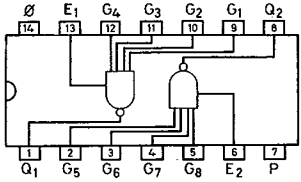
FCH101
FCH111



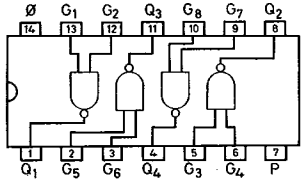
FCH151
FCH171



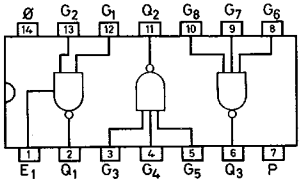
FCH121
FCH131



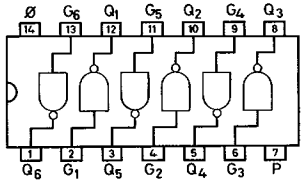
FCH181
FCH191



FCH141
FCH161

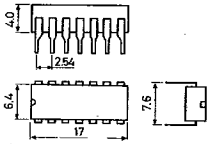


FCH201
FCH211

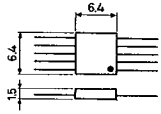


DIGITAL MONOLITHIC INTEGRATED CIRCUITS
FC family (Diode-Transistor Logic)
Standard temperature range

Supply voltage	V_P	6.0 V
Operating ambient temperature	T_{amb}	0 to 75 °C



Package D1 (dual in-line)
Dimensions in mm

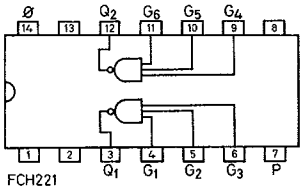


Package C1 (flat-pack)
Dimensions in mm

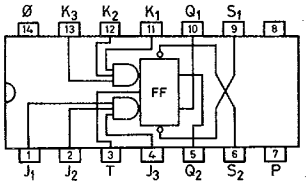
CHARACTERISTICS at $T_{amb} = 25$ °C

Type number	*Description (positive logic)*	*Propagation delay time (ns)*	*Maximum clock rate min. (MHz)*	*Available fan-out min.*	*Noise margin min. (V)*	*Power consumption (mW)*	*Package*
FCH221	Dual 3-input line driver NAND gate	max. 93		16	0.60	typ. 11.0 (each gate)	D1
FCJ101	Single JK flip-flop	max. 110	7	6	0.45	max. 69	D1
FCJ111	Single JK master-slave flip-flop	typ. 110	3	8	0.60	typ. 73	D1
FCK101	Monostable multivibrator (Output pulse width 100 ns to 1 s)	typ. 75	2.5	8	0.60	typ. 110	C1
FCL101	Level detector (Schmitt trigger)		1	3		max. 19	D1
FCY101	Triple gate input expander (10-diode array)						D1

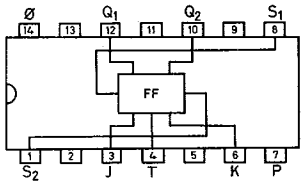
Terminal connections (top view)



FCH221

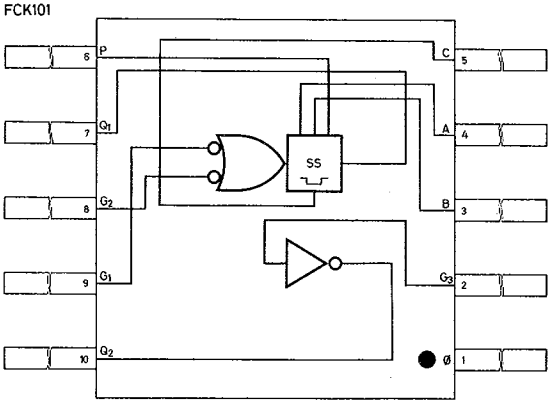


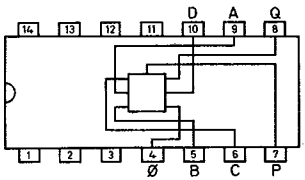
FCJ101



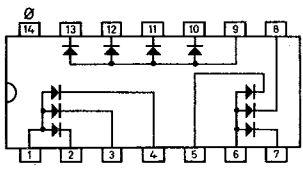
FCJ111

FCK101





FCL101

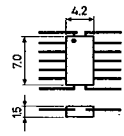


FCY101

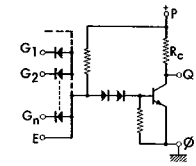
DIGITAL MONOLITHIC INTEGRATED CIRCUITS
FC family (Diode-Transistor Logic)
Extended temperature range

Supply voltage V_P 6.0 V
Operating ambient temperature T_{amb} −55 to +125°C

* collector resistor R_c omitted



Package E2 (flat-pack)
Dimensions in mm



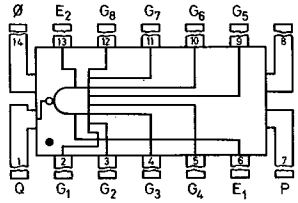
Basic gate circuit

CHARACTERISTICS at T_{amb} = 25°C (each gate)

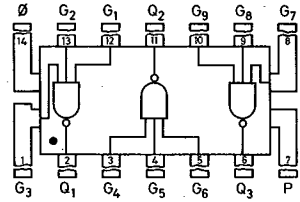
Type number	*Description (positive logic)*	*Propagation delay time typ. (ns)*	*Available fan-out min.*	*Noise margin*		*Power consumption typ. (mW)*	*Package*
				min. (V)	*typ. (V)*		
FCH102*	Single 8-input	32	11	0.55	1.2	7.0	E2
FCH112	NAND gate	32	11	0.55	1.2	10.5	E2
FCH122*	Dual 4-input	32	11	0.55	1.2	7.0	E2
FCH132	NAND gate	32	11	0.55	1.2	10.5	E2
FCH142*	Triple 3-3-2-input	32	11	0.55	1.2	7.0	E2
FCH162	NAND gate	32	11	0.55	1.2	10.5	E2
FCH152*	Triple 3-input	32	11	0.55	1.2	7.0	E2
FCH172	NAND gate	32	11	0.55	1.2	10.5	E2
FCH182*	Quadruple 2-input	32	11	0.55	1.2	7.0	E2
FCH192	NAND gate	32	11	0.55	1.2	10.5	E2
FCH202*	Sextuple	32	11	0.55	1.2	7.0	E2
FCH212	inverter	32	11	0.55	1.2	10.5	E2

Terminal connections (top view)

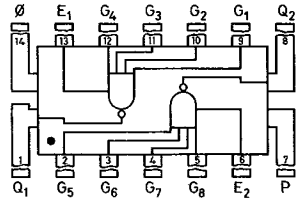
FCH102
FCH112



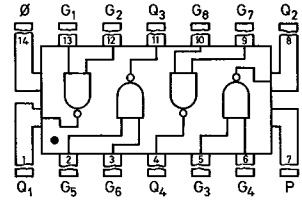
FCH152
FCH172



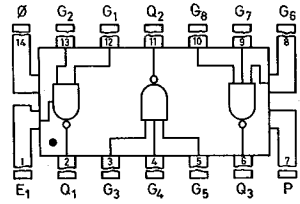
FCH122
FCH132



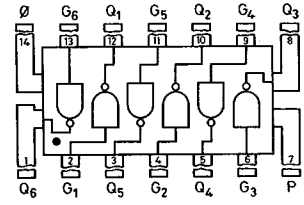
FCH182
FCH192



FCH142
FCH162



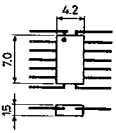
FCH202
FCH212



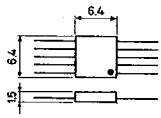
DIGITAL MONOLITHIC INTEGRATED CIRCUITS

FC family (Diode-Transistor Logic)
Extended temperature range

Supply voltage	V_P	6.0 V
Operating ambient temperature	T_{amb}	−55 to +125°C



Package E2 (flat-pack)
Dimensions in mm



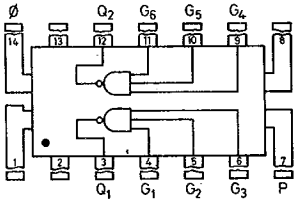
Package C1 (flat-pack)
Dimensions in mm

CHARACTERISTICS at $T_{amb}=25°C$

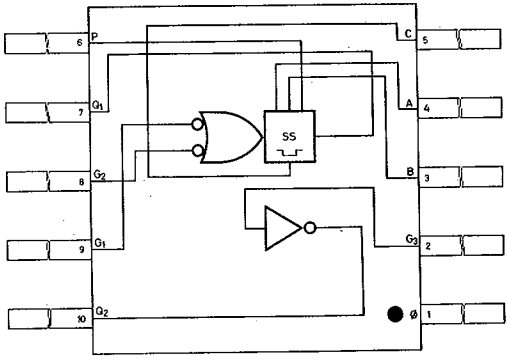
Type number	*Description (positive logic)*	*Propagation delay time (ns)*	*Maximum clock rate min. (MHz)*	*Available fan-out min.*	*Noise margin min. (V)*	*Power consumption (mW)*	*Package*
FCH222	Dual 3-input line driver NAND gate	max. 75		20	0.55	max. 17	E2
FCJ102	Single JK flip-flop	max. 60	10	10	0.55	max. 55	E2
FCK102	Monostable multivibrator (Output pulse width 100 ns to 1 s)	max. 100	2.5	11	0.55	typ. 105	C1
FCL102	Level detector (Schmitt trigger)		1	3		max. 19	E2
FCY102	Triple gate input expander (10-diode array)						E2

Terminal connections (top view)

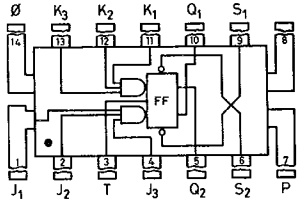
FCH222



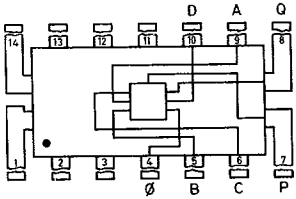
FCK102



FCJ102



FCL102



FCY102